数字电路作业

Verilog编程-Homework

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> 编程题 1： 用Verilog HDL描述第五章习题P5.20的电路

编程题1电路源码：

```
module mydelay(input CLK,input r,output [2:0] q);
reg [2:0] a;
reg [1:0] b;

always@(r)begin
    if(~r) begin a<=0; end
end

always@(posedge CLK) begin
    if(r)begin
        a<=a+1;
        end
    end

assign q=a;
endmodule
```

编程题1测试模块源码：

```
`timescale 1ns/1ps
module test ;
    reg CLK;
    reg r;
    wire [2:0] q;

    mydelay dut(.CLK(CLK),.r(r),.q(q));
initial begin
    CLK=0;
    forever begin
        #50 CLK=~CLK;
    end
end
initial begin
    r=0;
    #125 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
```

```
    #50 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
    #50 r=1;
    $finish();
end
initial begin
    $dumpfile("hw1_delay_test.vcd");
    $dumpvars(0);
end
endmodule
```

编程题1仿真波形：