JIWON CHOE

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RESEARCH INTERESTS

My dissertation focuses on the **software-hardware co-design of general-purpose concurrent data structures that efficiently utilize emerging near-data-processing (NDP) architectures**. NDP architectures allow host processors to offload data-intensive computations to near-memory compute units in order to reduce off-chip data movement and improve performance and energy savings. The *NDP-aware* concurrent data structures – provided as packaged software libraries – can lower barriers of NDP adoption by hiding the complexities of utilizing new NDP hardware from the programmer. Yet, this is a challenging problem, for the NDP-aware data structures must be carefully designed in order to preserve the high concurrency, correctness guarantees, and at times high on-chip cache locality provided by existing data structures which are highly optimized for conventional architectures. At the same time, they must still take full advantage of the features and work around the challenges introduced by the new architecture.

EDUCATION

Brown University, Providence, RI, USA 08/2016 - present
Ph.D. Candidate in **Computer Science** (Expected graduation date: 12/2021)
Sc.M. in **Computer Science** (05/2018)
Dissertation Title: Concurrent Data Structures with Near-Data-Processing: Software-Hardware Co-Design
Advisors: Professors Iris Bahar & Maurice Herlihy

Rice University, Houston, TX, USA 08/2009 - 05/2013
B.S.E.E. in **Electrical Engineering**, *cum laude*
B.A. in **Computer Science**, *cum laude*

PUBLICATIONS

Jiwon Choe, Andrew Crotty, Tali Moreshet, Maurice Herlihy, R. Iris Bahar.
(title redacted). ***Under review*** In *27th ACM SIGPLAN Annual Symposium on Principles and Practice of Parallel Programming* (**PPoPP 2022**).
Index data structures in online transaction processing systems often have *hierarchical* topologies, which provide high on-chip cache locality and thus low access latencies. In this work, we propose NDP-enabled *hybrid* data structures, which combine the data structure topology with features provided by new NDP architectures to further enhance the cache efficiency of these data structures.

Jiwon Choe, Amy Huang, Tali Moreshet, Maurice Herlihy, R. Iris Bahar.
Concurrent Data Structures with Near-Data-Processing: an Architecture-Aware Implementation. In *31st ACM Symposium on Parallelism in Algorithms and Architectures* (**SPAA 2019**).
https://dl.acm.org/citation.cfm?id=3323191
This empirical evaluation of NDP-based concurrent data structures provides insight into memory access patterns of data structures and identifies the minimal hardware support needed in the near-data compute units in order to increase throughput and reduce energy consumption.

Jiwon Choe, Tali Moreshet, R. Iris Bahar, Maurice Herlihy.
Attacking Memory-Hard scrypt with Near-Data-Processing (extended abstract). In *The International Symposium on Memory Systems* (**MEMSYS 2019**).
https://dl.acm.org/citation.cfm?id=3357570

Memory-hard cryptographic functions exploit the non-trivial memory access costs of DRAM to hinder brute-force security attacks. This preliminary investigation focuses on `scrypt`, a widely used memory-hard key-derivation function, to look into how compute-capable memory may impact the security of such memory-hard functions.

OPEN SOURCE TOOLS

Brown-SMCSim: gem5 full-system simulator for near-data-processing
`https://github.com/jiwon-choe/Brown-SMCSim`
A gem5 full-system simulator that includes the architecture support and full software stack for near-data-processing. Extended from Azarkhish *et al.*'s SMCSim project. Used for evaluation in SPAA '19 and MEMSYS '19 papers.

WORK EXPERIENCE

Software Engineer at **Oracle**, Santa Clara, CA 07/2013 - 12/2015
Single Server Management – Hardware Management Pack
Developed cross-platform, cross-OS software for monitoring and maintaining the status of various hardware components on Oracle servers.

HONORS & AWARDS

2020 **Sigma Xi**, Brown University
2019 **Best Student Presentation Award**
The International Symposium on Memory Systems (MEMSYS 2019)
2018 **Cadence Women in Tech Scholarship**
$5,000 award for women with strong academic record and leadership/passion in technology
2013 **Tau Beta Pi**, School of Engineering, Rice University
2012 **Eta Kappa Nu**, ECE Department, Rice University

TEACHING EXPERIENCE

ENGN 1630: Digital Electronics Systems Design Brown University
Graduate Teaching Assistant Fall 2019
Filled in for lectures; made problem sets and held several review sessions to help students prepare for exams; made and graded exam problems.

TRAINING & DEVELOPMENT

Teaching Certificate Program: Reflective Teaching (Fall 2019)
Brown University Sheridan Center for Teaching & Learning
Completed four seminar modules designed to develop and refine fundamental teaching and assessment strategies and communication skills based on how students learn, as well as a teaching observation in a real classroom environment to receive constructive feedback on my teaching.

SERVICES

Mentoring

- Research Mentoring for Undergraduate, Master's, & Early Ph.D. Students (Summer 2017 – present)
- Brown CS 1st Year Ph.D. Student Mentoring (Fall 2018 – Fall 2019)

Conference Volunteering

- Student Volunteer at ASPLOS 2019

Department Services

- Student Volunteer for Brown CS Ph.D. Admissions Committee (01/2020)
- Organizer for Brown CS New Graduate Student Orientation (Summer 2017)