JIWON CHOE

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EDUCATION

Brown University, Providence, RI, USA

08/2016 - present

Ph.D. Candidate in Computer Science

Sc.M. in Computer Science (05/2018)

Advised by: Professors Iris Bahar & Maurice Herlihy

Research Interests: The hardware-software co-design of concurrent data structures and algorithms with emerging memory technologies, such as compute-capable memory or non-volatile memory.

Rice University, Houston, TX, USA

08/2009 - 05/2013

B.S.E.E. in Electrical Engineering, cum laude

B.A. in Computer Science, cum laude

PH.D. THESIS WORK

Concurrent Data Structures with Near-Data-Processing (NDP)

related publications:

Jiwon Choe, Amy Huang, Tali Moreshet, Maurice Herlihy, R. Iris Bahar. Concurrent Data Structures with Near-Data-Processing: an Architecture-Aware Implementation. In 31st ACM Symposium on Parallelism in Algorithms and Architectures (SPAA 2019).

open-source framework: https://www.github.com/jiwon-choe/Brown-SMCSim

In the SPAA 2019 paper, NDP-based concurrent data structures that leverage the flat-combining synchronization scheme were implemented and evaluated on Brown-SMCSim, a gem5-based full-system NDP architecture simulator. This yielded a more realistic performance, energy, and power analysis compared to the prior theoretical analysis. However, we also show that lightweight hardware modifications can lead to significant improvements in performance and energy savings with the NDP-based concurrent data structures, without any modifications to the software.

More recently, I have been looking into how *large yet cache-friendly* concurrent data structures can be integrated with NDP, in order to take advantage of concurrency, host processor cache locality, and computation near memory.

WORK EXPERIENCE

Software Engineer at Oracle, Santa Clara, CA

07/2013 - 12/2015

Single Server Management - Hardware Management Pack

Developed cross-platform, cross-OS software for monitoring and maintaining the status of various hardware components on Oracle servers.

HONORS & AWARDS

2019 SPAA Student Travel Grant

31st ACM Symposium on Parallelism in Algorithms and Architectures
1st author/presenter of paper at conference

2018 Cadence Women in Tech Scholarship

\$5,000 award for women with strong academic record and leadership/passion in technology

2018 HPCA Student Travel Grant

24th IEEE International Symposium on High-Performance Computer Architecture

- 2013 Tau Beta Pi, School of Engineering, Rice University
- 2012 Eta Kappa Nu, ECE Department, Rice University

TEACHING EXPERIENCE

ELEC 220: Fundamentals of Computer Engineering

Rice University Spring 2011

Lab Assistant

Helped organize and proceed labs on: digital logic circuits and assembly language.

ELEC 241: Fundamentals of Electrical Engineering I

Rice University Fall 2011

Course Assistant

Held weekly help sessions for problem sets on: time and frequency domain signal analysis, analog and digital signal processing, and signal transmission.

ELEC 242: Fundamentals of Electrical Engineering II

Rice University

Course Assistant

Spring 2012

Held weekly help sessions for problem sets on: basic electronic devices, circuits, and electromechanical systems.

PRESENTATIONS

06/2019	Concurrent Data Structures with Near-Data-Processing: an Architecture-Aware
	Implementation

31st ACM Symposium on Parallelism in Algorithms and Architectures

01/2019 Hardware-Software Coordination for High-Performance Concurrent Data Structures with Near-Data-Processing

2019 Boston Area Architecture Workshop

01/2018 Managing Concurrent Data Structures with Processing-In-Memory 2018 Boston Area Architecture Workshop

10/2017 Managing Concurrent Data Structures with Processing-In-Memory

Career Workshop for Women and Minorities in Computer Architecture (at MICRO 2017)

SERVICES

2019	Student Volunteer for ASPLOS 2019
2017	Organizer for Brown CS New Graduate Student Orientation
2014-2015	Volunteer Writer for techNeedle (Korean online media for tech-related news)
2012-2013	Treasurer for Rice IEEE Student Chapter