National University of Computer and Emerging Sciences

FAST School of Computing Spring 2020 Islamabad Campus

EE-227: Digital Logic Design

Remote Final Exam

Attempt Time: 3 Hours
Submission (on LMS and through email) Time: 15 minutes

Wednesday, 24th June, 2020

Total Marks: 125

Course Instructor(s)

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Shams Farooq & Saad Salman.

Instructions:

1. Use A4 size blank white sheets to attempt the exam and use portrait format (unless a diagram or table requires landscape).
2. Each sheet of the A4 size paper MUST have the **Roll Number, Name, Course Code, Name of the Course, and Signature** of the student at the top of EACH sheet.
3. The answers MUST be in the same order as questions and MUST be attempted neatly. Each answer MUST start from a new page.
4. You can scan your solved solution using cam-scanner, MS lens applications, you should carry a clean scanning, free from any marks/stains etc.
5. The scanned copy MUST be **submitted** on both **google classroom** and via **email**. **NOTE:** Please do not compose a new email, you MUST reply to your instructor on the same email thread on which you received the exam.
   NOTE: Classroom submission should be made on your **section's classroom** only**.**
6. You are expected to submit a single PDF file. No other formats will be accepted. The name of the file should be CourseCode-RollNo-Section (e.g EE227-i190123-B).
7. Use permanent ink pens only.
8. **NO marks** for Direct Answers. You must show all the intermediary steps to score credit.
9. NO late submission shall be entertained.
10. Failure to comply with the above instructions may lead to serious penalties.
11. Try to submit soon after 3 hours of attempt time and do not wait for 15 minutes to be elapsed.
12. For **proven cheating/ plagiarism**, student will get an **F grade** even if the student had opted for **S/U grade**, and the case will be referred to DDC (Department's Disciplinary Committee). Instructors will conduct vivas of randomly selected students or in case of doubt (significantly different attempt as compared to past performance in the course or matching attempt with other students). Plagiarism includes sharing an attempt to other students (copy providing). Students who are not able to satisfactorily answer instructor's questions (based on the exam as well as slightly lateral but related concepts) during viva will also be considered as plagiarism cases.

	Q-1	Q-2	Q-3	Q-4	Q-5	Q-6	Q-7	Q-8	Q-9	Total
Marks Obtained										
Total Marks	**5**	**15**	**30**	**10**	**15**	**10**	**15**	**10**	**15**	**125**

Question 1[5 Marks]

Perform following operation using 2's complement addition where width of computer data bus is 10-bits.

$$-(98)_{10} - (127)_{10} = (\ ?\ )_2$$

Question 2 [1+3+2+6+3=15 Marks]

Consider your roll no. as 1AI-BCDE, Where A, B, C, D are the numbers in your ID, take any repetitive number in your roll number only once.

Examples: 19I-1234 $F = \prod(1,2,3,4,9)$

18I-2234 $F = \prod(1,2,3,4,8)$

19I-2345 $F = \prod(1,2,3,4,5,9)$

Convert it to a function like this: $F = \prod(1, A, B, C, D, E)$

I. Convert it in SOP form, $F = \sum(\ ?\ )$
II. Put the min-terms you get in (a) in 4-variable K-Map. List all the Prime Implicants and Essential Prime Implicants
III. Simplify the function you get in (a) using K-Map and write the result in standard form.
IV. Write the function in SOP form and simplify it to a minimum number of literals using Boolean laws.
Note: Don't forget to write the name of the law you applied in each step.
V. Draw logic diagram of the function you get in (c) using 2-level implementation of NOR gates only.

Question 3[5x6 = 30 Marks]

Perform the following. You must show all the steps to get credit.

I. $(3016)_{10} = (\ ?\ )_3$, where base 3 numbers are {0,1,2}

II. $(F01\ .\ 700)_{16}$ - $(9A\ .\ 81)_{16}$ = $(?)_{16}$ = $(?)_{10}$

III. $(110\ .\ 1001)_8$ - $(45\ .\ 6237)_8 = (?)_8$ = $(\ ?\ )_{16}$

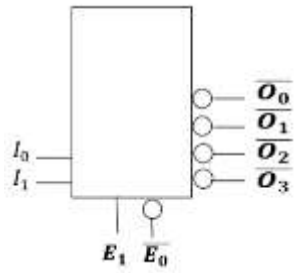
IV. Perform BCD Addition $(2\ .92)_{BCD} + (0.68)_{BCD} = (\ ?\ )_{BCD}$

V. Produce next three excess-4 codes of the Binary number $(110011)_2$

VI. $(52413)_6 + (11254)_6 = (\ ?\ )_6$, where base 6 numbers are {0,1,2,3,4,5}

Question 4[6+4 = 10 Marks]

I. Design the following **2 x 4 decoder.** Create table and produce expressions.



II. Design **4 x 16 decoder** by using above given 2x4 decoders only?

Question 5[15 Marks]

Design **4x2 Priority Encoder** where priority sequence is $D_2 < D_0 < D_3 < D_1$. Inputs are **active high** and Outputs are **active low enable?** Perform simplification & extract expressions?

INPUT				OUTPUT		
D_0	**D_1**	**D_2**	**D_3**	**$\overline{A}$**	**$\overline{B}$**	**Valid**

Question 6[10 Marks]

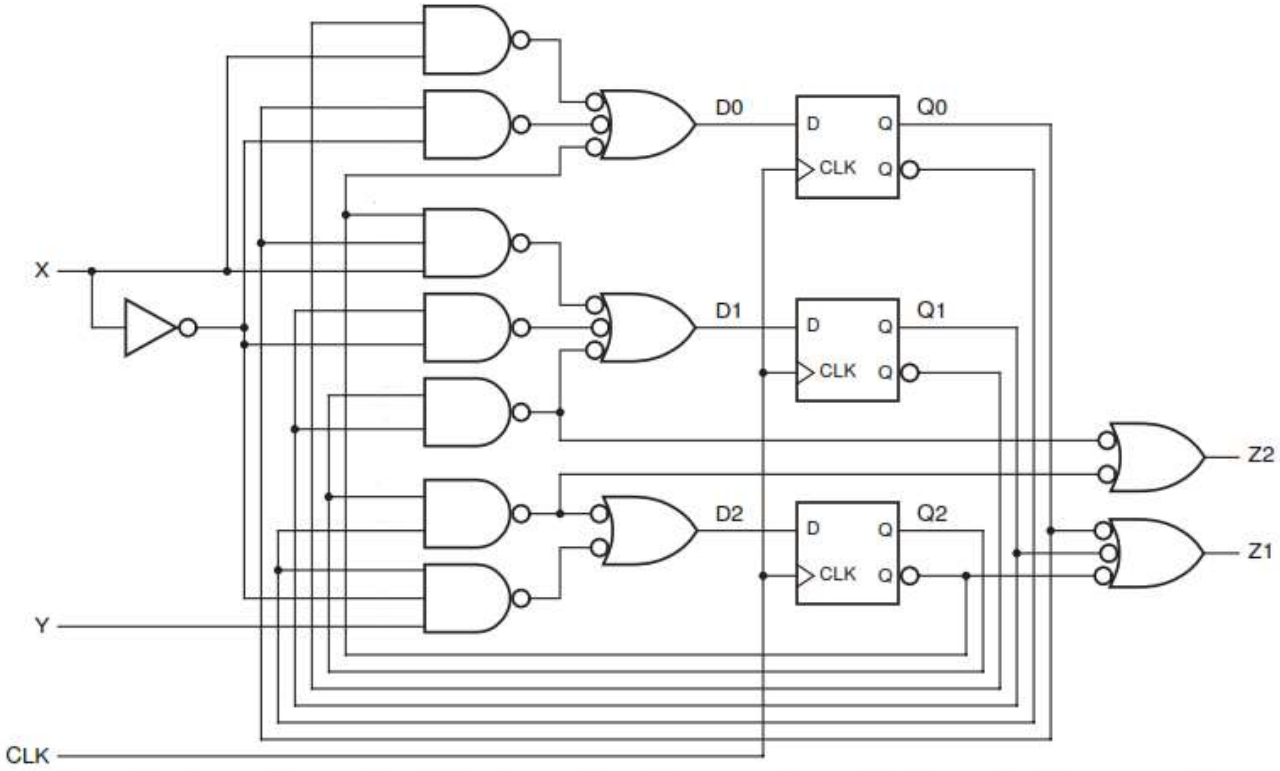
Design a combinational circuit that converts a **3-bit Binary number** to a **3-bit Gray code+1**? Extract simplified expressions using K-Maps.

HINT:

Produce Gray code for each binary number & add ONE to it, whereas Gray code +1 for binary 5 is 000.

	BINARY			GRAY CODE+1		
	A	B	C	G2	G1	G0
0	0	0	0			
1	0	0	1			
2	0	1	0			
3	0	1	1			
4	1	0	0			
5	1	0	1	0	0	0
6	1	1	0			
7	1	1	1			

Question 7[5+5+5 = 15 Marks]



A sequential circuit shown in the given figure has three D flip-flops **Do, D_1** and **D_2** , two inputs **X** and **Y**, and outputs **Z_1** and **Z_2**.

I. Derive the state equations

II. Tabulate the state table.

III. Draw the state diagram of the circuit.

Question 8[10 Marks]

Develop a synchronous **3-bit gray code up/down counter** with a gray code sequence using **'T'** flip flops. The counter should count up when control input **'M'** is 0 and count down when the control input is 1. Treat **011** and **101** as unused states. Unused states can be treated as Don't Care Terms.

Question 9[15 Marks]

Draw and label the circuit diagram of a universal shift register using four 8 x 1 multiplexers and four D flip flops. The shift register should operate according to the following table.

Mode Control			Register Operation
S2	**S1**	**S0**	
0	0	0	Reset to 0
0	0	1	Shift left
0	1	0	Set to 1
0	1	1	Complement the input
1	0	0	Shift right
1	0	1	Give 1's complement of the input
1	1	0	Parallel Load
1	1	1	Set to 1