National University of Computer and Emerging Sciences

FAST School of Computing **Fall 2019** **Islamabad Campus**

EE-227: Digital Logic & Design

Serial No:

Final Exam

Total Time: 3 Hours

Total Marks: 100

Tuesday,24 th December, 2019

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Signature of Invigilator

Course Instructors

SHAMS FAROOQ

_____ _____ _____ _____

Student Name Roll No Section Signature

DO NOT OPEN THE QUESTION BOOK OR START UNTIL INSTRUCTED.

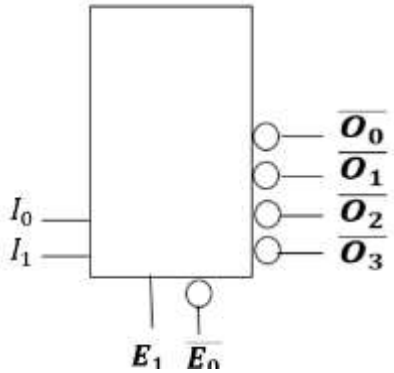
Instructions:

1. Attempt on question paper. Attempt all of them. Read the question carefully, understand the question, and then attempt it.
2. No additional sheet will be provided for rough work. Use the back of the last page for rough work.
3. If you need more space write on the back side of the paper and clearly mark question and part number etc.
4. After asked to commence the exam, please verify that you have twenty (20) different printed pages including this title page. There are a total of 8 questions.
5. Calculator sharing is strictly prohibited.
6. Use permanent ink pens only. Any part done using soft pencil will not be marked and cannot be claimed for rechecking.

	Q-1	Q-2	Q-3	Q-4	Q-5	Q-6	Q-7	Q-8	Total
Marks Obtained									
Total Marks	**10**	**10**	**10**	**15**	**15**	**15**	**10**	**15**	**100**

Question 1 [5+5 Marks]

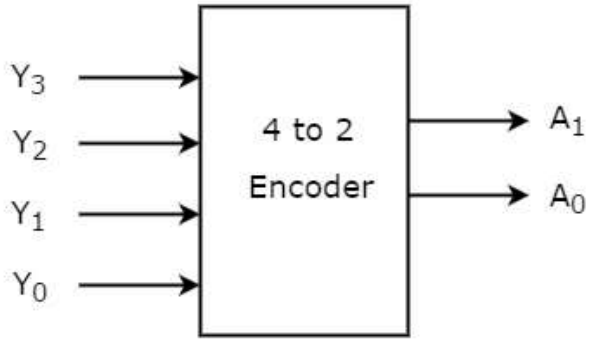
*a. Design **2x4 Decoder** using following block diagram?*



TRUTH TABLE

EXPRESSIONS

b. *Design* ***2x4 High Priority Encoder?*** *Where Y3 has more priority over Y2*

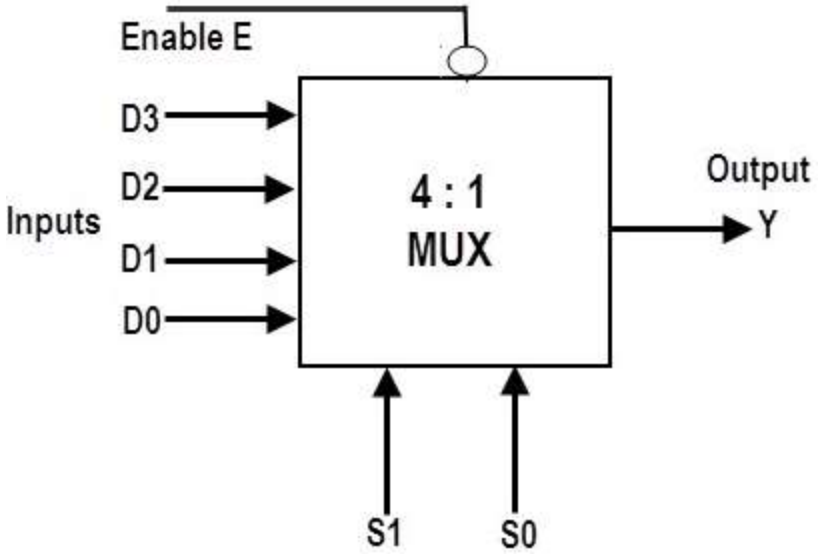


TRUTH TABLE

EXPRESSIONS

Question 2 [5+3+2 Marks]

a. *Design **4x1 Multiplexer?***

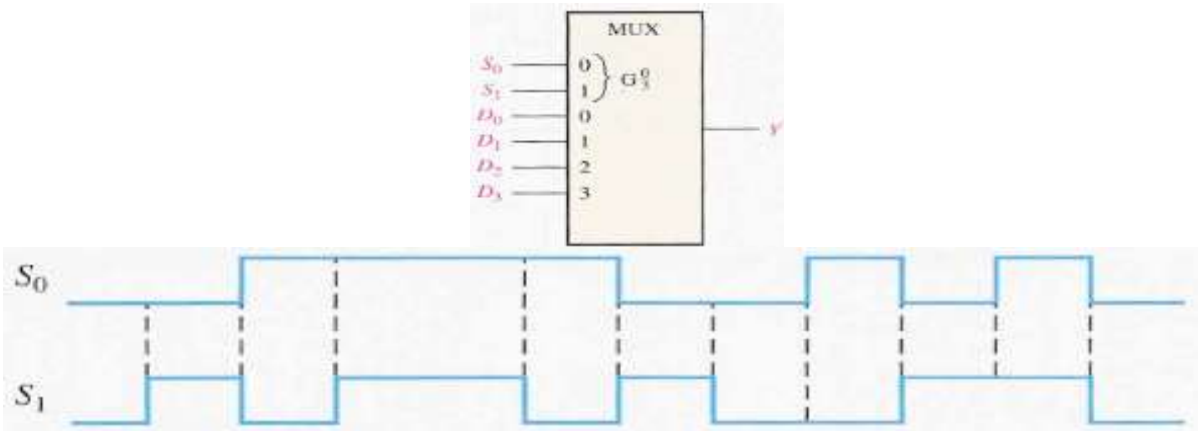


TRUTH TABLE

EXPRESSIONS

*b. Use block diagram given above to create **8x1 Multiplexer?***

*c. For the multiplexer given below, determine output **Y** (Timing Diagram) with **data select inputs S_0 and S_1** to the multiplexer are sequenced as shown in waveform given below, where **D_0 =0, D_1 =1, D_2 =1, D_3=0.***



Y

Question 3 [5+5 Marks]

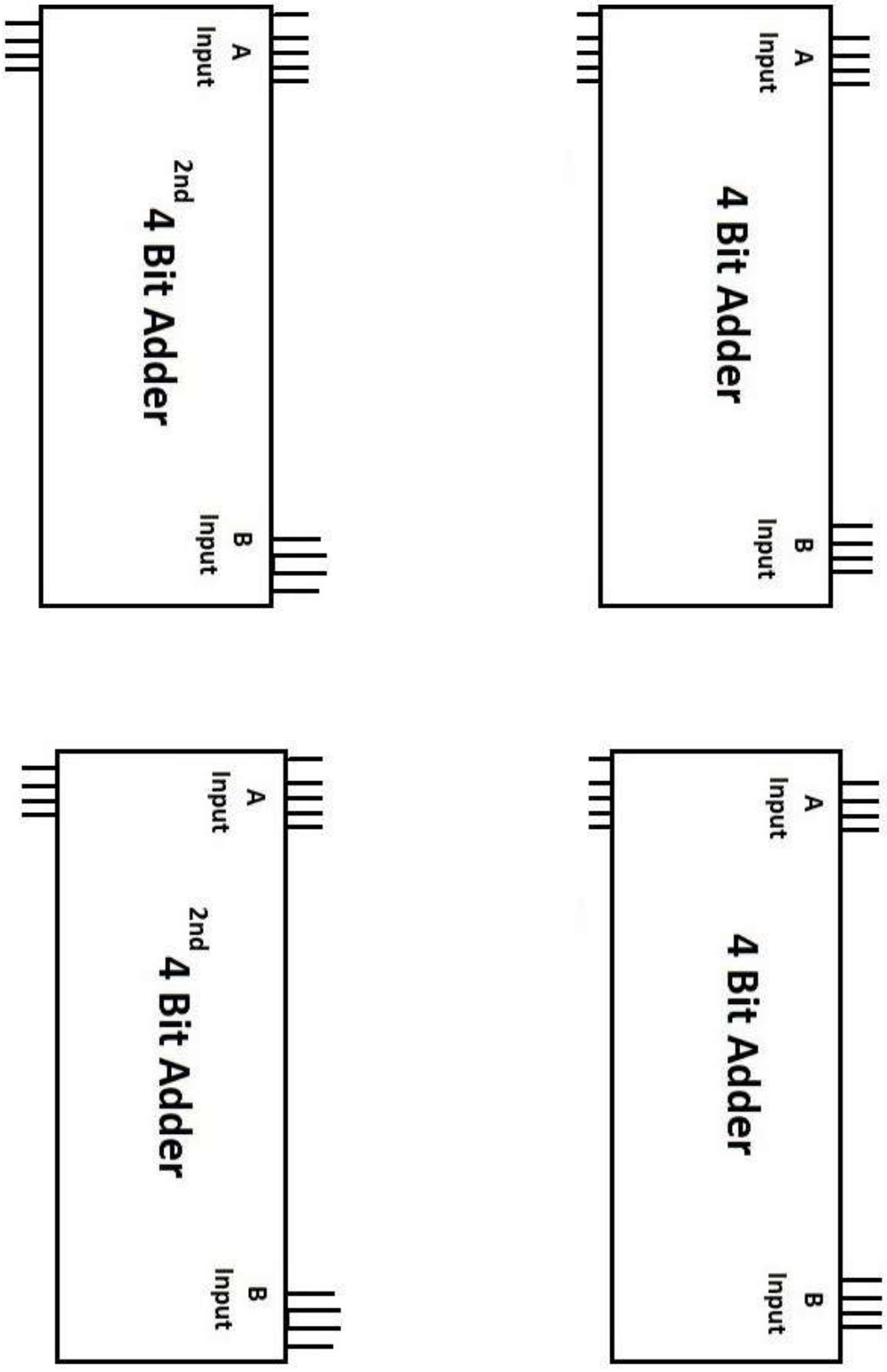
a. *Design Invalid* ***BCD Detector circuit****?*

TRUTH TABLE

SIMPLIFICATION

EXPRESSION

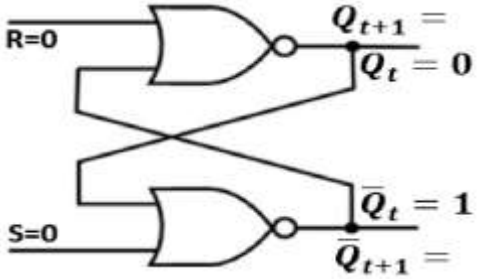
b. *Modify Circuit given below by adding INVALID DECTECTOR Circuit designed above so circuit is able to add BCD number* ***$(96)_{bcd}+(85)_{BCD}$***

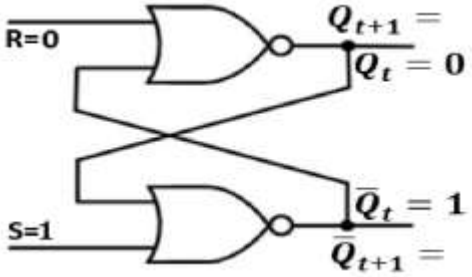


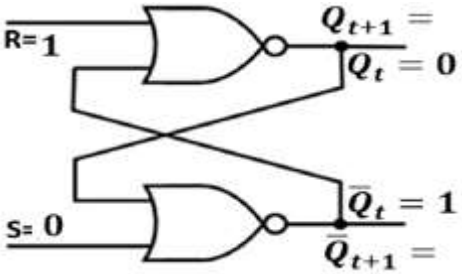
Question 4 [6 +6+ 3 Marks]

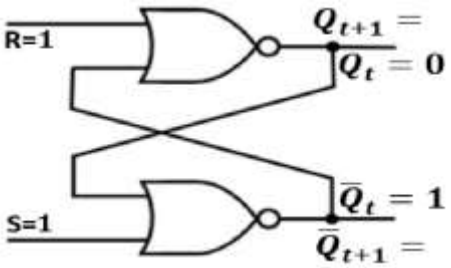
a. Process each state given below to find values of $\mathbf{Q_{t+1}}$ and $\overline{Q}_{t+1}$? Fill the results in a table?

CASE I

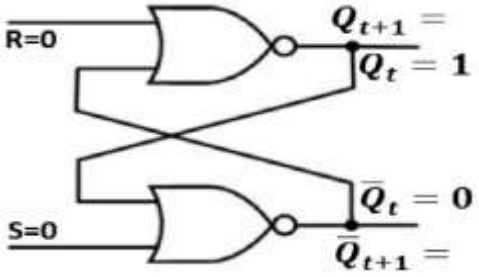


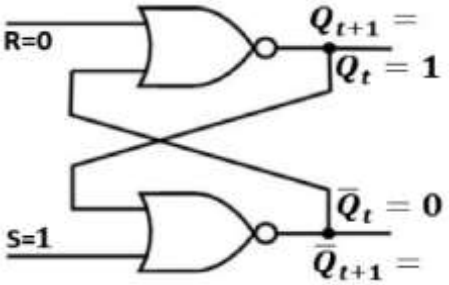


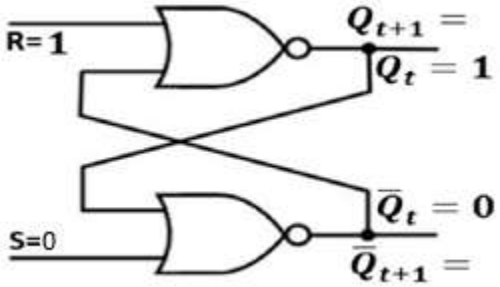


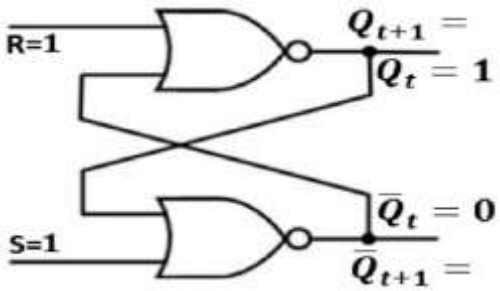


CASE II

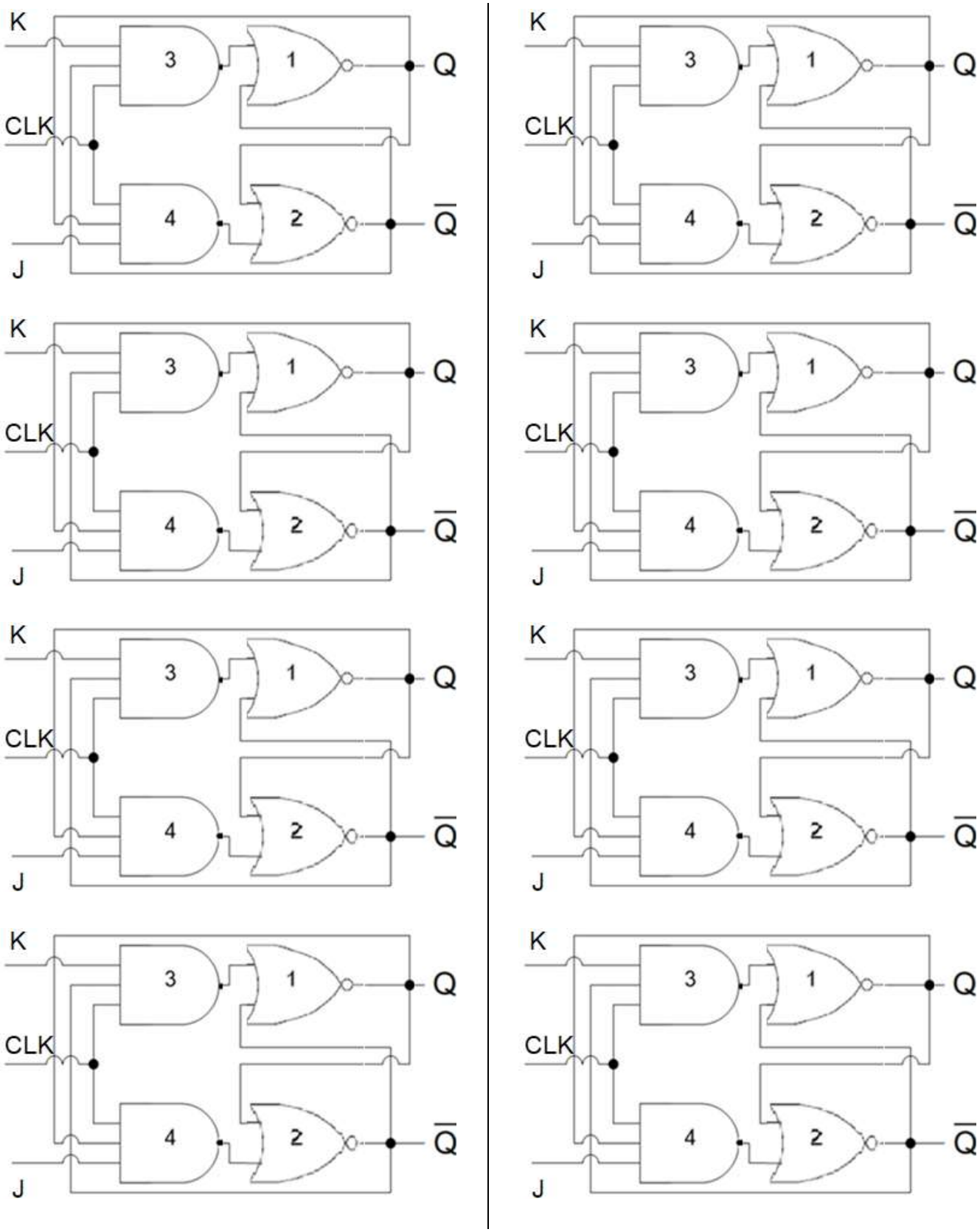






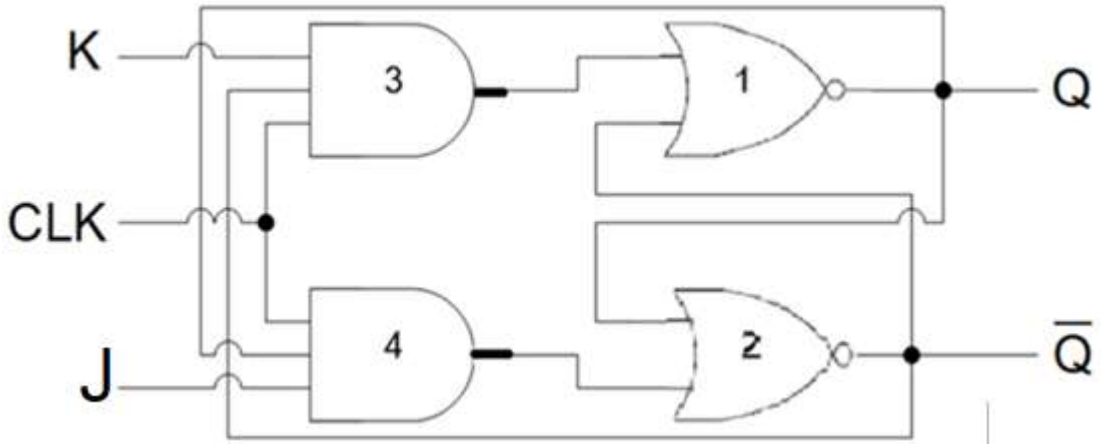


b. *Process the following circuit and produce table.*



CLK	*J*	*K*	Q_{t+1}	$\overline{Q_{t+1}}$

c. *Modify given circuit to introduce Asynchronous **CLEAR** and **SET** inputs fill table*



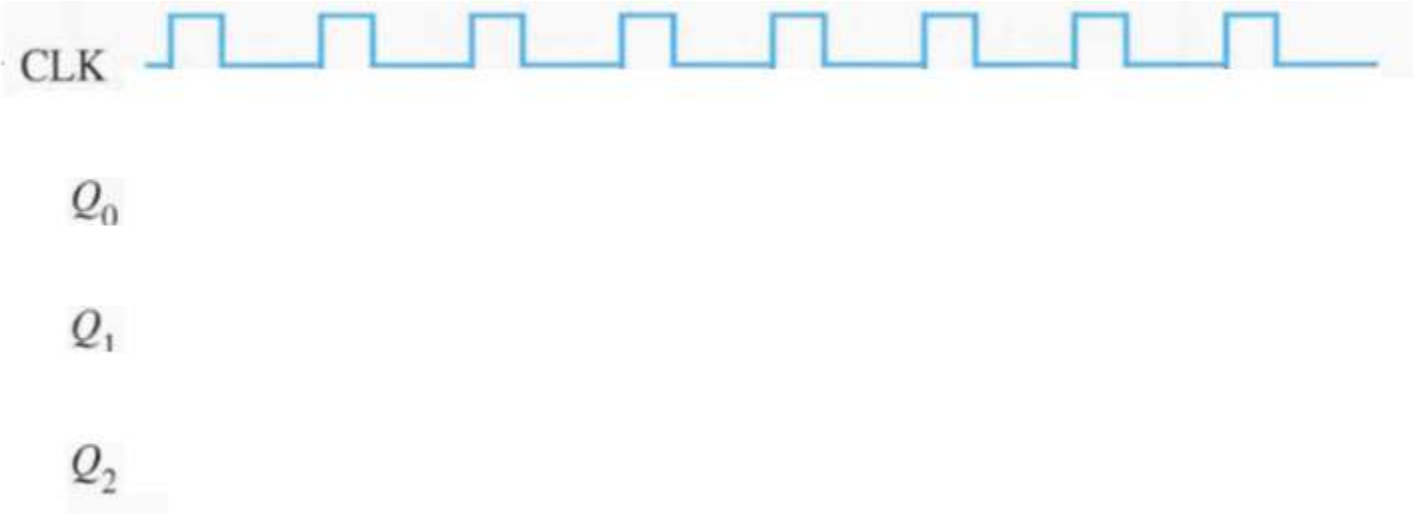
SET	CLEAR	Q_{t+1}	$\overline{Q}_{t+1}$
0	0		
0	1		
1	0		
1	1		

Question 5 [5+4+ 3+3 Marks]

a. *Design **3-Bit Asynchronous Down counter** using Positive edge triggered **T flip-flop**.*

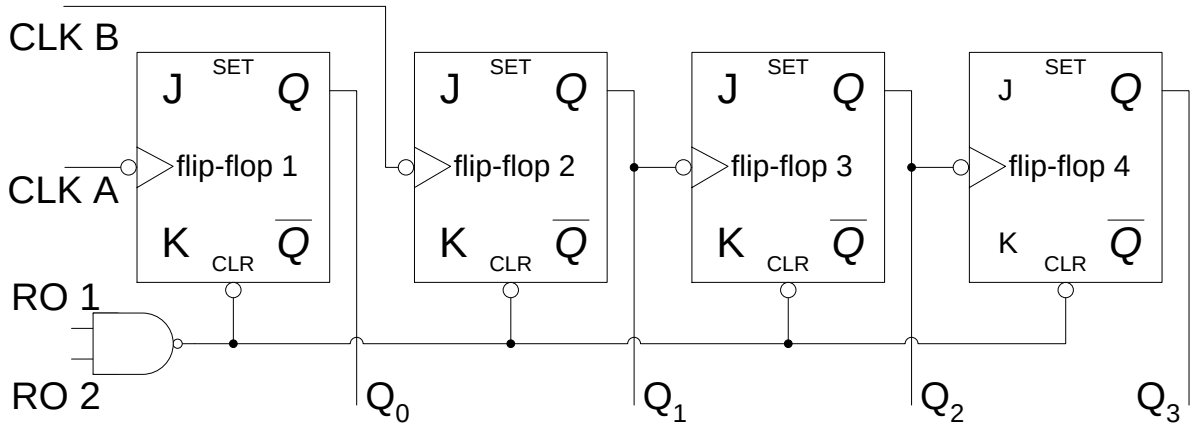
b. *Convert the above designed 3-bit Asynchronous Down Counter to **Mod-5 Down Counter**?*

c. *Draw Timing Diagram for **MOD-5 DOWN COUNTER.***



*d. Following is a **74LS93** is a 4-bit Asynchronous Counter logic diagram? Convert it to **Decade Counter**?*

***NOTE:** You are not supposed to use any additional gates*



Question 6 [4+3+4+4= 15 Marks]

	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

a. *For the Following state table. Draw the corresponding state diagram*

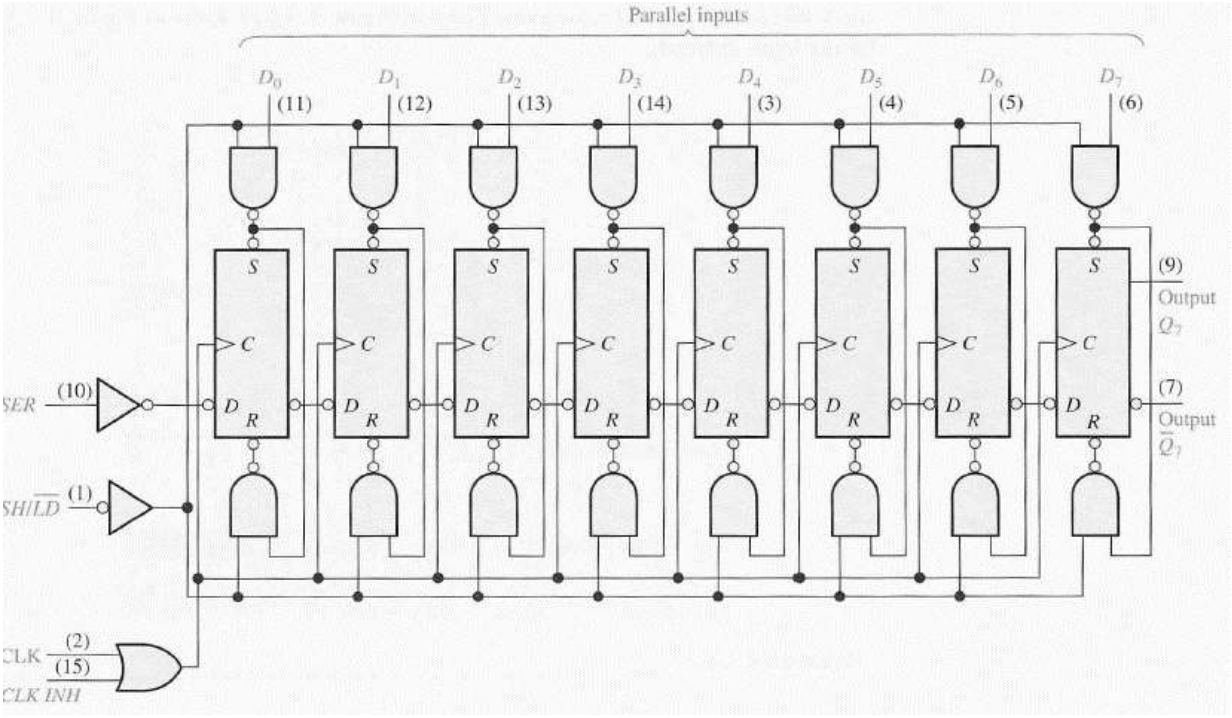
b. *Tabulate the reduce table*

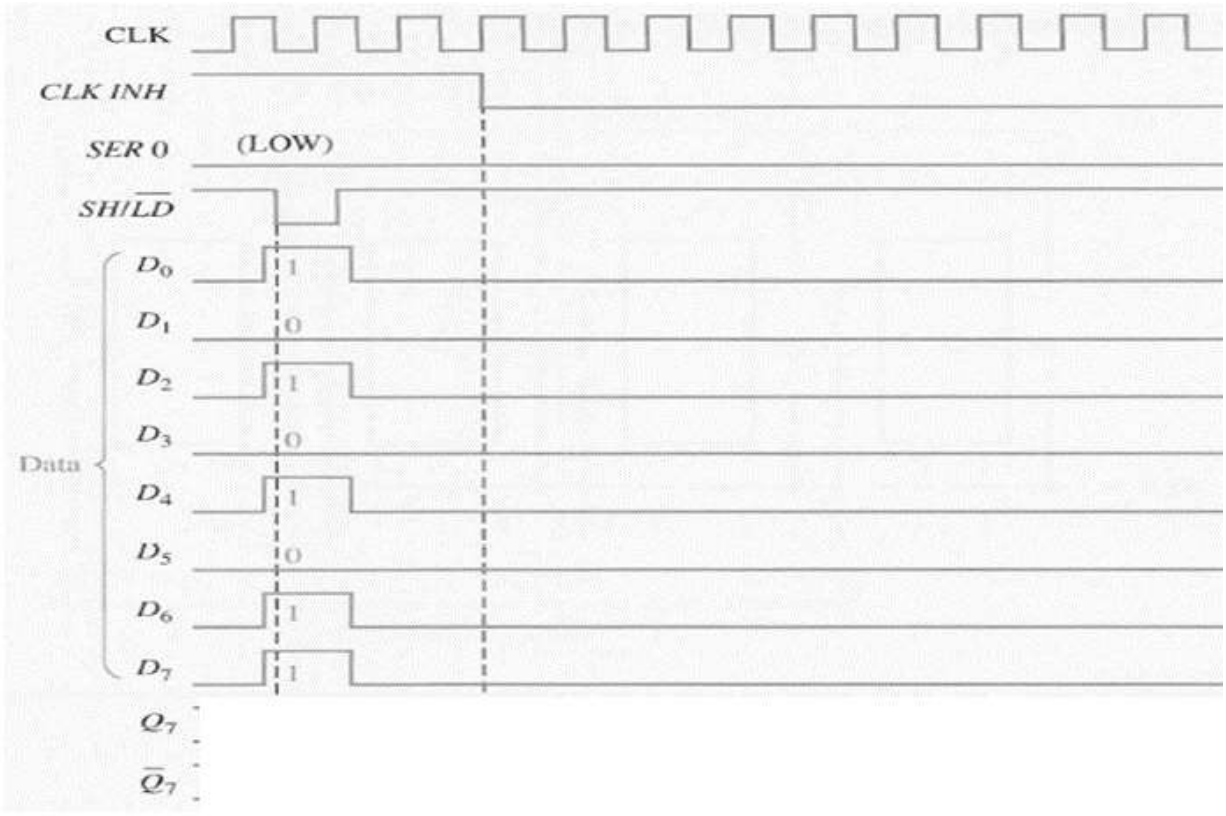
c. Draw the state diagram corresponding to the reduce state table

d. Starting from A and the input sequence **01110010011**, Determine output sequence for actual and reduce state diagram

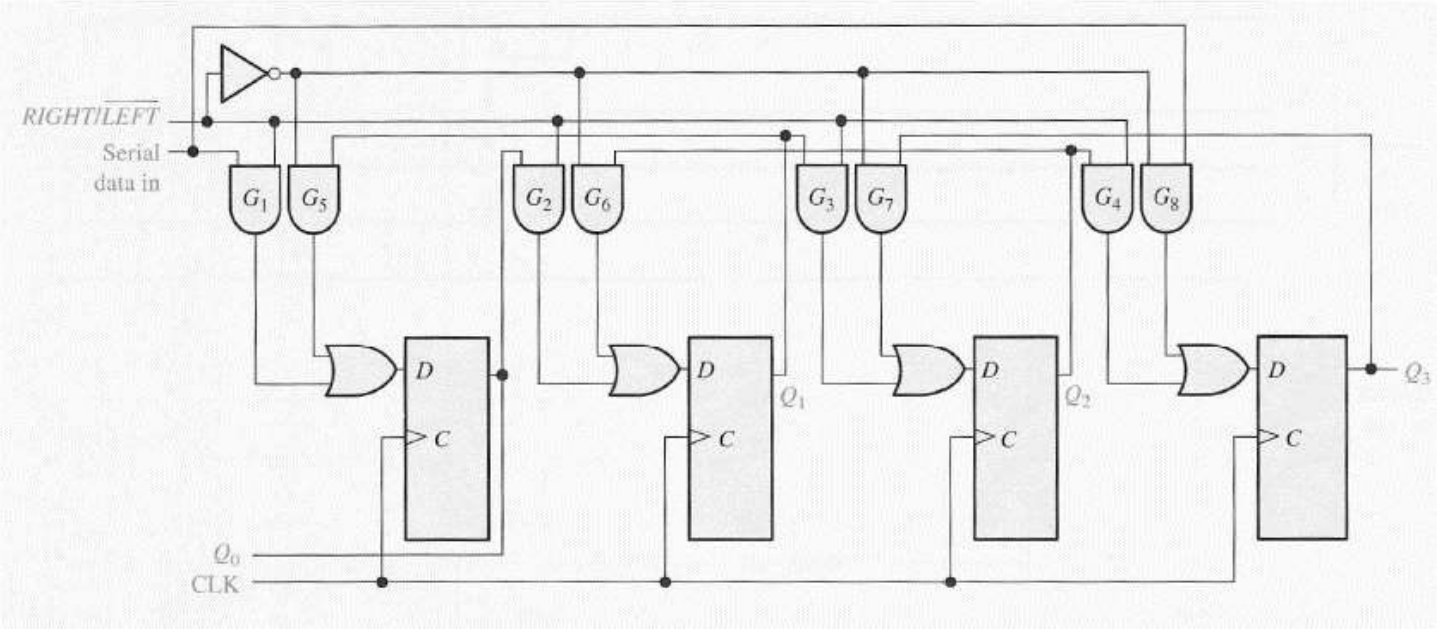
Question 7 [5+5]

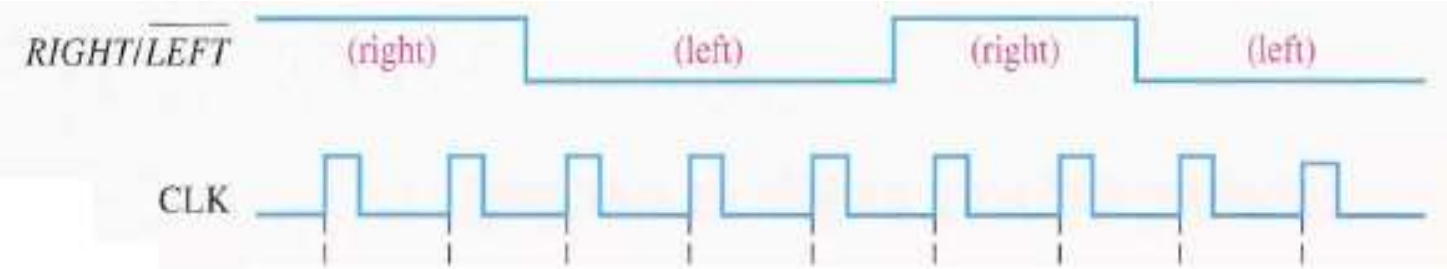
a. Name the following circuit? Complete Timing Diagram fill Q_7 .





b. *Name the following circuit? Complete Timing Diagram assume* ***Q_0=1, Q_1=1, Q_2=0*** *and* ***Q_3=1*** *and that* ***serial Data input*** *line is* ***LOW***





Q_0

Q_1

Q_2

Q_3

Question 8 [15 Marks]

*Design **UP/DOWN Counter** using **JK Flip-Flop** to produce following sequence **1,4,3,5,7,6,2…** when x=0 counter Counts and for x=1 counter count down? Draw State diagram, State Transition table, K-map, Extract expression where least significant flip-flop is named A with J_A and K_A inputs Output is Q_A*

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