



Parallel Architectures

(CS 3006)

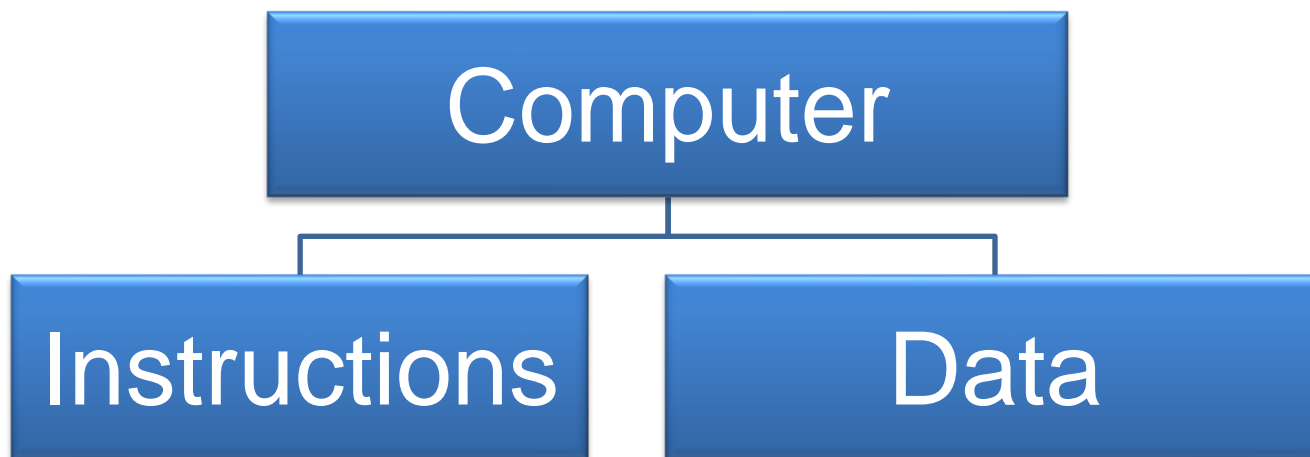
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Islamabad Campus



Flynn's Taxonomy

- Specific **classification** of **parallel architecture**
- By **Michael Flynn** (from Stanford, in 1966)
 - Made a **classification** of **computer systems** known as **Flynn's Taxonomy**





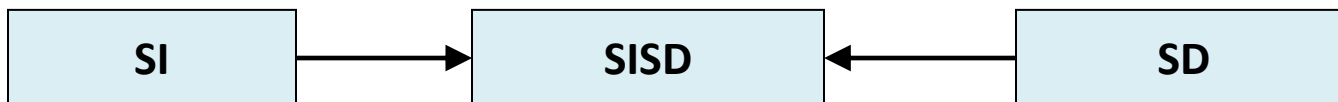
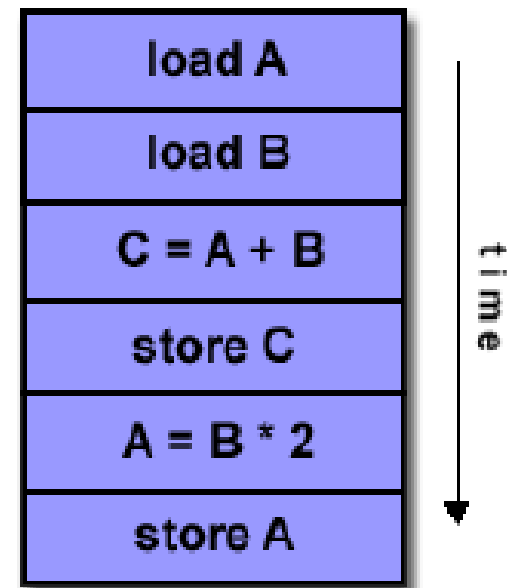
Flynn's Taxonomy

		Instruction Streams	
		one	many
Data Streams	one	SISD traditional von Neumann single CPU computer	MISD May be pipelined Computers
	many	SIMD Vector processors fine grained data Parallel computers	MIMD Multi computers Multiprocessors



1. Single Instruction, Single Data Stream – SISD

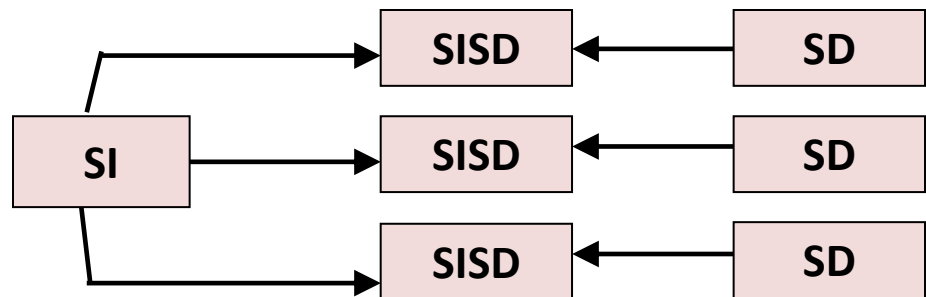
- Single processor
- Single instruction stream
- Data stored in single memory
- Deterministic execution





2. Single Instruction, Multiple Data Stream - *SIMD*

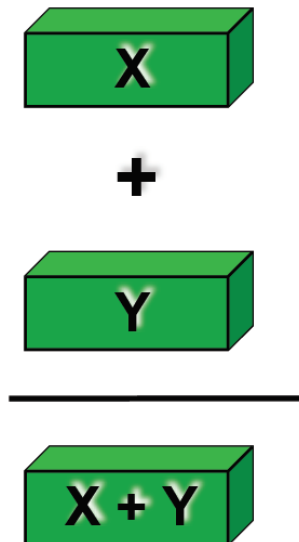
- A **parallel processor**
- **Single instruction**: all **processing units** execute same instruction at **any given clock cycle**
- **Multiple data**: Each **processing unit** can **operate on** a **different data element**
- **Large number** of **processing elements** (with local memory)
- Examples: GPUs, etc.



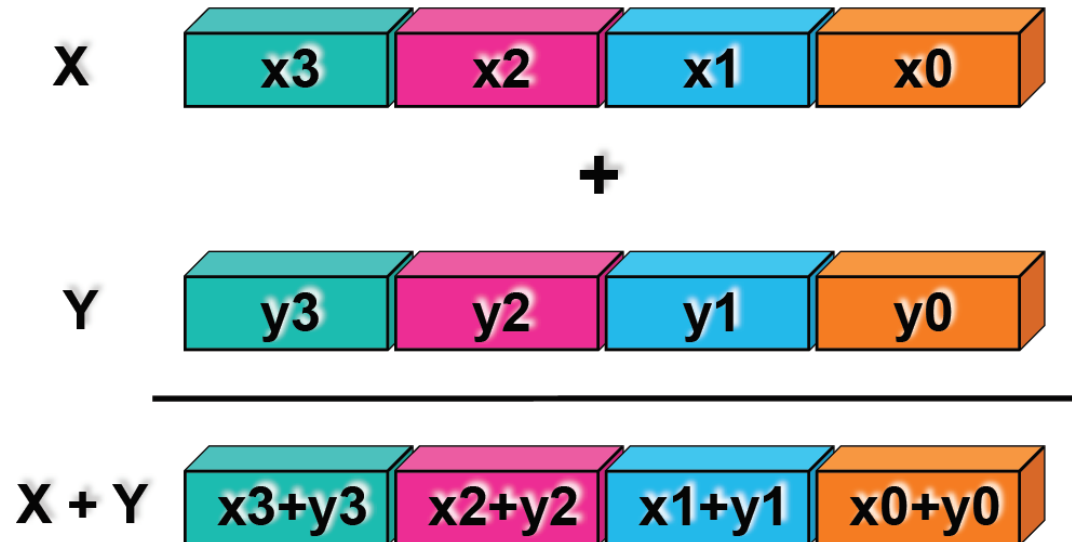


2. Single Instruction, Multiple Data Stream - *SIMD*

- **Scalar processing**
—one operation produces one result



- **SIMD vector units**
—one operation produces multiple results



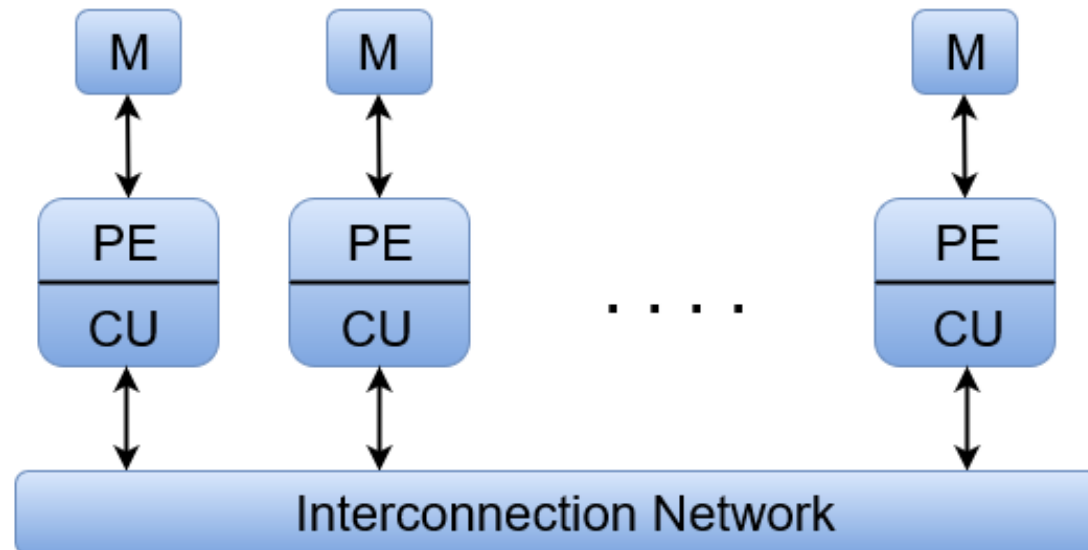


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- The diagram illustrates a multi-processor system architecture. On the left, an **Instruction Stream** feeds into a vertical column of processing units. Each unit consists of three blue rounded rectangular blocks: **M** (Memory), **CU** (Control Unit), and **P** (Processor), connected sequentially by horizontal arrows. Vertical ellipses between the units indicate multiple parallel processors. On the right, a **Memory** block is connected to the **P** blocks of all processors. A **Data Stream** is shown as a vertical arrow pointing upwards from the processors to the Memory block. A feedback loop connects the top **P** block back to the top **M** block of the first processor.



4. Multiple Instruction, Multiple Data Stream- *MIMD*

- Most common **parallel** processor architecture
- **Simultaneously** execute different instructions
- Using **different** sets of **data**
- Examples: *Multi-cores, SMPs, Clusters, Grid, Cloud*



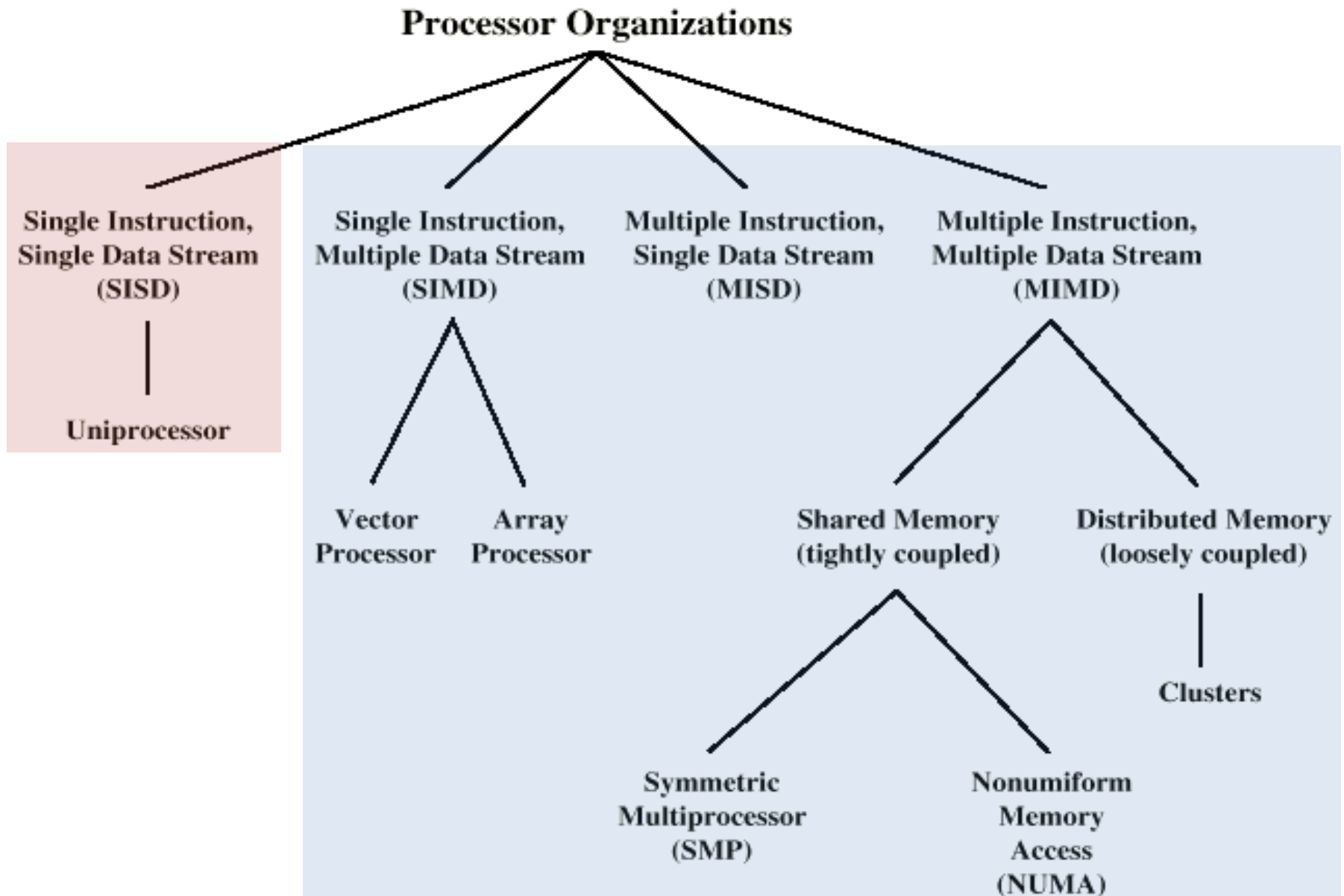


MIMD - Overview

- **General purpose** processors
- **Each** can **process** all **instructions** necessary
- Further *classified by method of processor communication*:
 1. **Shared Memory**
 2. **Distributed Memory**



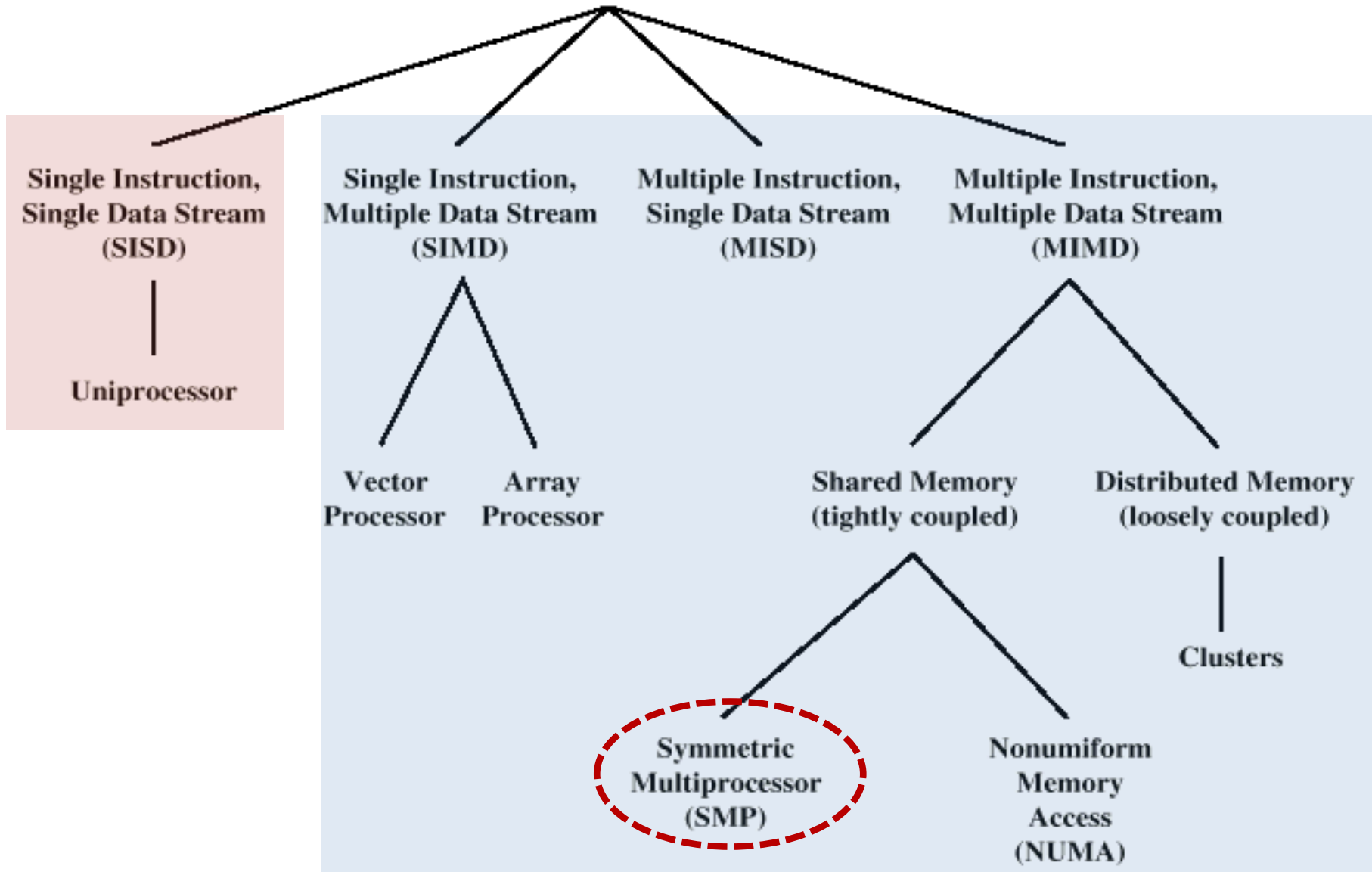
Taxonomy of Processor Architectures





Taxonomy of Processor Architectures

Processor Organizations





Symmetric Multiprocessor (SMP)

- Processors **share memory** (tightly coupled)
- **Communicate** via **shared memory** (single bus)
- **Same memory access time** (any memory region, from any processor)
- Processors **share I/O address space** too

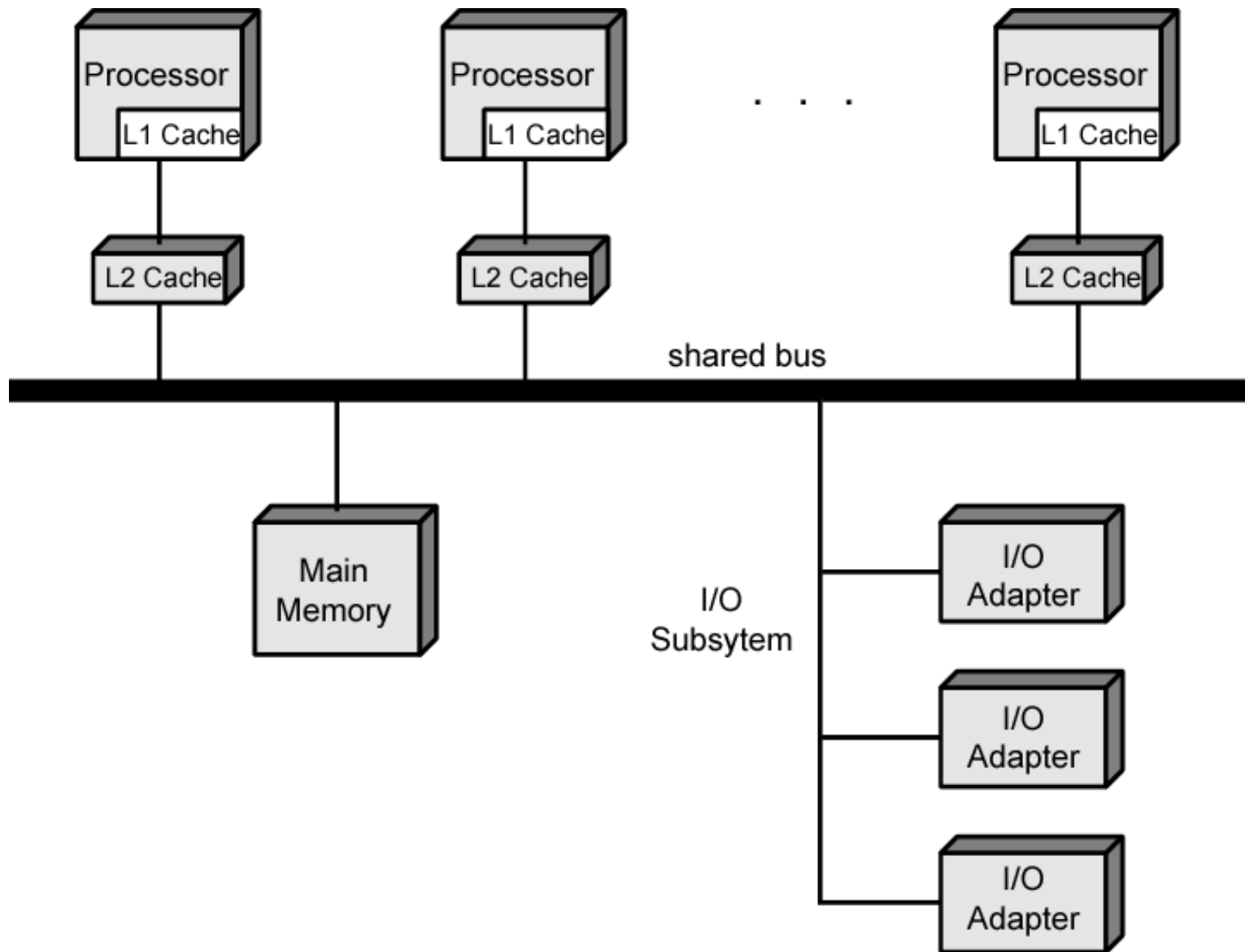


SMP Advantages

- **Performance**
 - **work** can be **done** in **parallel**
- **Availability**
 - **Failure** of a **single processor** **does not halt system**
- **Incremental growth**
 - **Adding** additional **processors** **enhances performance**
- **Scaling**
 - **Range of products** based on **number of processors**



Symmetric Multiprocessor Organization





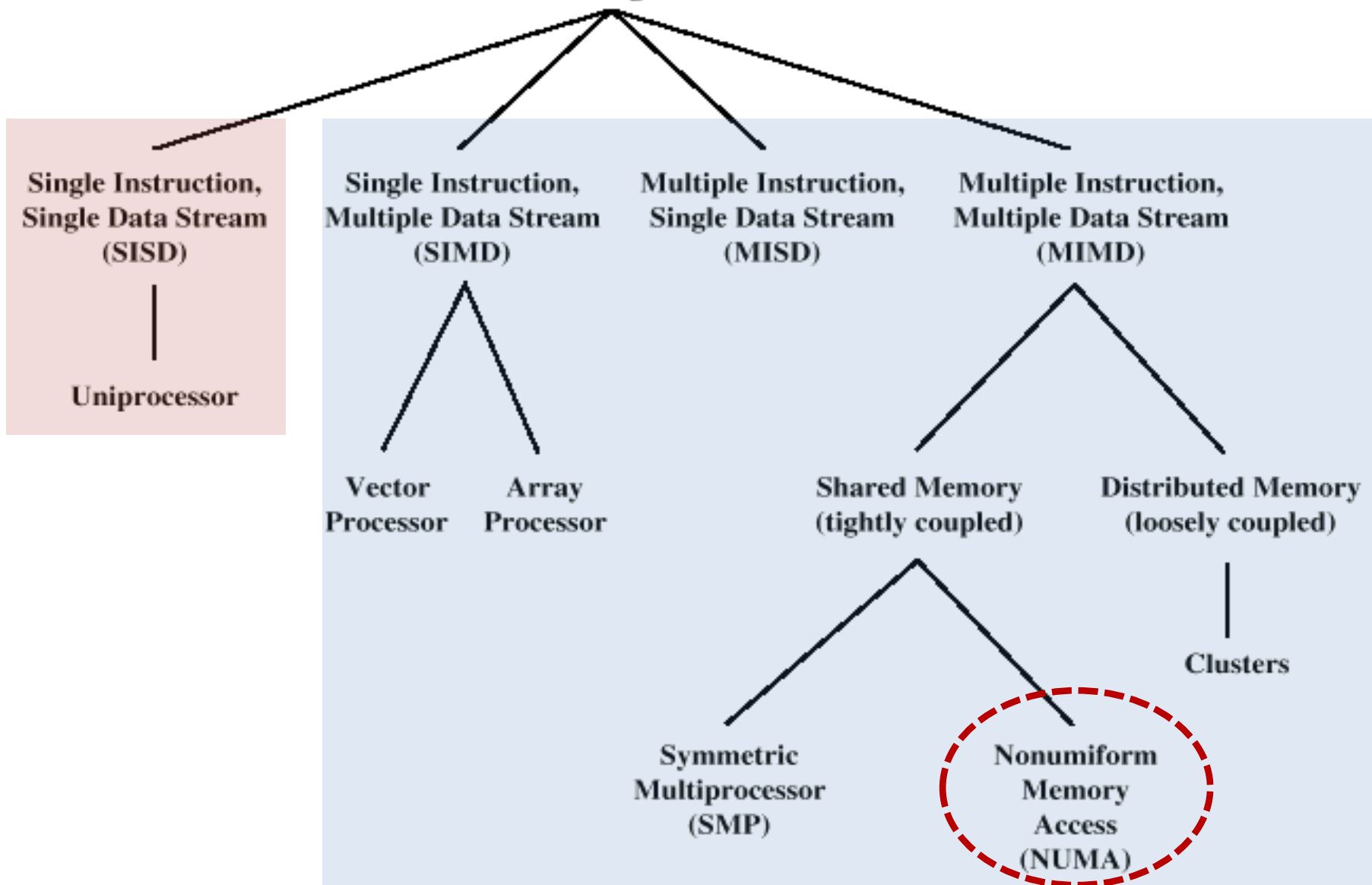
Multithreading and Chip Multiprocessors

- Instruction stream divided into smaller streams called “threads”
- Executed in parallel



Taxonomy of Processor Architectures

Processor Organizations



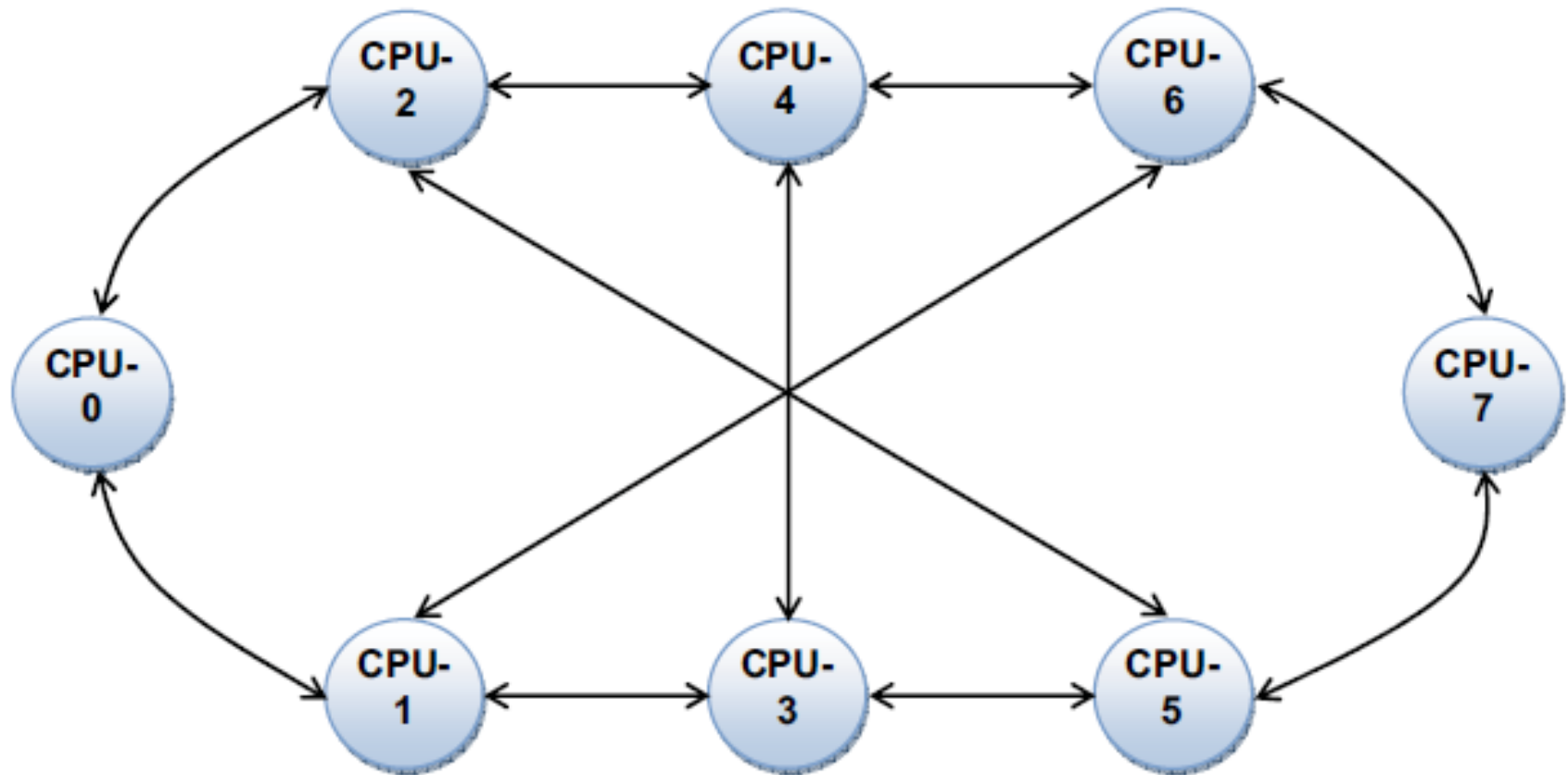


Tightly Coupled - NUMA

- **Non-Uniform Memory Access (NUMA)**
 - Access times to different regions of memory differs



SunFire X4600M2 NUMA machine





Non-uniform Memory Access (NUMA)

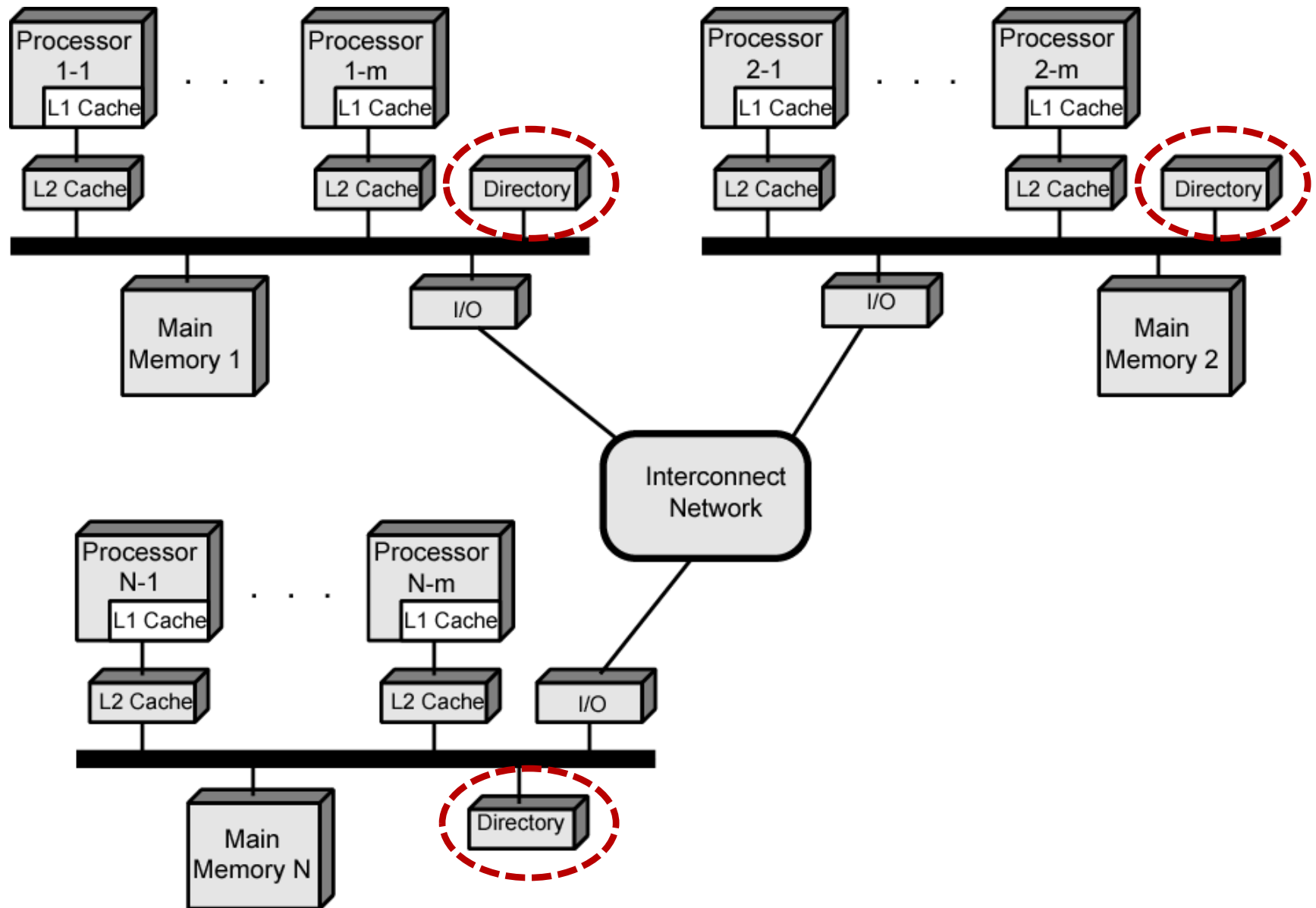
- **Non-uniform memory access**
 - All processors have access to all parts of memory
 - **Access time** of processor **differs** depending on **memory region**
 - **Different processors** access **different regions** of memory at **different speeds**
- **Cache-coherent NUMA (cc-NUMA)**
 - Cache coherence is **maintained** among the **caches** of the **various processors**



Motivation (Why NUMA)

- **SMP** has **practical limit** to **number** of **processors**
 - Bus traffic limits to between 16 and 64 processors
- In **clusters** each **node** has **own memory**:
 - **Apps do not see large global memory**
 - **Coherence maintained by software not hardware**
- **NUMA** retains **SMP flavour** while giving **large scale multiprocessing**

CC-NUMA Organization





CC-NUMA Operation

- Each processor has own L1 and L2 cache
- Each node has own main memory
- Nodes connected by some networking facility
- Each processor sees single addressable memory
- Hardware support for read/write to non-local memories, *cache coherency*
- **Memory request order:**
 1. L1 cache → L2 cache (local to processor)
 2. Main memory (local to node)
 3. Remote memory



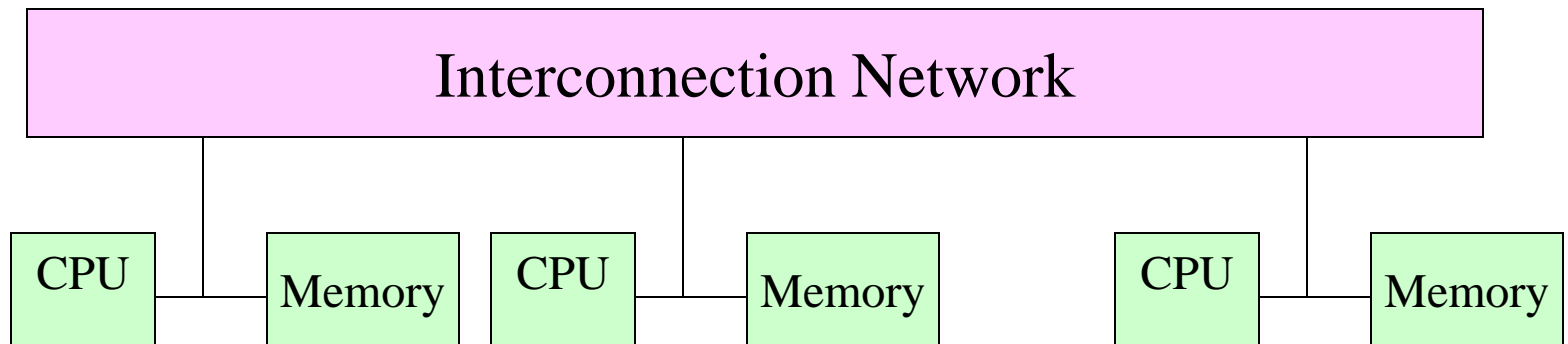
NUMA Pros & Cons

- **Effective performance at higher levels of parallelism than SMP**
- **No major software changes**
- **Performance can breakdown if too much access to remote memory**



Distributed Memory / Message Passing

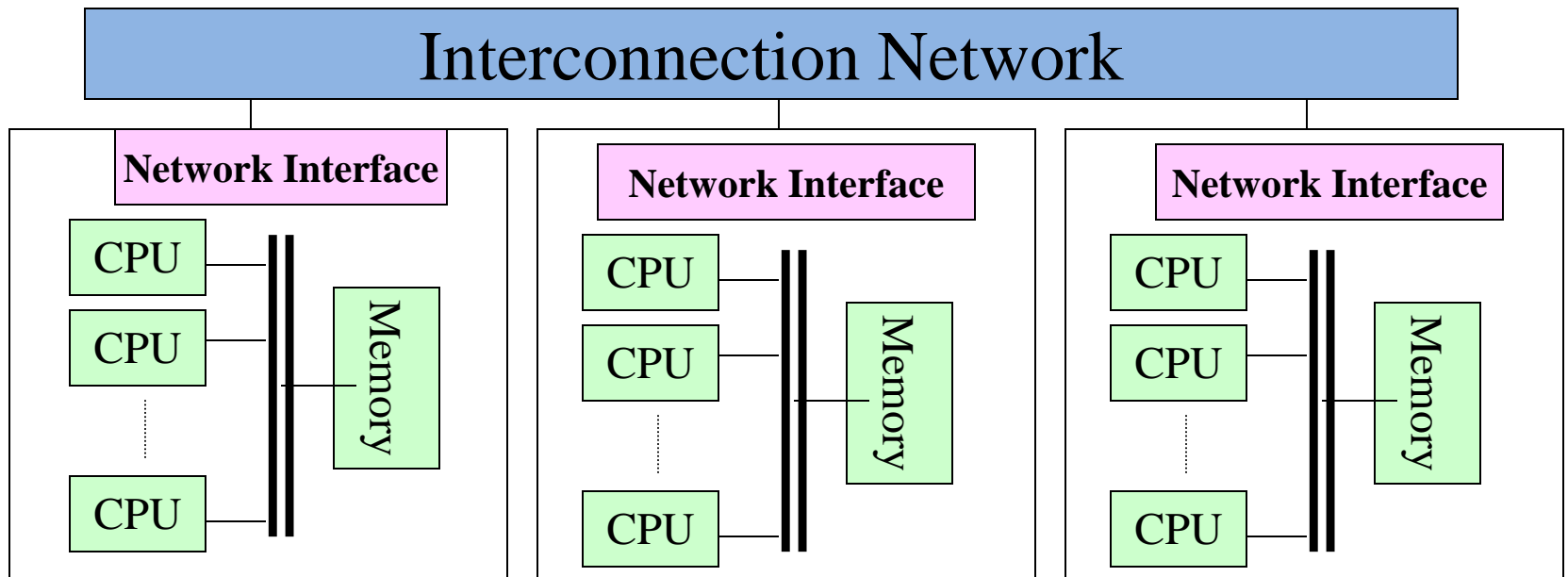
- Each **processor** has **access** to its **own memory only**
- **Data transfer** between **processors** is **explicit** (via message passing functions): **E.g., MPI library**
- User has **complete control/responsibility** for **data placement and management**





Hybrid Systems

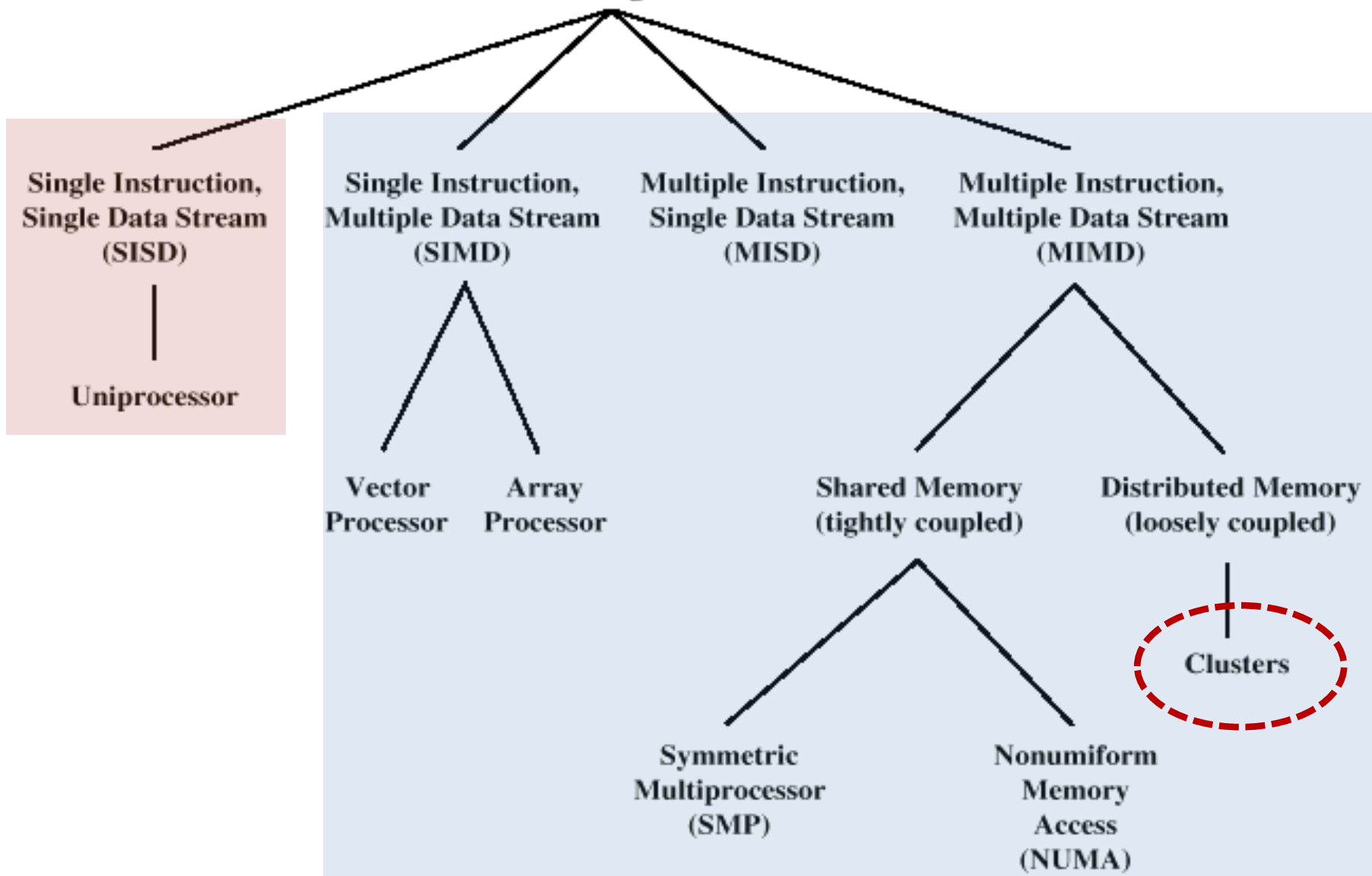
- **Distributed memory system** with **multiprocessor** **shared memory nodes**
- **Most common parallel architecture**





Taxonomy of Processor Architectures

Processor Organizations





Distributed Computing

- Using **distributed systems** to solve large problems
- **Paradigms:**
 - **Cluster** computing
 - **Grid** computing
 - **Cloud** computing



Cluster Computing



Clusters - Loosely Coupled

- **Collection** of **independent** **uni-processor** **systems** or **SMPs**
- **Interconnected** to form a **cluster**
- **Communication via** fixed path or **network** connections
- **Not a single shared memory**



Introduction to Clusters

- Alternative to **SMP**
- **High performance**
- **High availability**
- A **group** of **interconnected** whole **computers**
- **Working together** as **unified resource**
- **Illusion** of being **one big machine**
- Each **computer** called a **node**

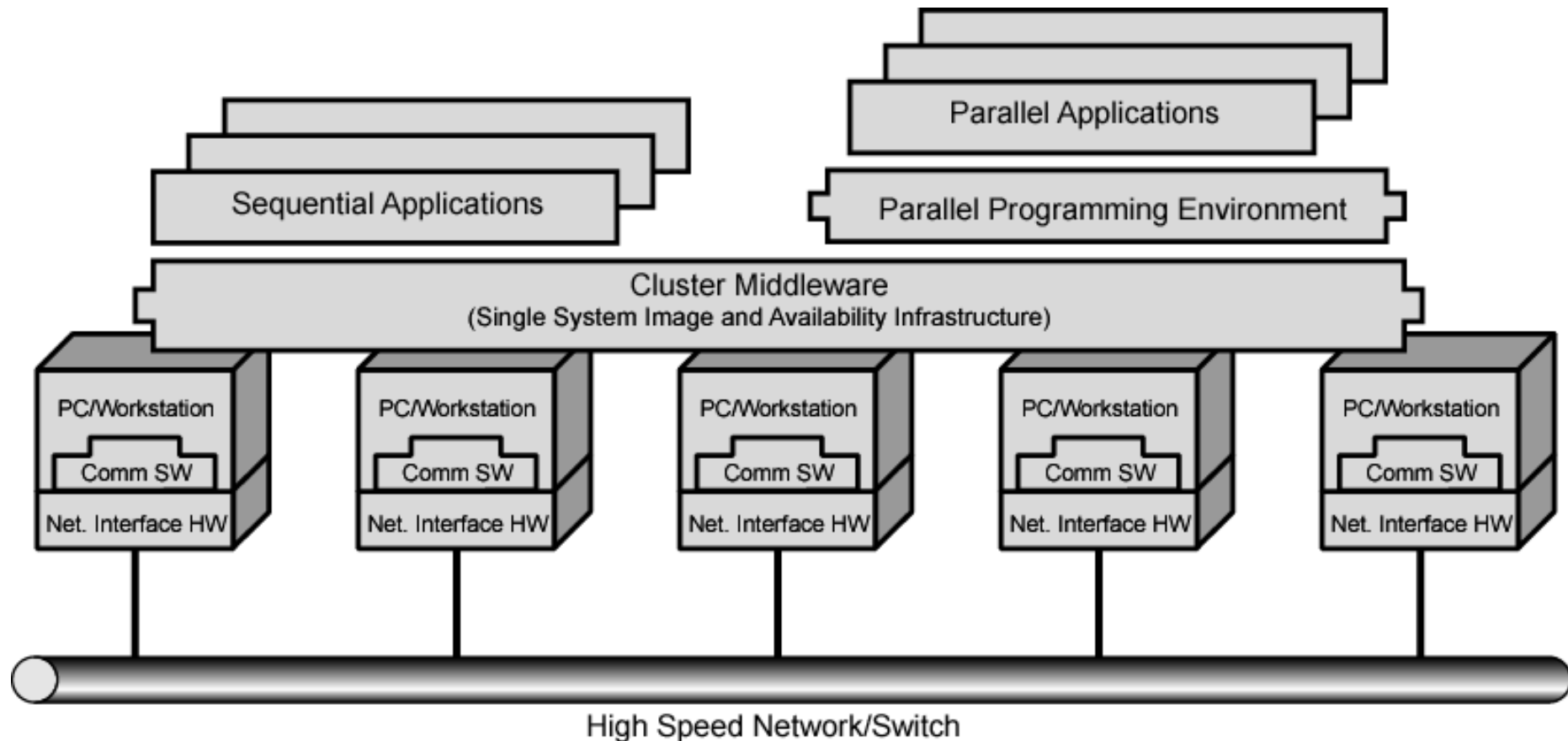


Cluster Benefits

- Scalability
- Superior price/performance ratio



Cluster System Architecture





Cluster Middleware

- **Unified image to user**
 - Single system image
- **Single point of entry**
- **Single file hierarchy**
- **Single job management system**
- **Single user interface**
- **Single I/O space**



Cluster vs. SMP

- Both provide **multiprocessor support**
- **SMPs:**
 - **Easier to manage and control**
 - **Closer to single processor systems:**
 - Scheduling is main difference
 - Less physical space required
 - Lower power consumption



Cluster vs. SMP

- **Clustering:**
 - Superior incremental scalability
 - Superior availability
 - Redundancy



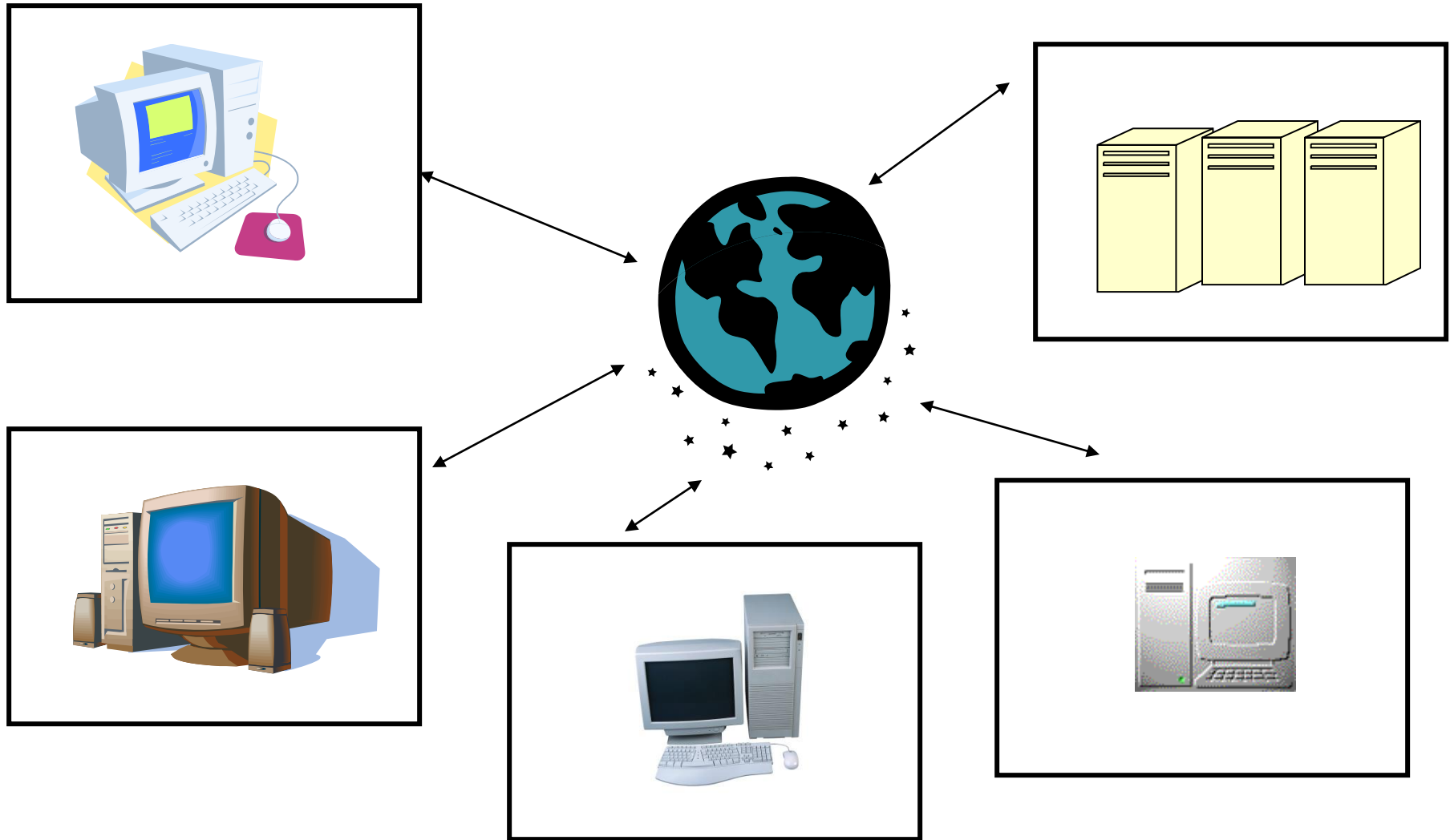
Grid Computing



Grid Computing

- **Heterogeneous computers** over the whole world providing **CPU power** and **data storage capacity**
- **Applications** can be **executed** at **several locations**
- **Geographically distributed services**
- **Coordinates/Access of resources; as contract to centralized control**
- Uses **standard, open, general-purpose protocols** and **interfaces**

Grid Architecture



Autonomous, globally distributed computers/clusters



A typical view of Grid environment

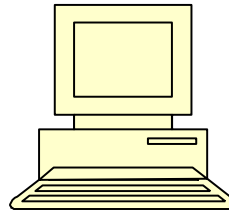
Grid Information Service

Grid Information Service system collects the details of the available Grid resources. Passes information to resource broker.

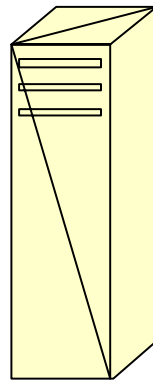


User

A **User** submit computation or data intensive application to Grids.



Details of Grid resources

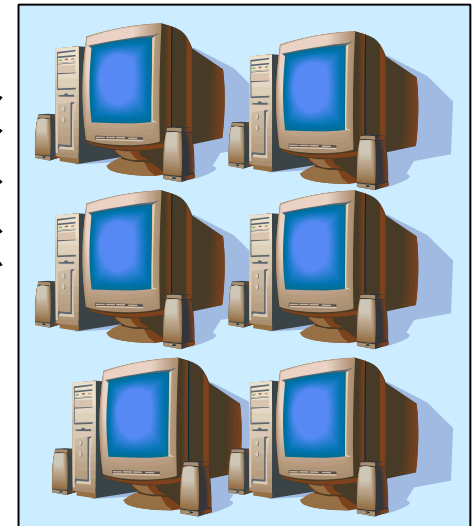


Resource Broker

A **Resource Broker** distribute the jobs in an application to the Grid resources based on user's QoS requirements and available Grid resources.

Computational jobs

Processed jobs



Grid Resources

Grid Resources (Cluster, PC, Supercomputer, database, instruments, etc.)



Cloud Computing



What is Cloud Computing?

- **Cloud Computing** is a **network-based computing** that takes place **over the Internet**:
 - a **collection/group** of **integrated** and **networked hardware, software, and Internet infrastructure** (called a **platform**).
- **Hides the complexity** and details of the **underlying infrastructure**



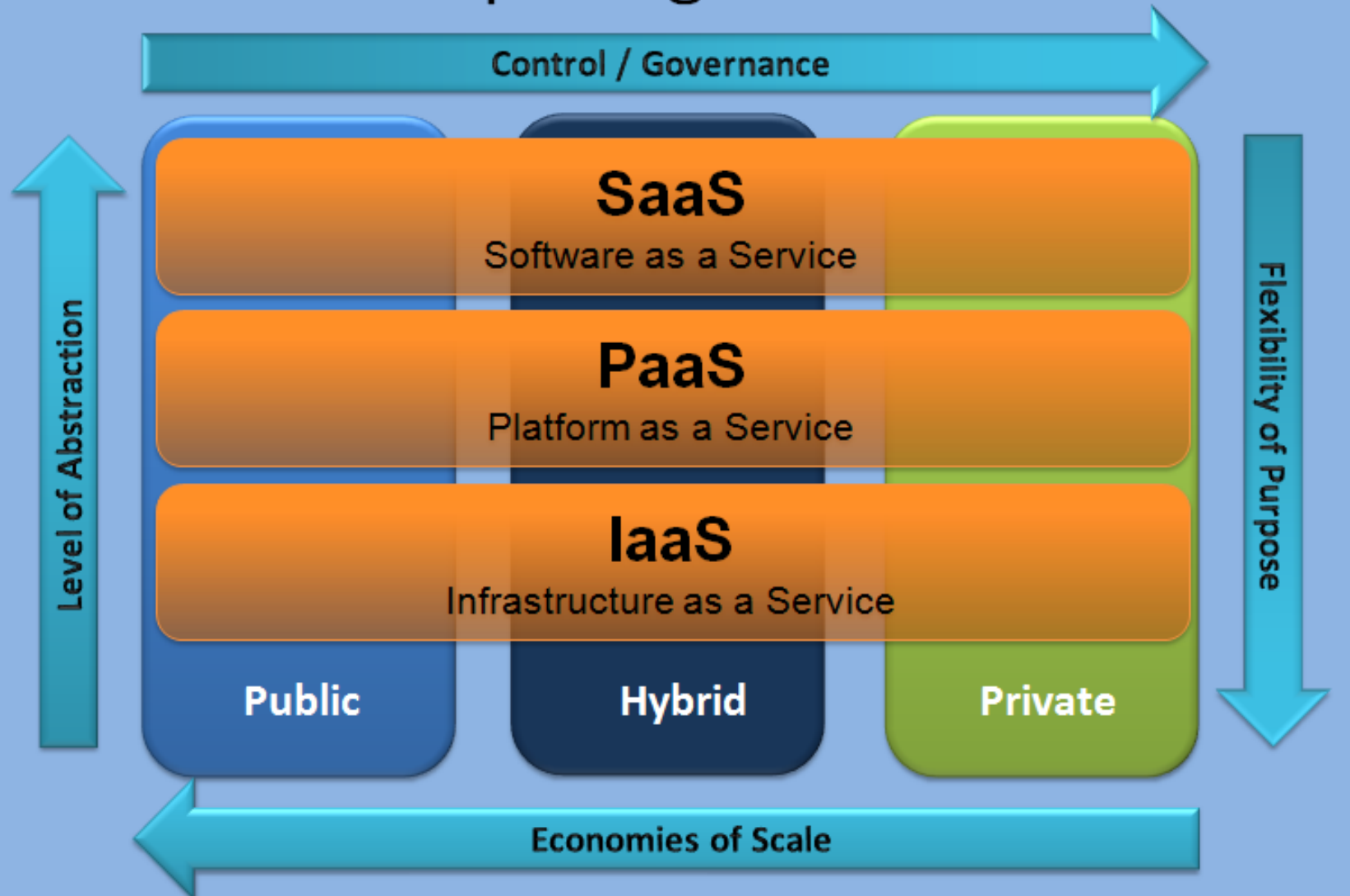
What is Cloud Computing?

- On demand services, that are **always ON**, **Anywhere**, **Anytime** and **Any place**
- Pay for use and as **needed**
- Elastic: **scale up and down (capacity and functionalities)**
- Shared pool of **configurable computing resources**



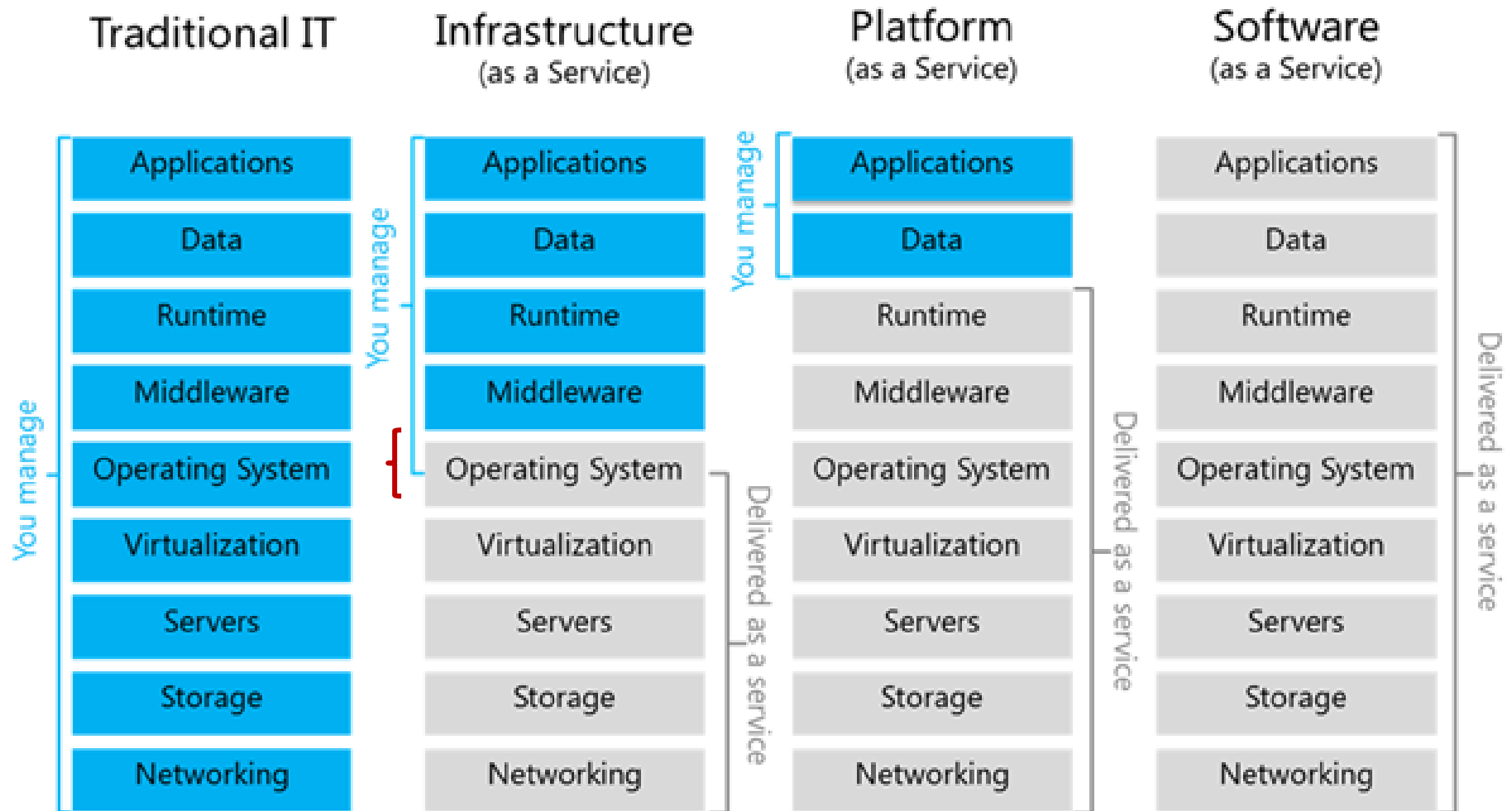
Service Models

Cloud Computing Service Models



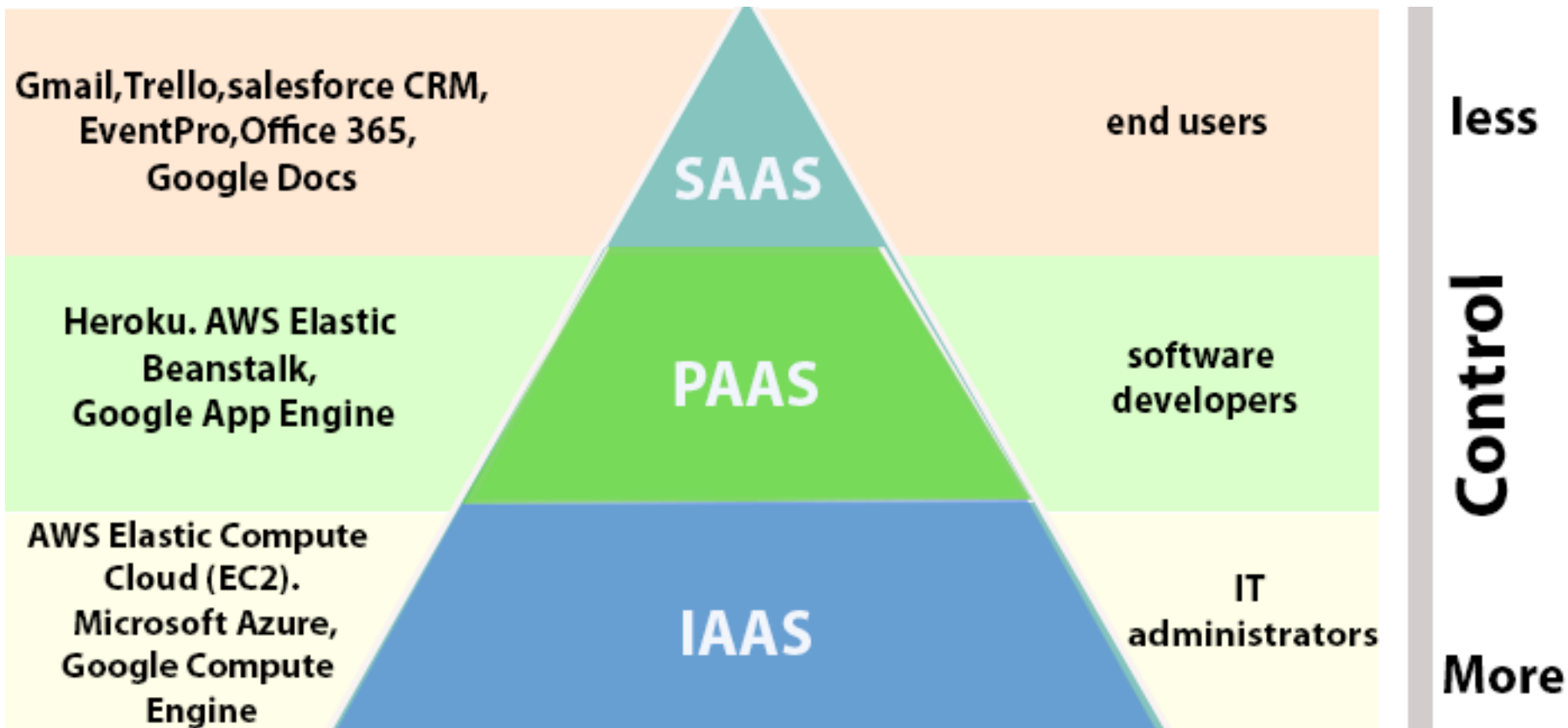


Cloud Service Models





Cloud Providers





SuperComputers



What is Cloud Computing?

- **Typical definition***: A **computer** that **leads** the world in **terms of processing capacity, speed of calculation**, at the time of its introduction
 - **Computer speed** is measured in **FLoating Point Operations Per Second (FLOPs)**
 - Currently the **LINPACK Benchmark** is **officially** used to **determine a computers speed**.
<http://www.netlib.org/benchmark/hpl>
 - **Top 500 SuperComputers**
 - A **ranked list** of **general purpose systems** that are in **common use for high-end applications**

*https://home.chpc.utah.edu/~thorne/computing/L13_Supercomputing_Part1.pdf



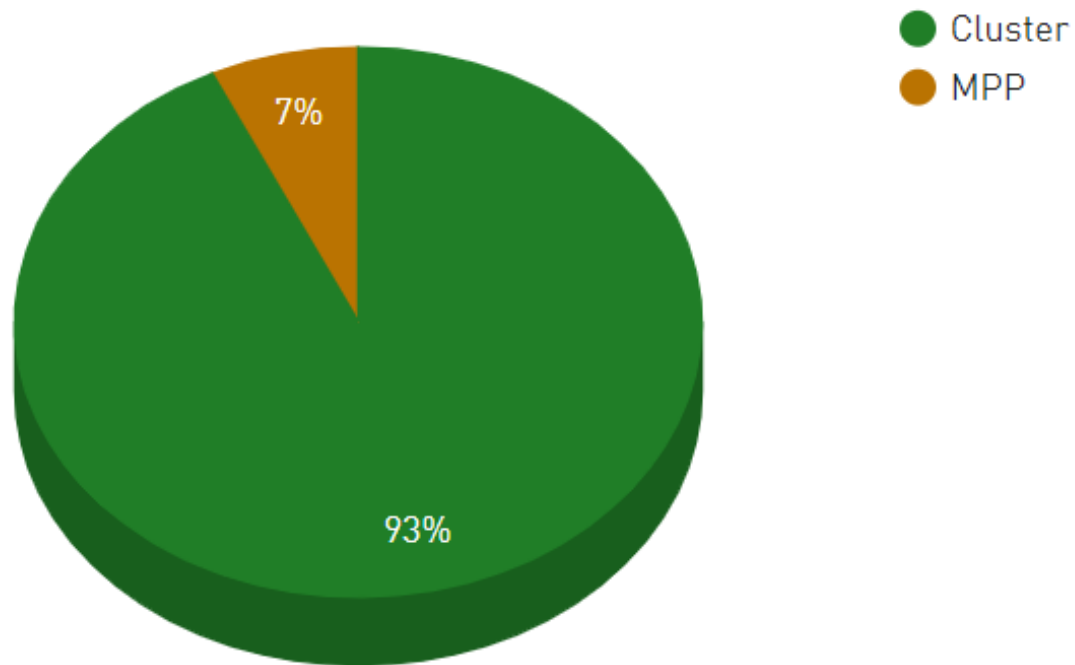
Top 5 of the list (Nov. 2020)

Rank	System	Cores	Rmax (TFlop/s)	Rpeak (TFlop/s)	Power (kW)
1	Supercomputer Fugaku - Supercomputer Fugaku, A64FX 48C 2.2GHz, Tofu interconnect D, Fujitsu RIKEN Center for Computational Science Japan	7,630,848	442,010.0	537,212.0	29,899
2	Summit - IBM Power System AC922, IBM POWER9 22C 3.07GHz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband, IBM DOE/SC/Oak Ridge National Laboratory United States	2,414,592	148,600.0	200,794.9	10,096
3	Sierra - IBM Power System AC922, IBM POWER9 22C 3.1GHz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband, IBM / NVIDIA / Mellanox DOE/NNSA/LLNL United States	1,572,480	94,640.0	125,712.0	7,438
4	Sunway TaihuLight - Sunway MPP, Sunway SW26010 260C 1.45GHz, Sunway, NRCPC National Supercomputing Center in Wuxi China	10,649,600	93,014.6	125,435.9	15,371
5	Selene - NVIDIA DGX A100, AMD EPYC 7742 64C 2.25GHz, NVIDIA A100, Mellanox HDR Infiniband, Nvidia NVIDIA Corporation United States	555,520	63,460.0	79,215.0	2,646



Top 500 SuperComputers - Nov. 2020

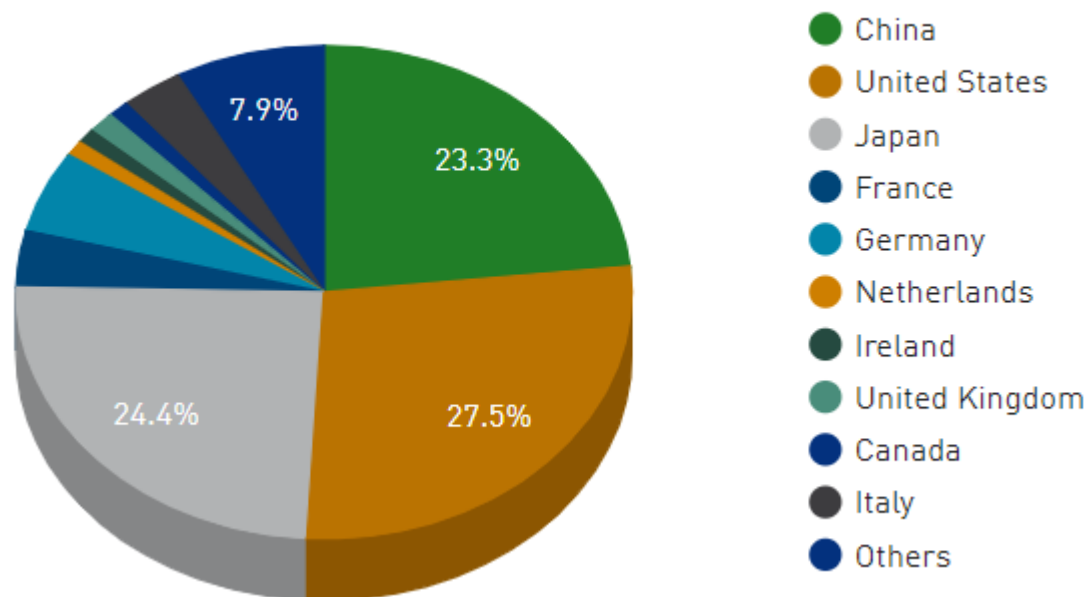
Architecture System Share



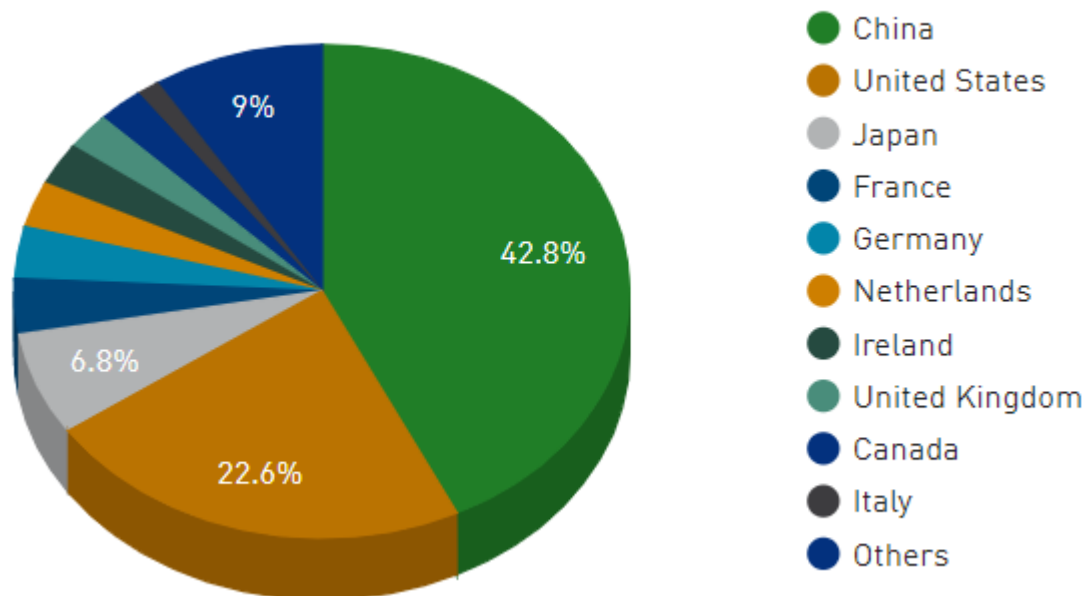


Top 500 SuperComputers - Nov. 2020

Countries Performance Share



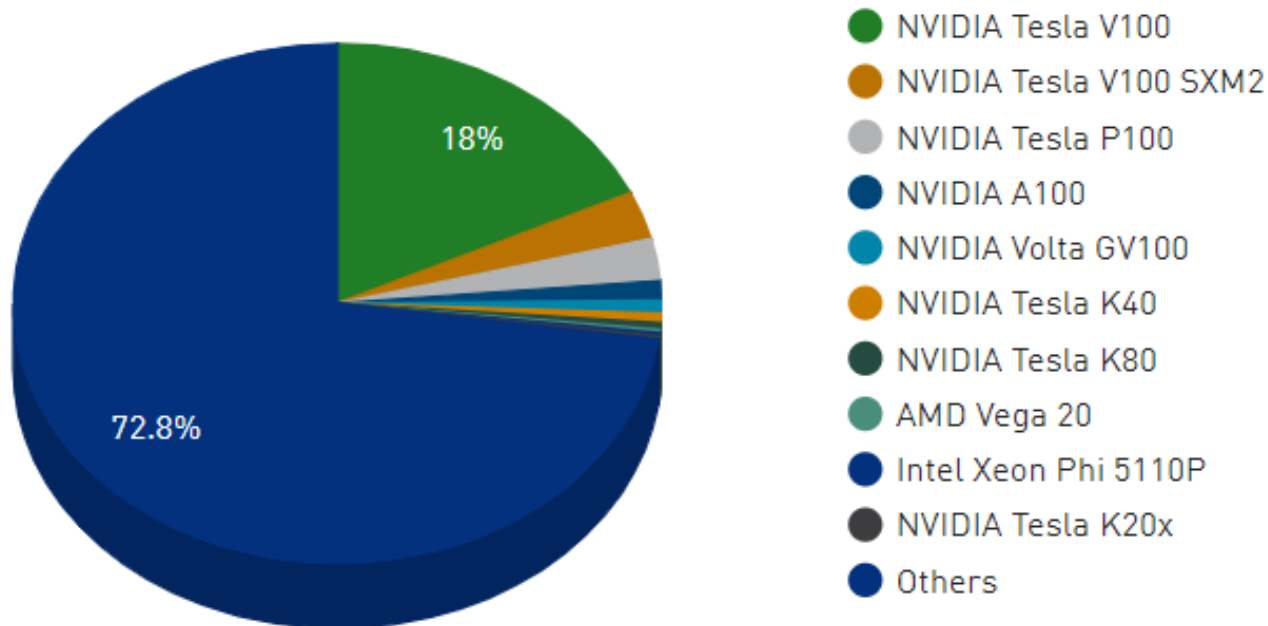
Countries System Share





Top 500 SuperComputers - Nov. 2020

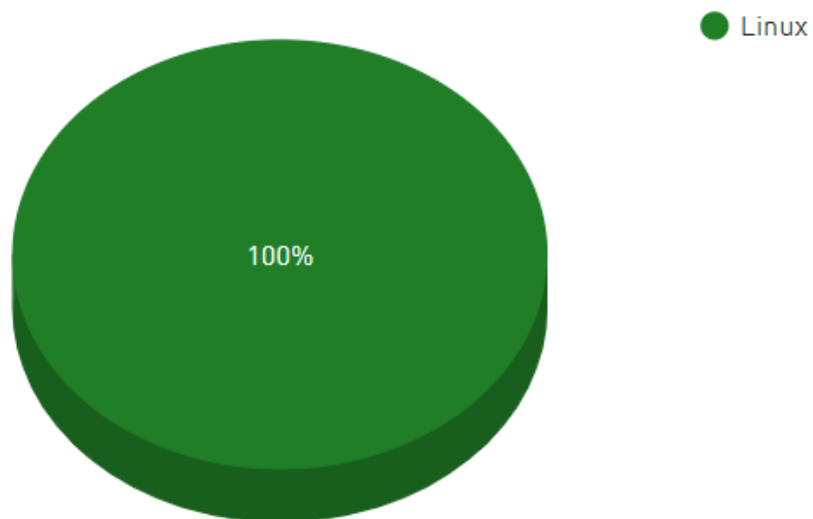
Accelerator/Co-Processor System Share



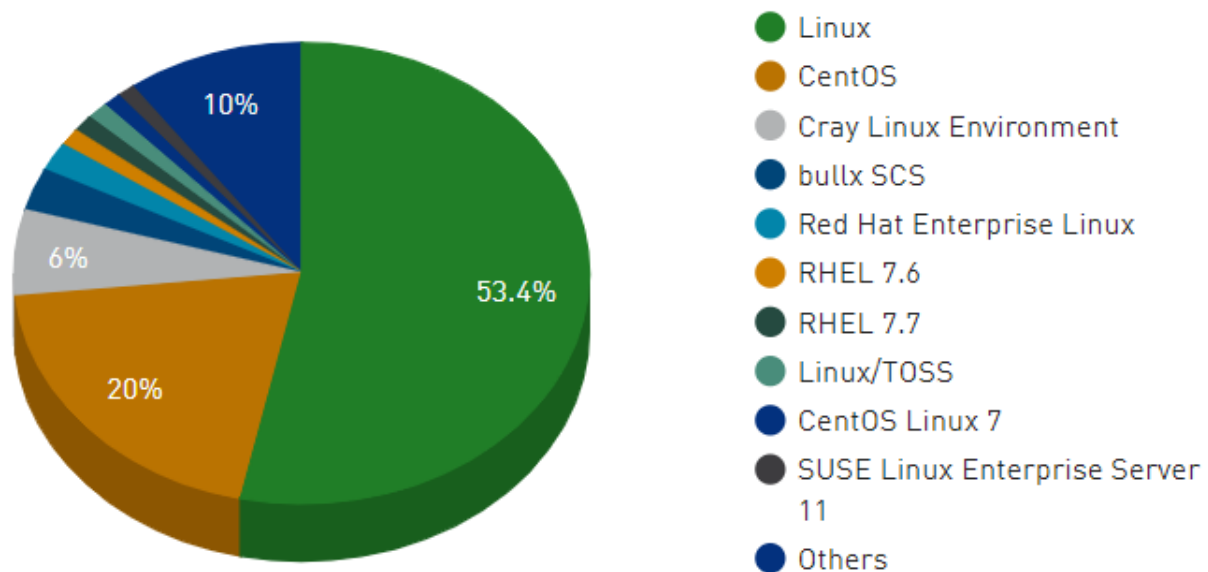


Top 500 SuperComputers - Nov. 2020

Operating system Family System Share



Operating System System Share





Any Questions?