Basics of Electronics Engineering (EC142)

FIELD EFFECT TRANSISTOR (FET)

CHITKARA UNIVERSITY

- INTRODUCTION TO JFET
- STRUCTURE OF JFET
- JFET CHARACTERSITICS
- JFET PARAMETERS

INTRODUCTION TO JFET

CHITKARA UNIVERSITY

- FET was developed in the early 1960s.
- Name ***field effect*** is derived from the fact that the current flow in the device is controlled by an electric field set up by an externally applied voltage.
- Two types of FETs

(a) Junction field effect tansistor

(b) Metal oxide semiconductor field effect transistor.

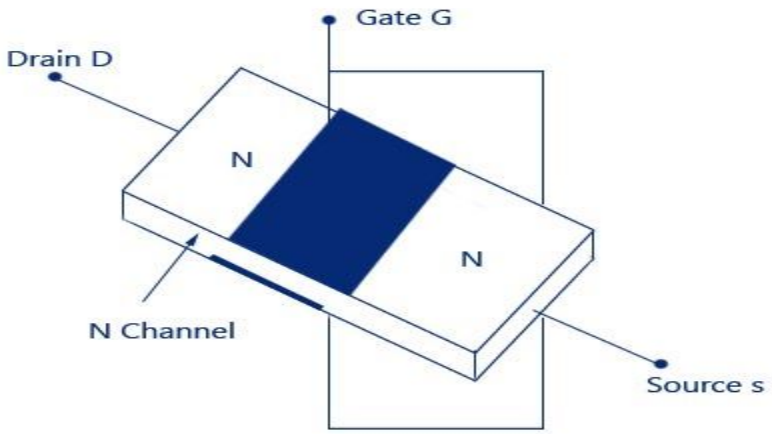
- In BJT, current is conducted by charge carriers of both polarity,whereas in FET current conducted by the majority charge carriers in the channel(by electrons in N-channel and by hole in P-channel)

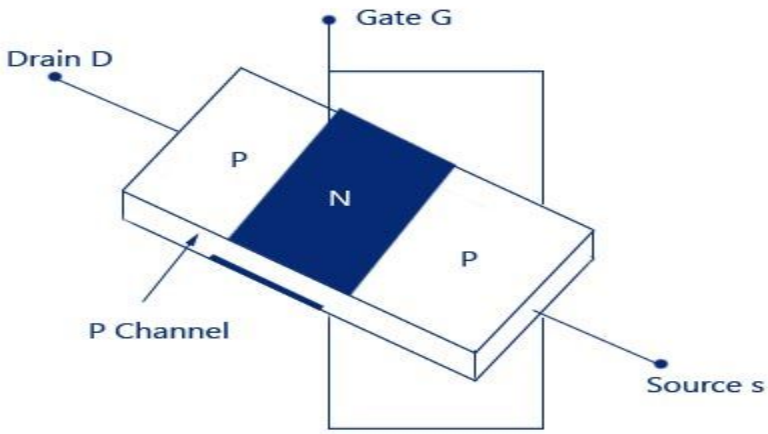
STRUCTURE OF JUNCTION FIELD EFFECT TRANSISTOR(JFET)

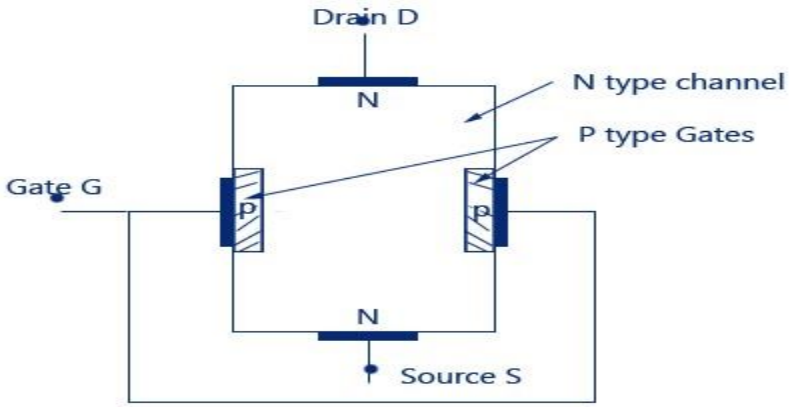
CHITKARA UNIVERSITY

- Two smaller pieces of P-type silicon material diffused on the opposite sides of its middle part, forming P-N junctions.
- Two P-N junctions forming diodes or gates are connected internally and a common terminal, called the gate terminal, is brought out.
- Ohmic contacts are made at the two ends of the channel—one lead is called the Source terminal S and the other Drain terminal D.
- The silicon bar behaves like a resistor between its two terminals D and S.
- The gate terminal is similar to the base of an ordinary transistor(BJT) and used to control the flow of current from source to drain.

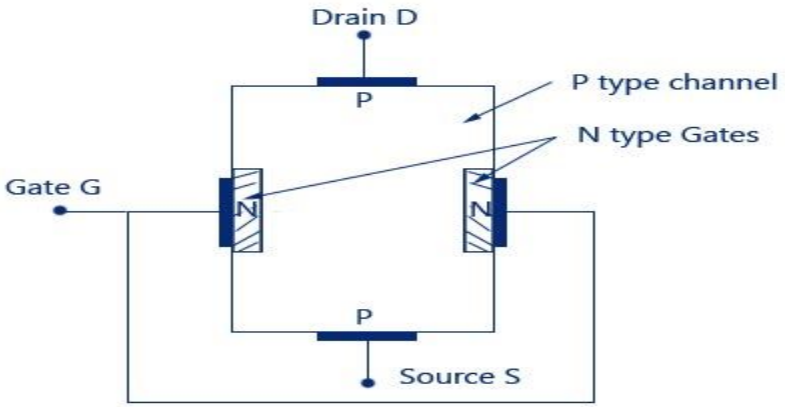
STRUCTURE OF JFET







N Channel JFET



P Channel JFET

JFET Junction Field Effect Transistors

STRUCTURE OF JUNCTIONFIELD EFFECT TRANSISTOR(JFET)

CHITKARA UNIVERSITY

- JFET is a silicon device, it takes only 0.7 volts for forward bias to get significant current in either diode.

- With the gate terminal not connected, and a potential applied (+ ve at the drain and – ve at the source), a current called the drain current.

- ID flows through the channel located between the two P-regions. This current consists of only majority carriers-electrons in this case.

Standard Notations in FET:

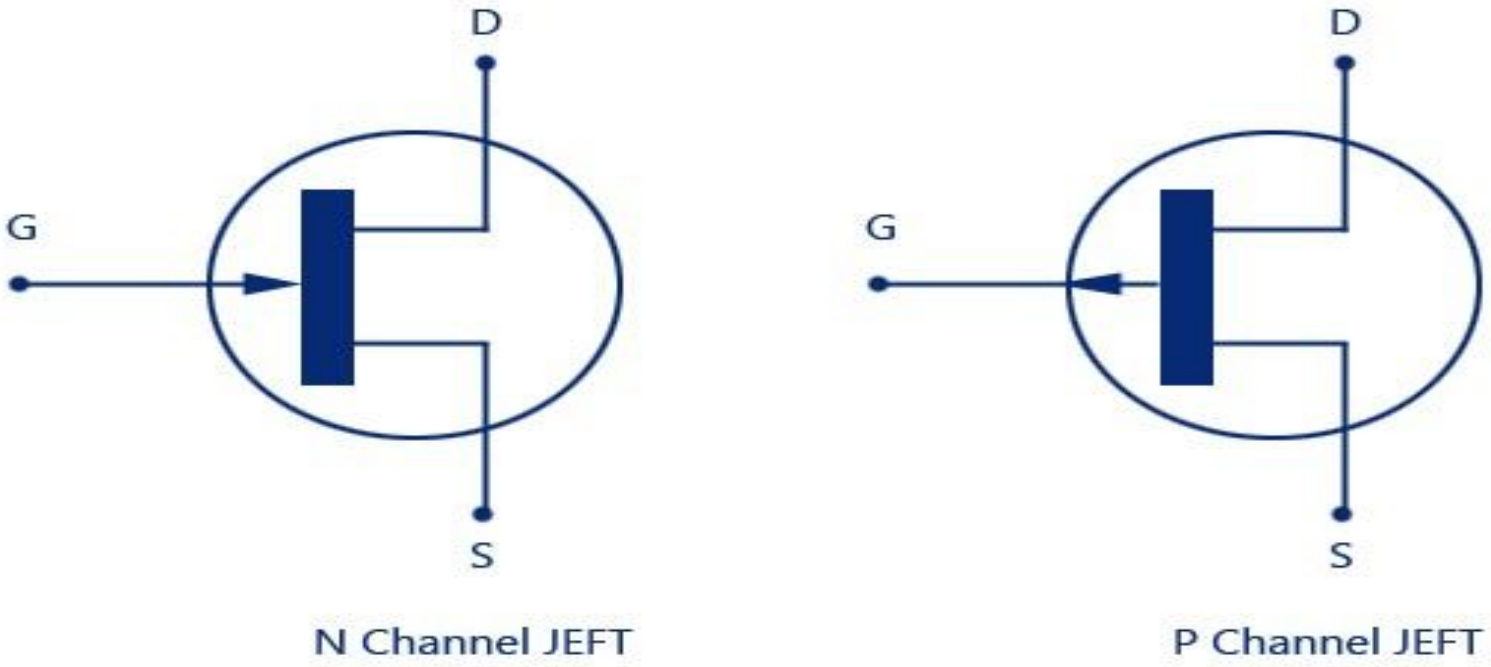
- ***Source*** – The terminal through which the majority carriers enter the channel, is called the source terminal S.

- ***Drain*** – The terminal, through which the majority carriers leave the channel, is called the drain terminal D.

- ***Gate*** – There are two internally connected heavily doped impurity regions formed by alloying, by diffusion,These impurity regions are called the gate G. A voltage VGS is applied between the gate and source in the direction to reverse-bias the P-N junction.

- ***Channel*** – The region between the source and drain, sandwiched between the two gates is called the channel.

SYMBOL OF N CHANNEL AND P CHANNEL JFET



JFET-N-Channel and P-channel Schematic Symbol

CONTD.....

- The direction of the arrow at the gate indicates the direction in which the gate current flows when the gate junction is forward biased.

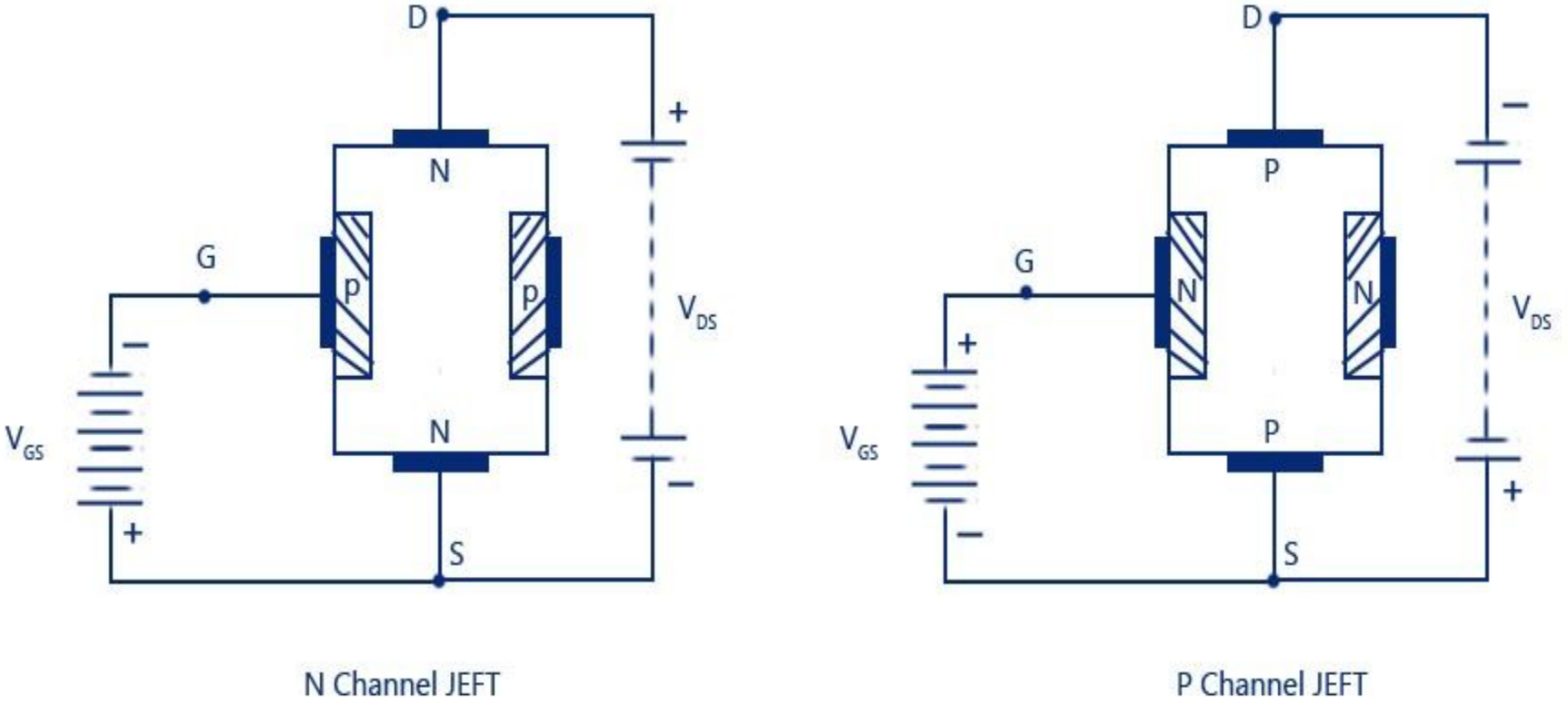
- The N-channel JFET, the arrow at the gate junction points into the device and in P-channel JFET, it is away from the device.

POLARITY CONVENTION USED IN JFET

CHITKARA UNIVERSITY

- The voltage between the gate and source is such that the gate is reverse biased.
- The drain and source terminals are interchangeable, that is either end can be used as a source and the other end as a drain.
- The source terminal is always connected to that end of the drain voltage supply which provides the necessary charge carriers, that is, in an N-channel JFET source terminal, S is connected to the negative end of the drain voltage supply for obtaining.

POLARTIY CONVENTION IN JFET



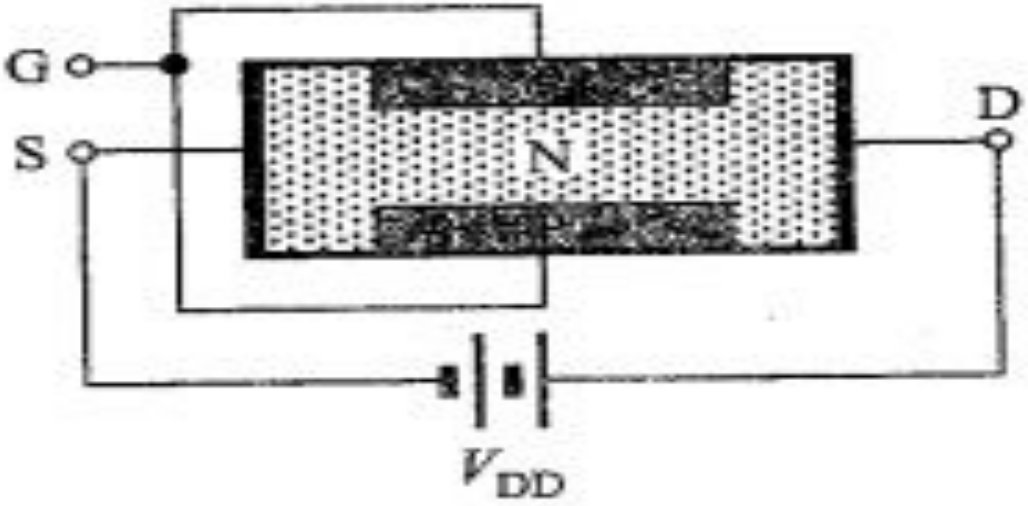
N Channel JEFT

P Channel JEFT

JFET Polarity Conventions

WORKING OF N-CHANNEL JFET

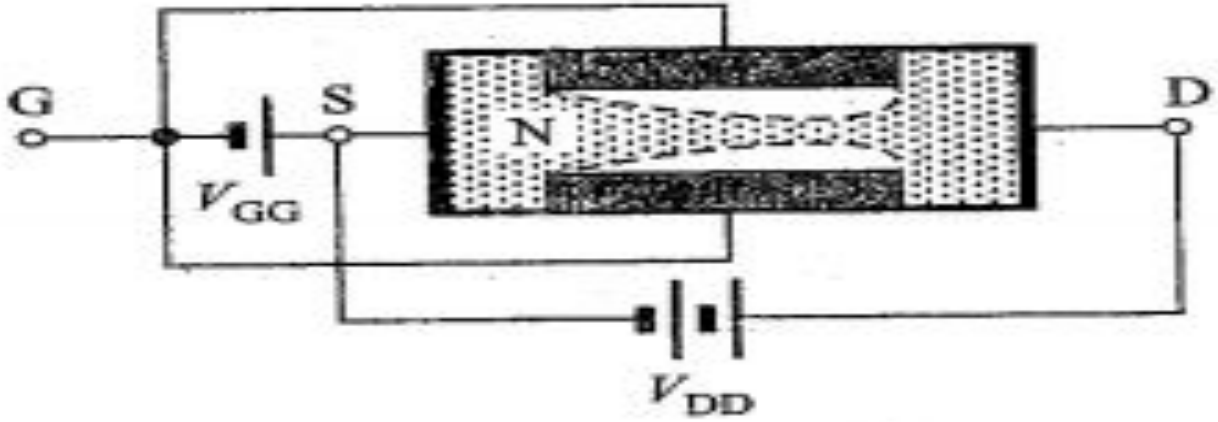
- When no bias is applied to the gate (i.e. when VGS = 0) and (i.e. when VDS = 0), the depletion regions around the P-N junctions , are of equal thickness and symmetrical.



(a) With no bias

WORKING OF N-CHANNEL JFET

- When positive voltage is applied to the drain terminal D w.r.t. source terminal S without connecting gate terminal G to supply, the electrons (which are the majority carriers) flow from terminal S to terminal D whereas conventional drain current ID flows through the channel from D to S.



(b) With small reverse bias

WORKING OF N-CHANNEL JFET

- Due to flow of this current, there is uniform voltage drop across the channel and this voltage drop reverse biases the diode.
- The gate is more “negative” to the channel which are nearer to D than to S. depletion layers penetrate more deeply into the channel at points lying closer to D than to S.
- Wedge-shaped depletion regions are formed,
- when Vds is applied. The size of the depletion layer formed determines–the width of the channel and hence the magnitude of current ID flowing through the channel.

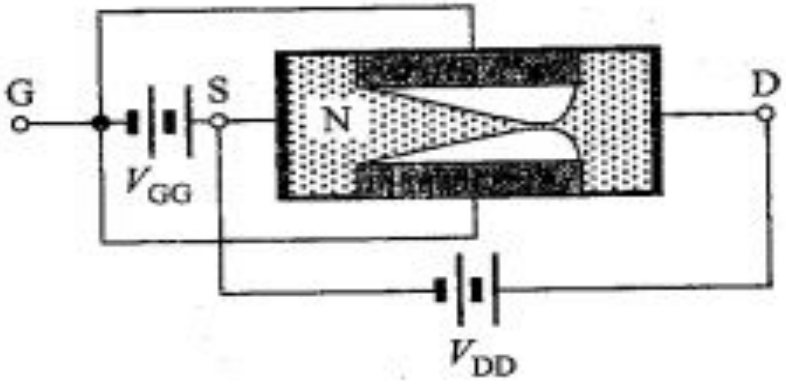
WORKING OF N-CHANNEL JFET

- how the width of the channel varies with the variation in gate voltage, assume that the gate is negative biased with respect to the source while the drain is applied with positive bias with respect to the source.
- The P-N junctions are then reverse biased and depletion regions are formed. P regions are heavily doped compared to the N-channel, so the depletion regions penetrate deeply into the channel.
- The result is that the channel is narrowed, the resistance is increased and drain current ID is reduced. If the negative voltage at the gate is again increased, depletion layers meet at the centre and the drain current s cut-off completely.

WORKING OF N-CHANNEL JFET

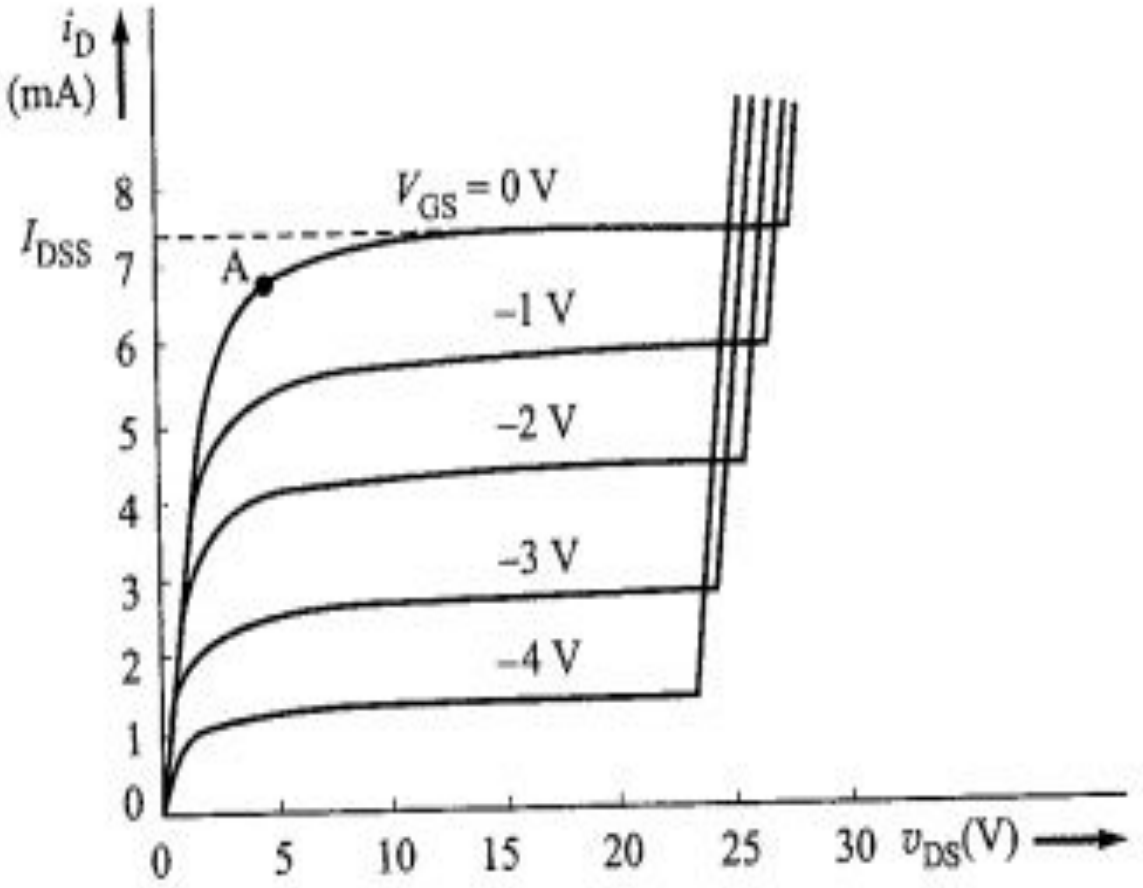
- If the negative bias to the gate is reduced, the width of the depletion layers gets reduced causing decrease in resistance and , therefore, increase in drain current ID.

- (The gate-source voltage VGS at which drain current ID is cut-off completely (pinched off) is called the pinch-off voltage Vp.



(c) Pinch-off occurs at large reverse bias

JFET CHARACTERISTICS



JFET PARAMETERS

CHITKARA UNIVERSITY

- **Dynamic Drain Resistance(r_d)** : Ratio of small change in drain voltage to the change in drain current,keeping the gate voltage constant

$$r_d = \frac{\Delta v_{DS}}{\Delta i_D}\Big|_{V_{GS}= Const.}$$

- **Mutual conductance or Transconductance(g_m)**: Ratio of small change in drain current to the small change in gate voltage,keeping the drain voltage constant.

$$g_m = \frac{\Delta i_D}{\Delta v_{GS}}\Big|_{V_{DS}= Const.}$$

JFET PARAMETER

CHITKARA UNIVERSITY

- **Amplification Factor(μ)**: Ratio of small change in drain voltage to the small change in gate voltage, keeping the drain current constant.

$$\mu = \left.\frac{\Delta v_{DS}}{\Delta v_{GS}}\right|_{I_D = Const.}$$

CHITKARA UNIVERSITY

Thank You