# Speculative Taint Tracking (STT): A Comprehensive Protection for Speculatively Accessed Data

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ADAM MORRISON*, JOSEP TORRELLAS, CHRISTOPHER W. FLETCHER
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# Speculative Execution Attacks

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// Spectre Variant 1

if (addr < N) {    // speculation

    // access instruction
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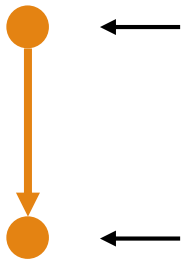

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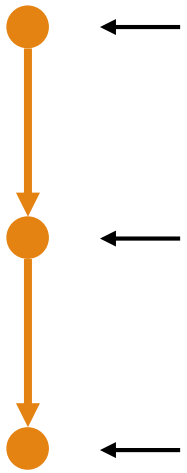

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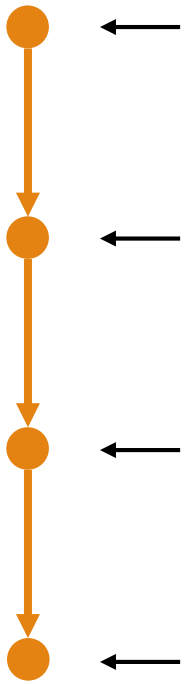

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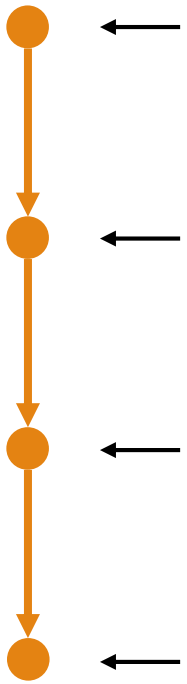

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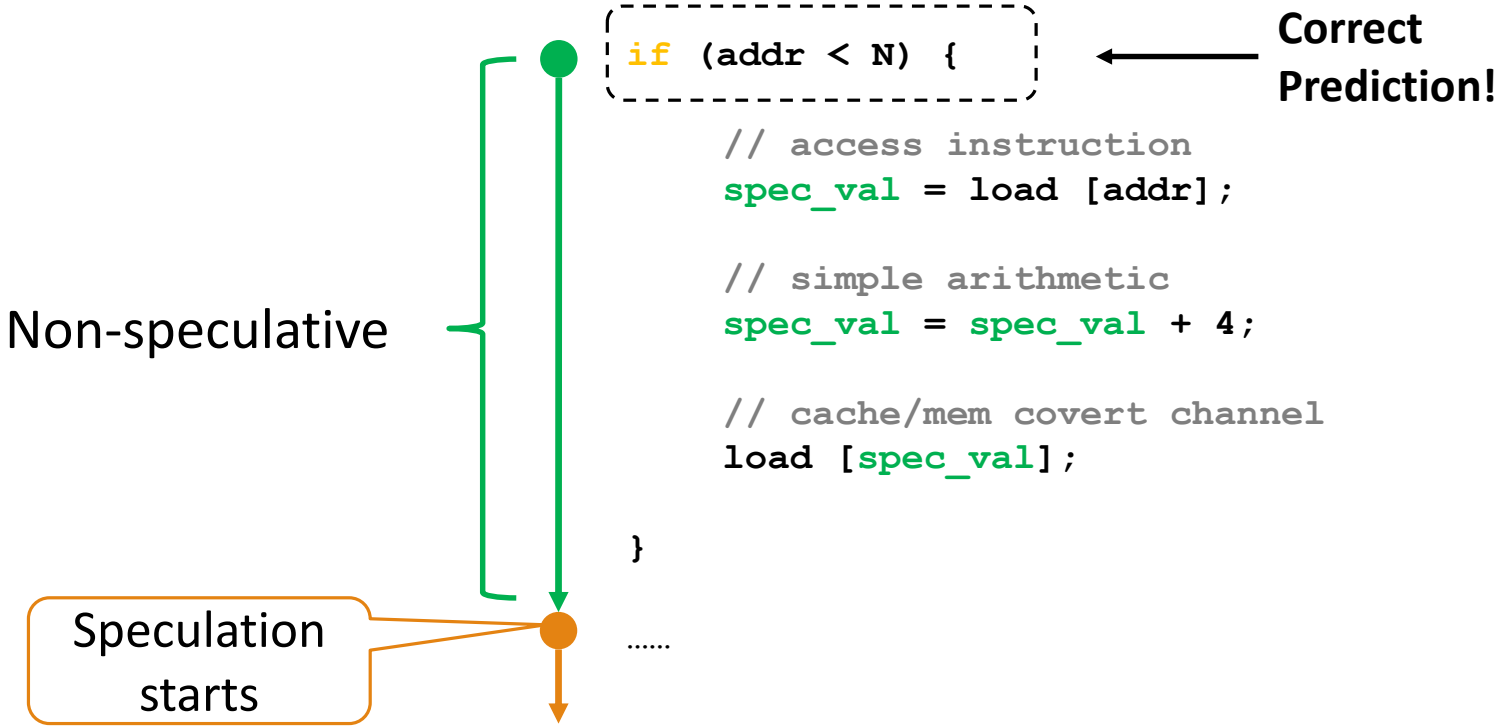


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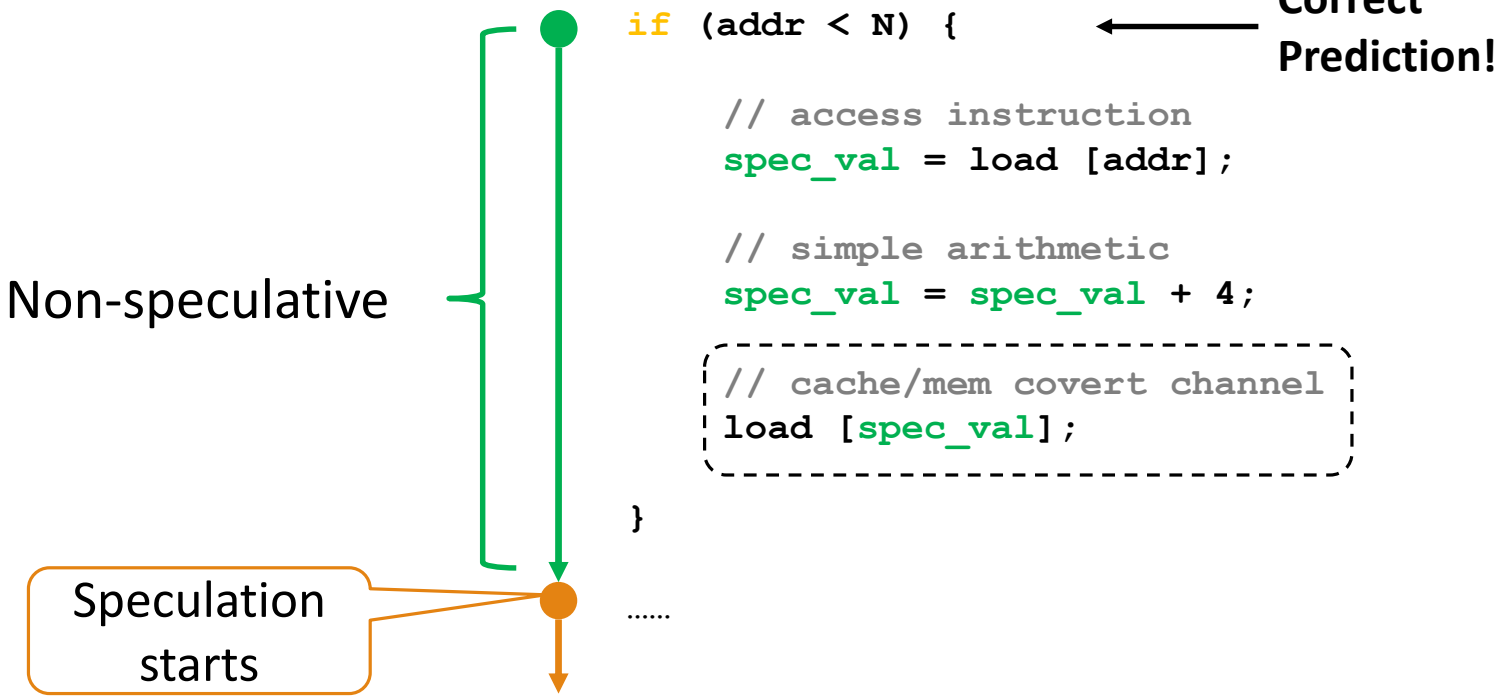


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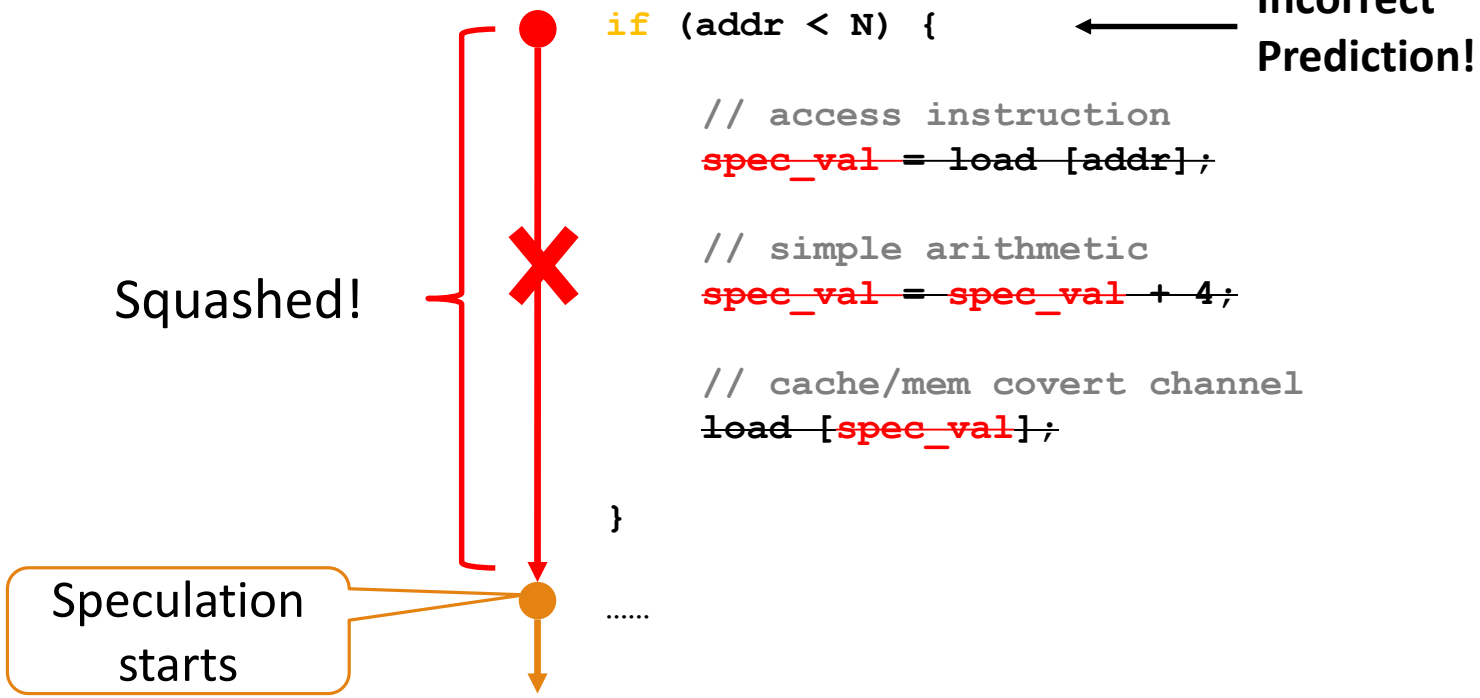


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**What are the covert channels?** → **A new classification to understand covert channels in speculative machines**

**How to identify all the secrets?** → **A new taint/untaint mechanism to track secrets in hardware**

# A Classification of Covert Channels in HW

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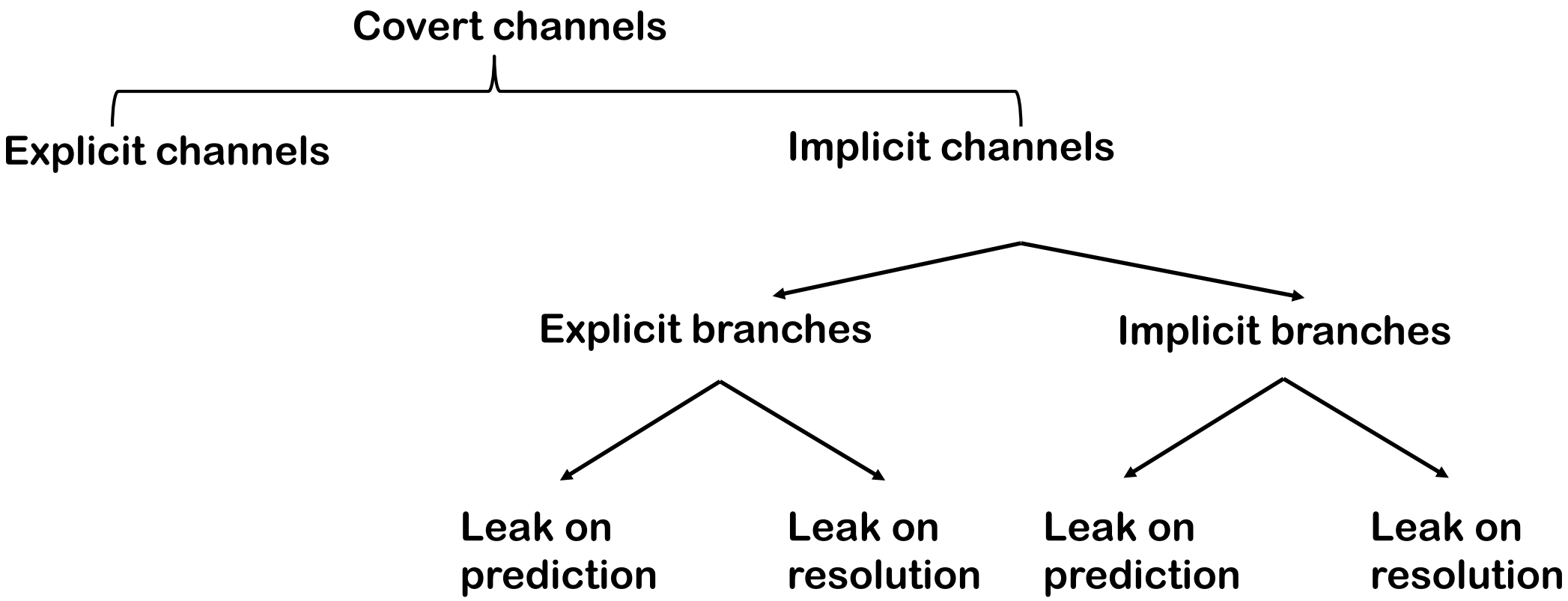

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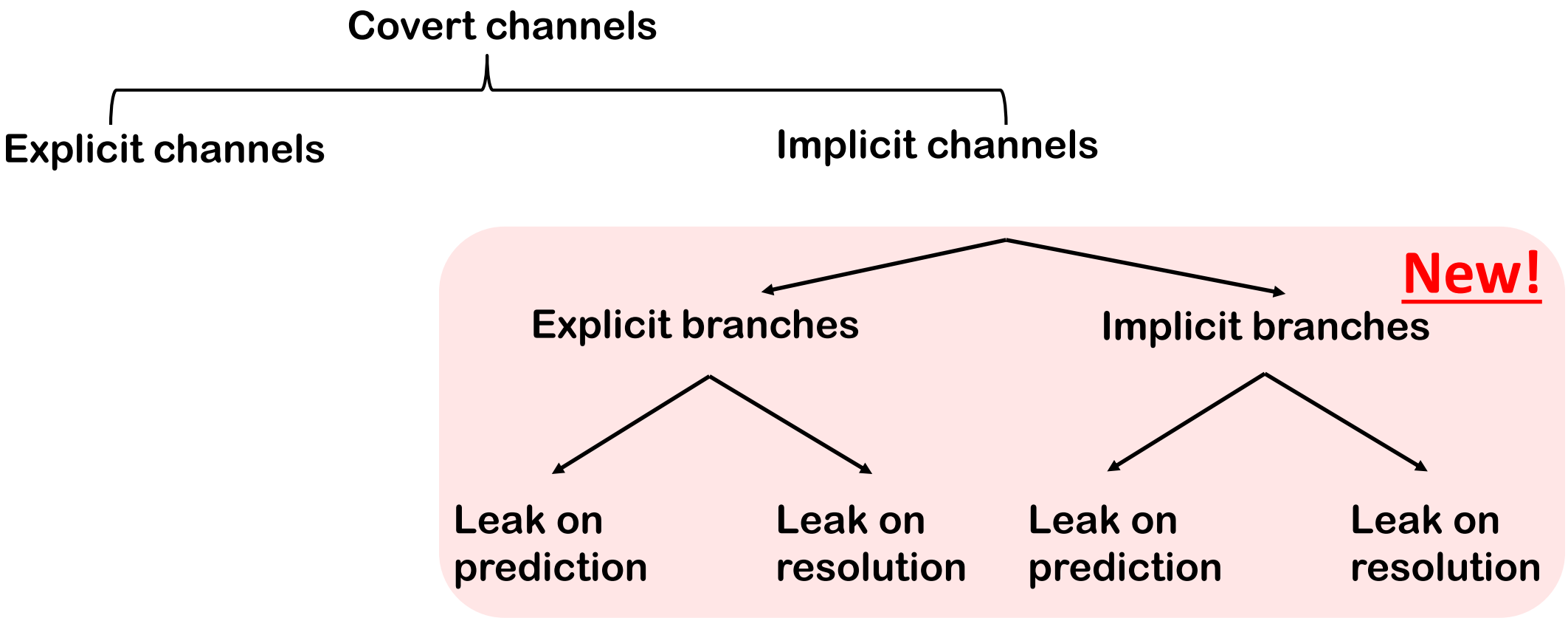

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**Explicit channels:**
Secret inputs are directly leaked by *operand-dependent hardware resource usage*

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load [secret];
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secret = load [addr];
if (secret == 1)
    load [0x00];
```

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The predictor state becomes a function of secret

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… …
if ( secret )
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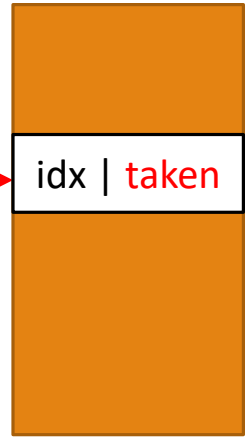
Resolve and update branch predictor

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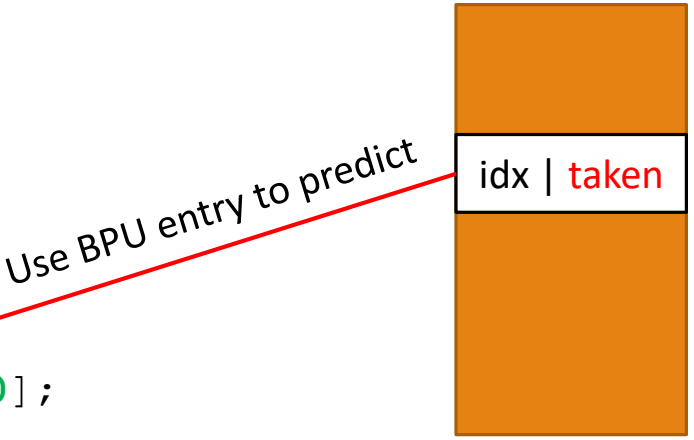


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**secret** != prediction
→ squash
→ load executes twice!

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store [secret] = foo;

bar = load [0x00];
```

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Non-control flow instructions create branch-like behaviors.

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Non-control flow instructions create branch-like behaviors.

```
store [secret] = foo;

bar = load [0x00];
```

Can be thought as:

```
if (secret == 0x00) {
    forward from store queue
}
else {
    cache_load [0x00]
}
```

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speculative

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......
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speculative

# Microarchitect Identifies …

Instructions forming **explicit channels**

- E.g. load, data-dependent arithmetic

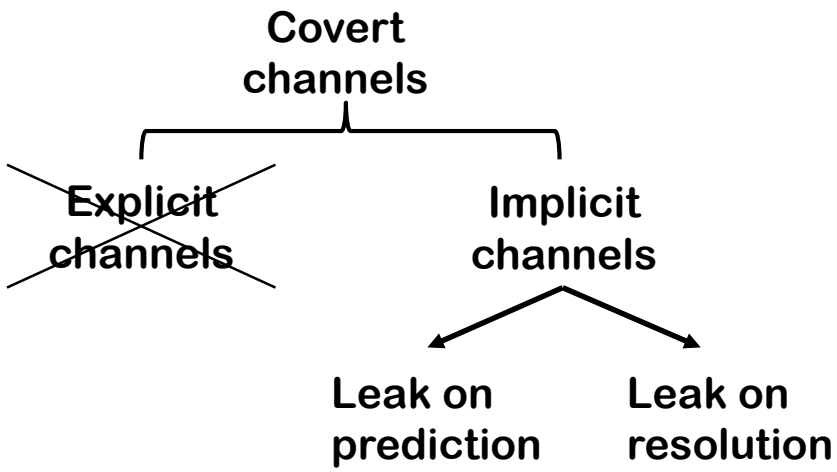
Instructions forming **implicit channels**

- E.g. control-flow instructions, store-load pairs

# Blocking Covert Channels

**Explicit channels:**

- Delay execution until operands **untainted** (e.g., load address)



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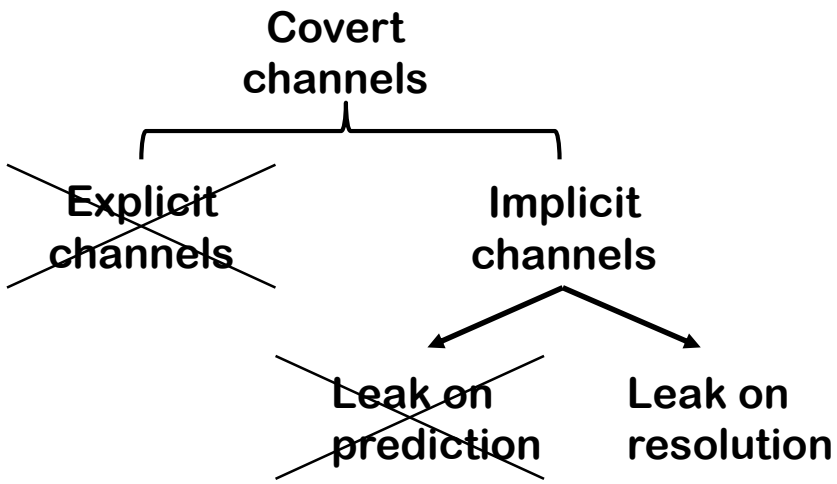

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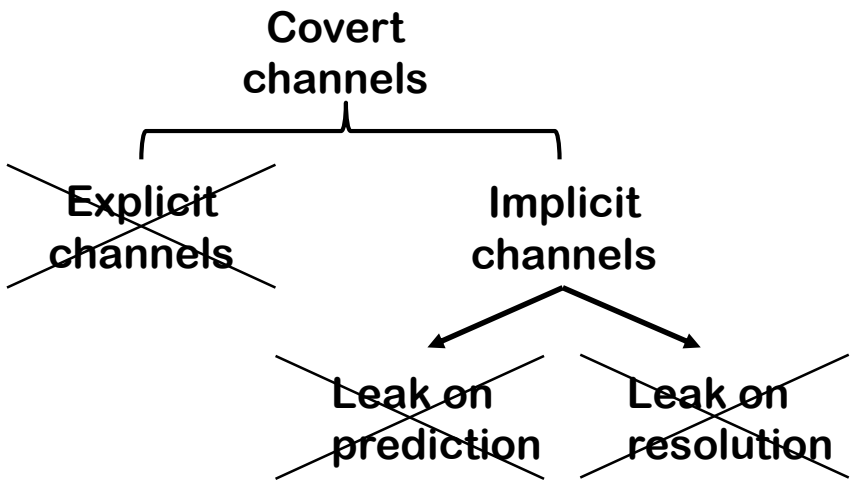

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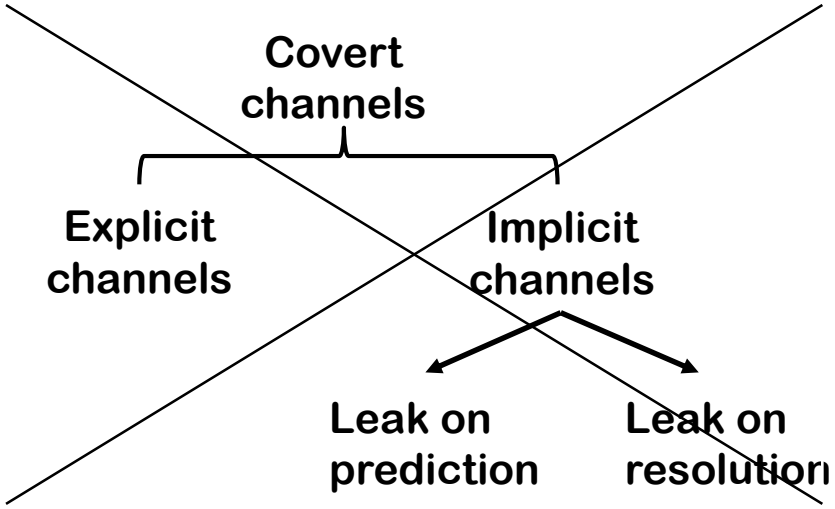

# Hardware Implementation of STT

# Efficient Implementation of Tainting/Untainting Logic

program order

1) branch
2) a = load [0x00]
3) branch
4) b = load [0x04]
5) branch
6) c = a + b
7) load [c]

Delay execution!

speculative

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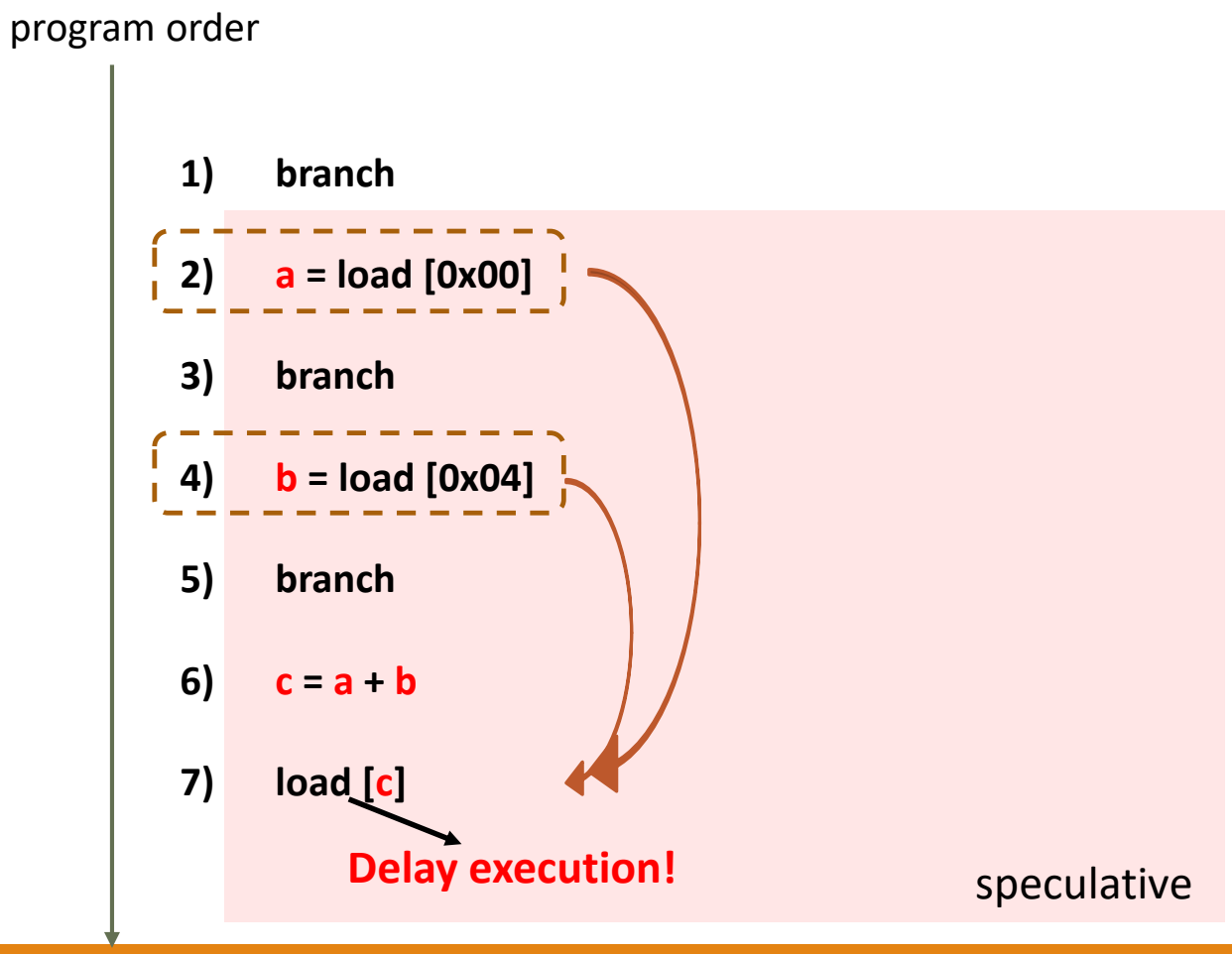

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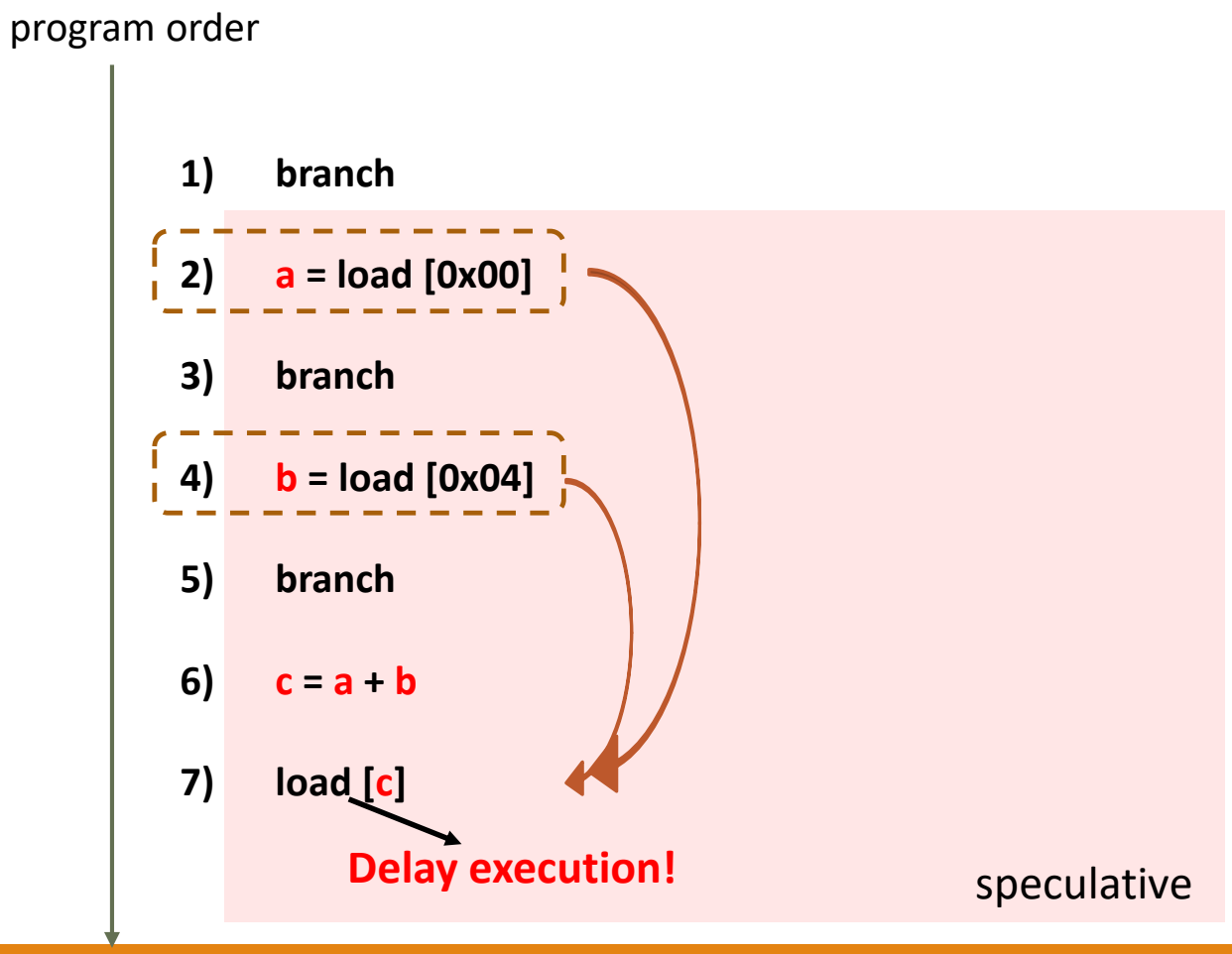
Observation: All instructions turn non-speculative in-order



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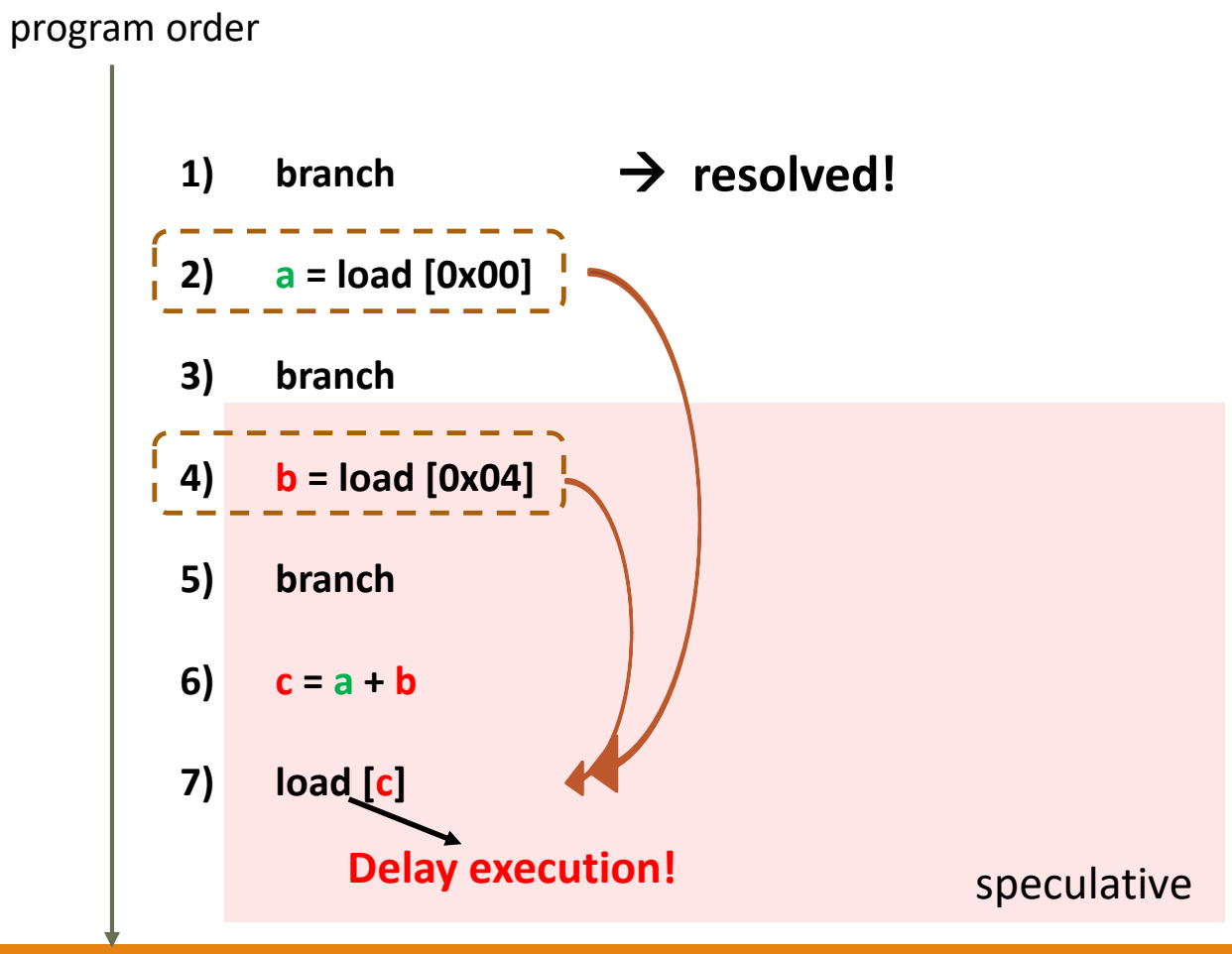

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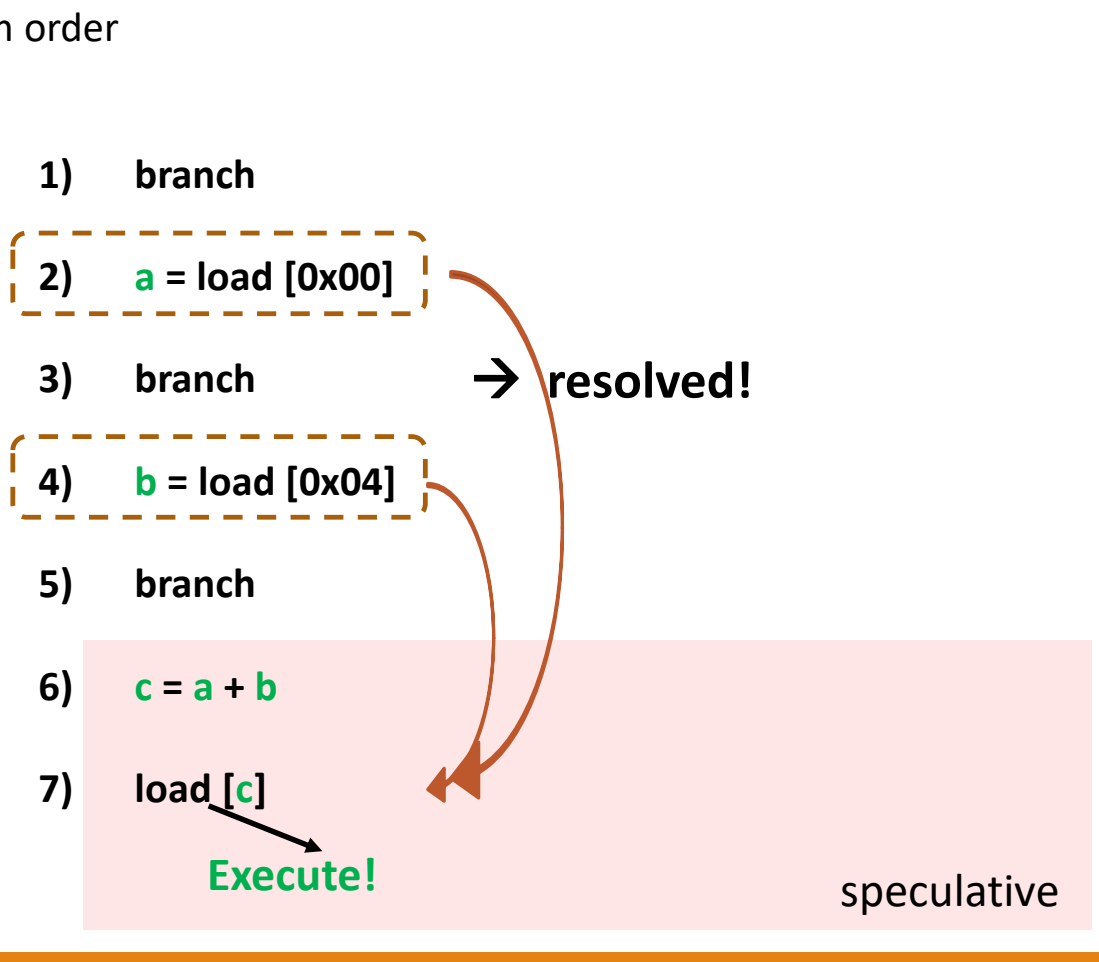

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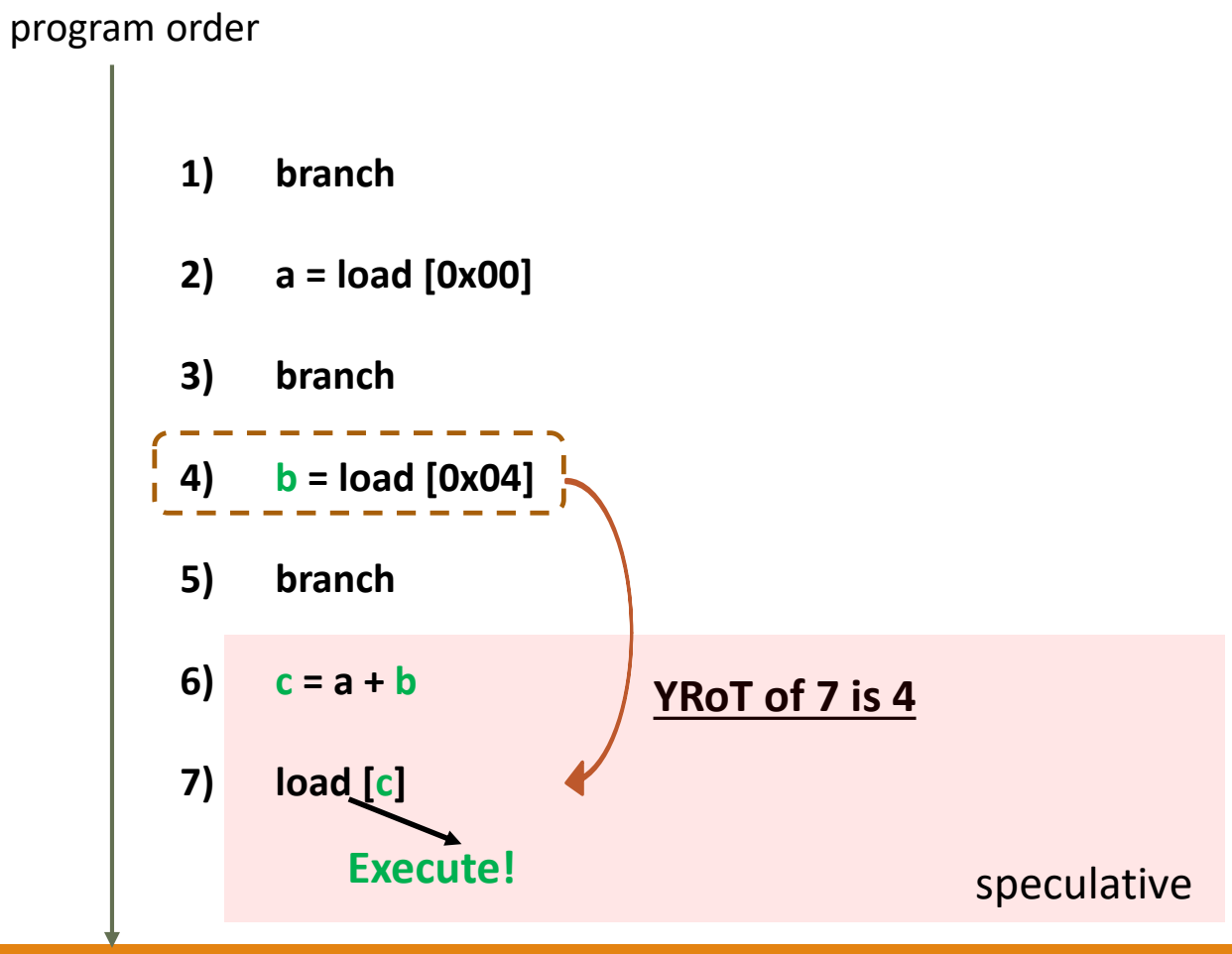
Each instruction tracks the "youngest access instruction" it depends on -- ***"Youngest Root of Taint" (YRoT)***



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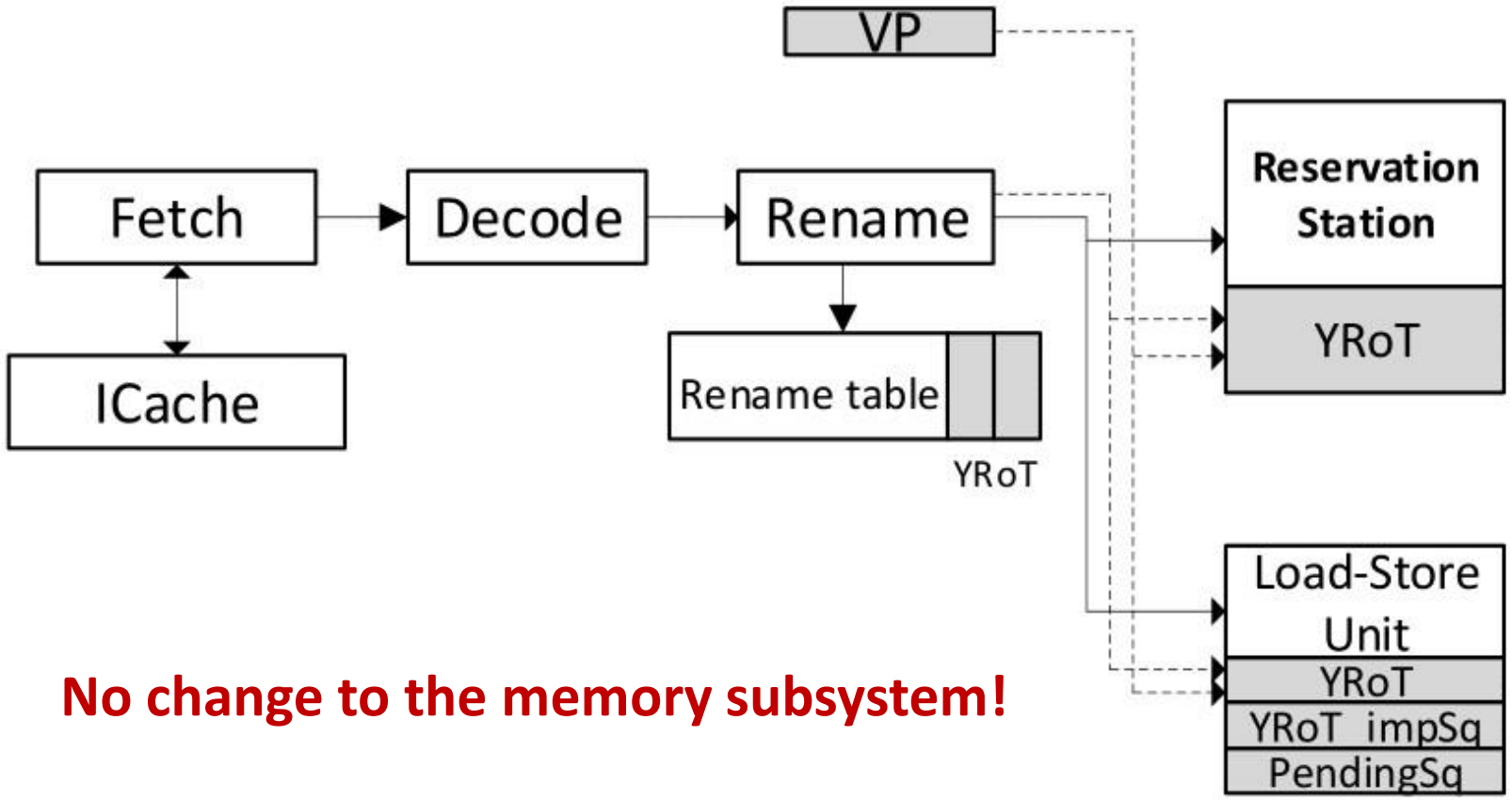



**No change to the memory subsystem!**

# Security Evaluation

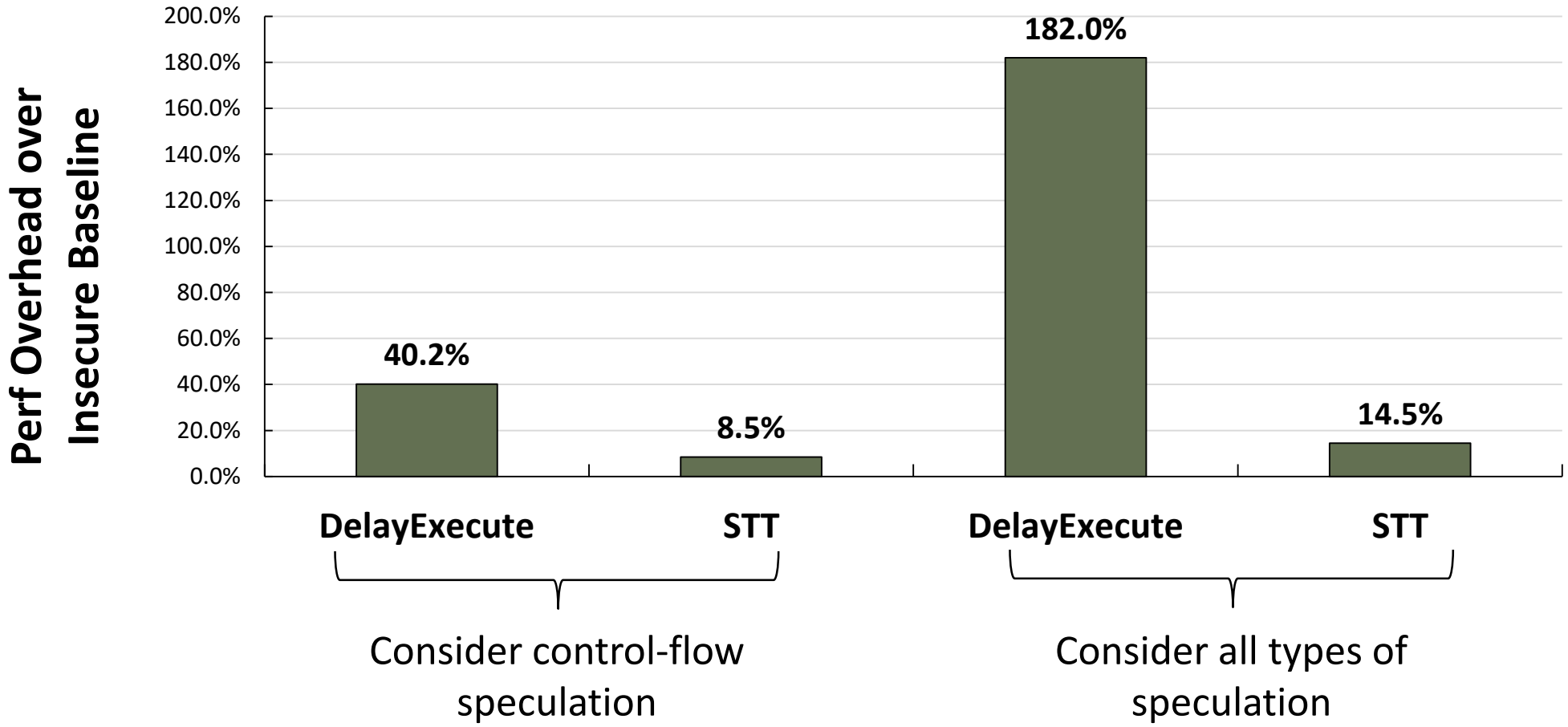
Security definition:

**Arbitrary speculative execution can only leak retired register file state (not arbitrary program memory)**

To prove it: STT enforces a non-interference property w.r.t speculatively accessed data

The link to the **detailed formal analysis and security proof** is in the paper

# Performance Evaluation on SPEC2006



# Conclusion

STT Blocks leakage of speculatively accessed data over any uarch covert channels with:

1) High performance

2) Provable security protection

3) No software change; No memory subsystem change

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**Questions?**

# Backup slides

# Threat Model

A powerful attacker who:

- Monitors covert channels
  - Cache, SIMD units, or any shared hardware resources
- From everywhere
  - Within same thread
  - Adjacent SMT context
  - Cross core
- At cycle granularity

# TODO: compare with NDA and SpecShield

# TODO: STT threat model vs. STT+ threat model

# Outline

Introduction

Threat Model

Speculative Taint Tracking

Evaluation

Conclusion

# Implementation of STT

A new classification of covert channels in HW

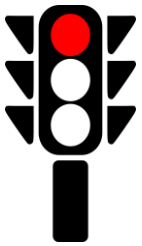
➔ Specify instructions with explicit or implicit channels

# Putting it together

Executes all instructions w/ untainted inputs

Executes non-transmit instructions w/ tainted inputs

Predicts explicit/implicit branches w/ tainted predicates



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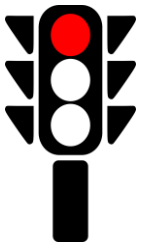


Delay executing transmit instructions w/ tainted inputs → Block explicit channel

Delay resolution/predictor updates of explicit/implicit branches w/ tainted predicates

# Putting it together

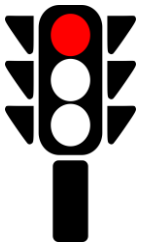
Executes all instructions w/ untainted inputs

TODO: spend a little bit more time on this slide?

Executes non-transmit instructions w/ tainted inputs

Predicts explicit/implicit branches w/ tainted predicates

TODO: what is transmit instruction?



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# Microarchitecture Design of STT

- Each instruction has its "*Youngest Root of Taint*" (YRoT)

For each (transmit) instruction:

Input is secret

⇔ YRoT is still speculative

⇔ Visibility point is ahead of YRoT

program order

1) branch
2) a = load [0x00] // YRoT = -1
3) branch_1
4) b = load [0x04] // YRoT = -1
5) branch
6) **c** = a + b // YRoT = max(2, 4) = <u>4 > 1</u>
7) d = load [**c**] // YRoT = <u>4 > 1</u>

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program order

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2) a = load [0x00] // YRoT = -1

3) branch_1

4) b = load [0x04] // YRoT = -1

5) branch_2

6) **c** = a + b // YRoT = max(2, 4) = <u>4 > 3</u>

7) d = load [**c**] // YRoT = <u>4 > 3</u>

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2)  a = load [0x00]     // YRoT = -1
3)  branch_1
4)  b = load [0x04]     // YRoT = -1
5)  branch_2                          ← VP
6)  c = a + b           // YRoT = max(2, 4) = 4 < 5
7)  d = load [c]        // YRoT = 4 < 5
```

# Efficient Implementation of Tainting/Untainting Logic

Observation: All instructions turn non-speculative in-order

Each instruction tracks the "youngest access instruction" it depends on -- ***"Youngest Root of Taint" (YRoT)***

For each instruction:

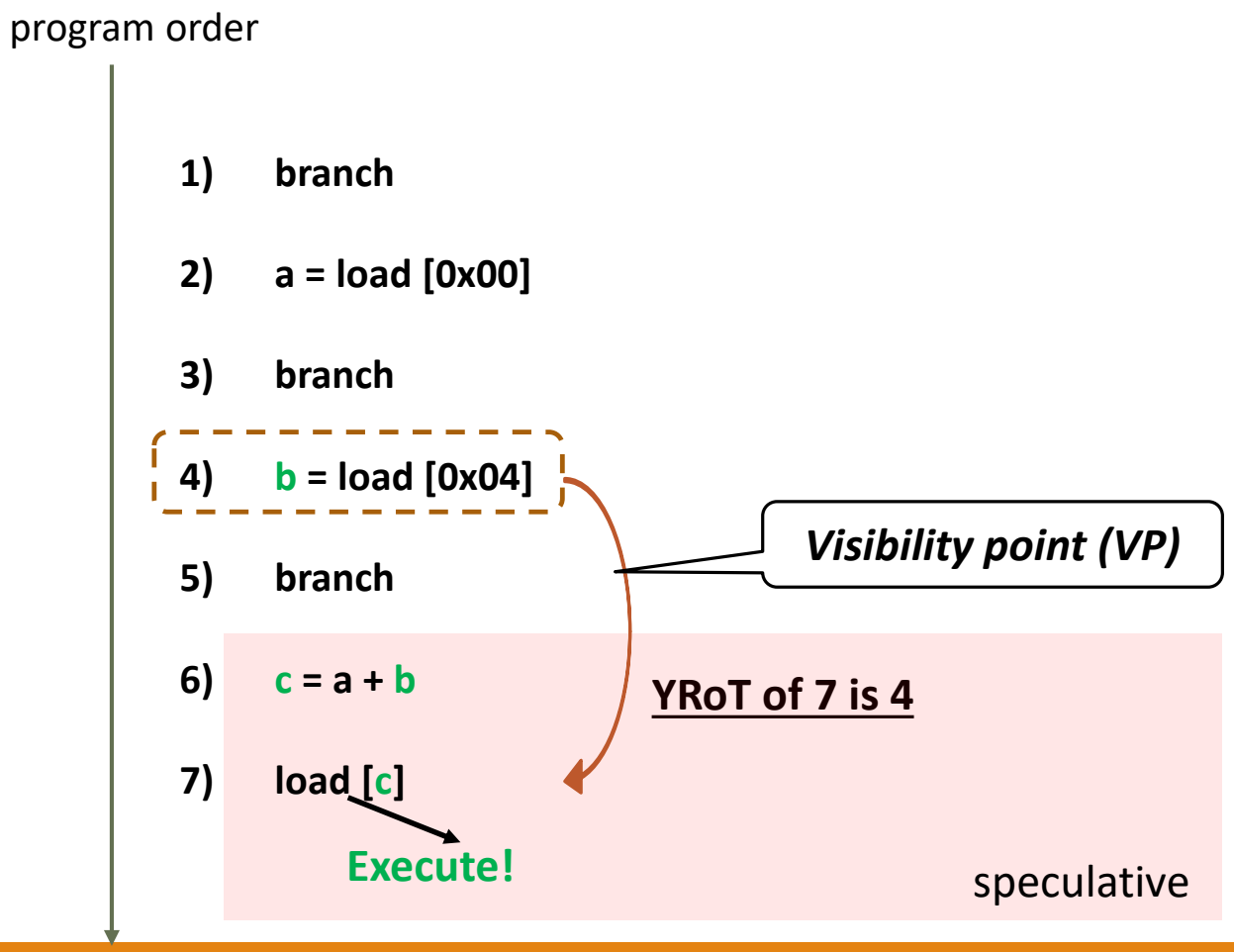
Input is tainted

TODO: remove this

⇔ Input depends on some speculative access instruction

⇔ YRoT is still speculative

⇔ Visibility point is ahead of YRoT



# Security Evaluation

Arbitrary speculative execution can only leak retired register file state (not arbitrary program memory)

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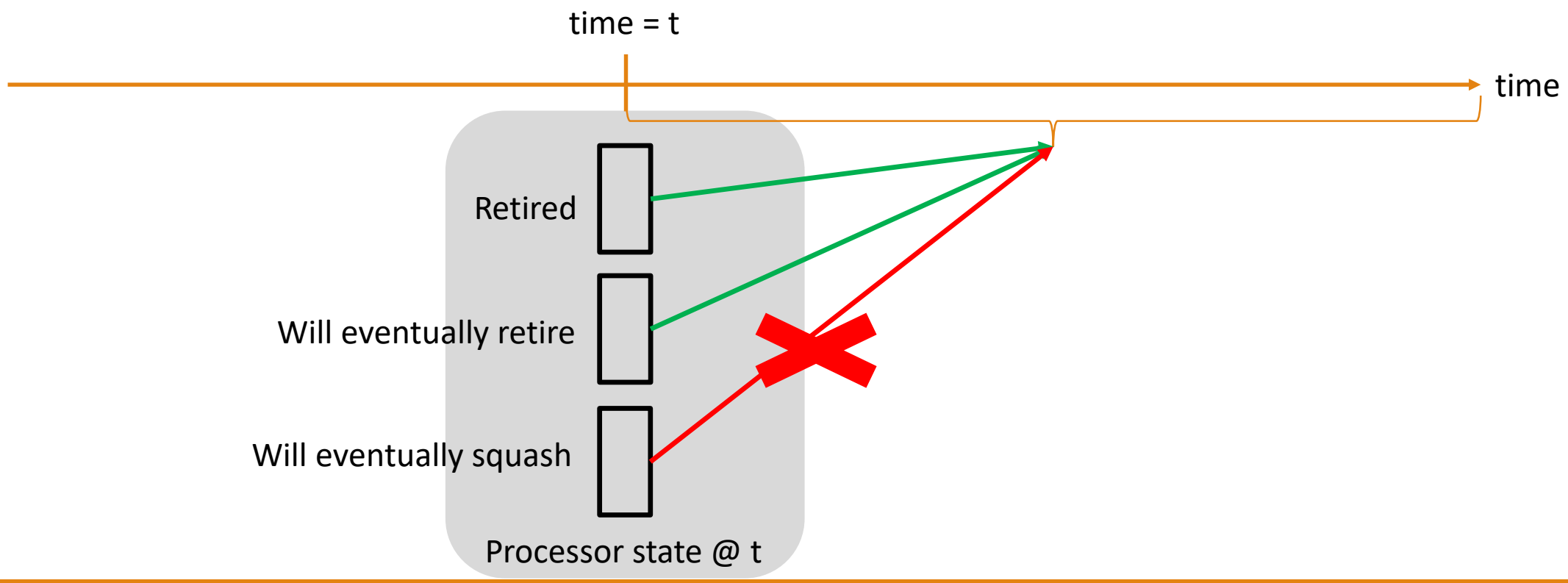
**The Universal Read Gadget** == many Spectre variants (1, 3, 4, ..), MDS attacks, Meltdown, etc.

# Security Evaluation

STT enforces a non-interference property w.r.t speculatively accessed data:



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