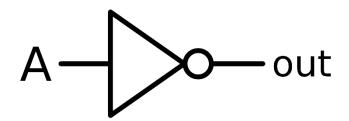
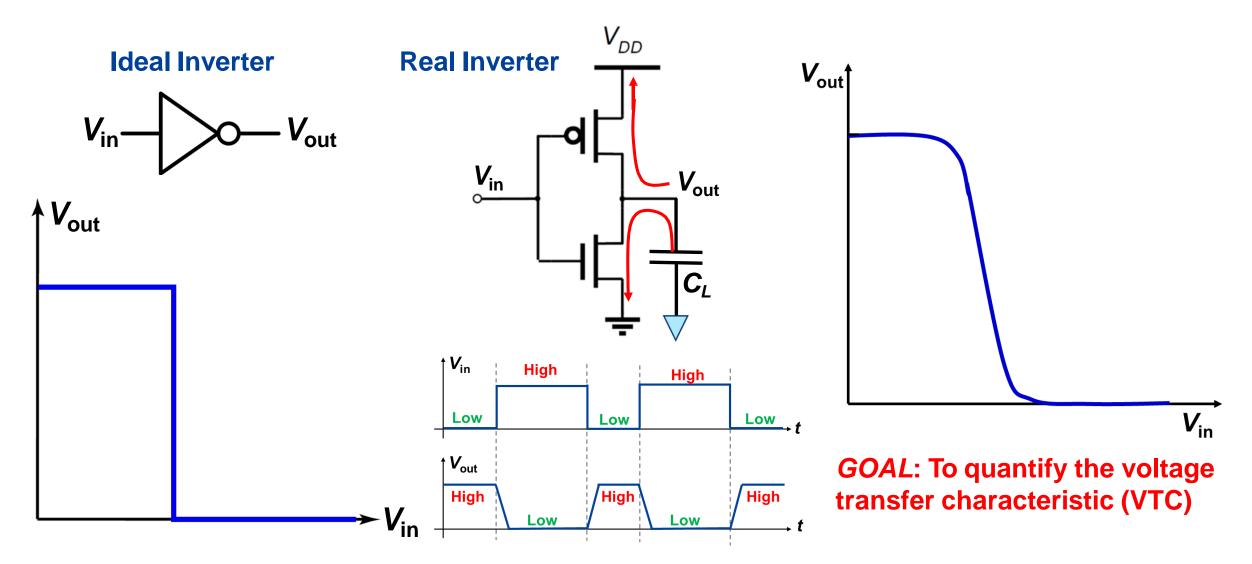
Lecture 3: Complementary Metal Oxide Semiconductor (CMOS)



Outline

- CMOS Inverter Operating Principle
 - Operating in logical high, low and transitions
- CMOS Inverter Voltage Transfer Characteristic (VTC)
 - Five operating regions
 - VTC Construction
- CMOS Inverter Reliability and Design Rules
 - Switching Threshold
 - Noise Margin 噪声容忍门限

Static CMOS Inverter



MOSFET Modes of Operation

 \Box Cutoff: $V_{GS} - V_{T} < 0$

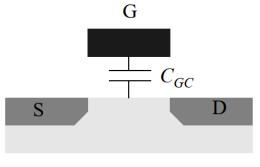
$$I_{DS} \sim 0$$

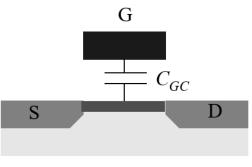
 \square Linear (Resistive): $V_{GS} - V_{T} > V_{DS}$

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \cdot [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

 \Box Current Saturation: $0 < V_{GS} - V_{T} < V_{DS}$

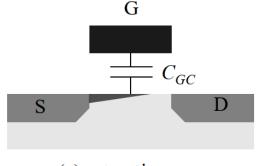
$$I_D(sat) = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$



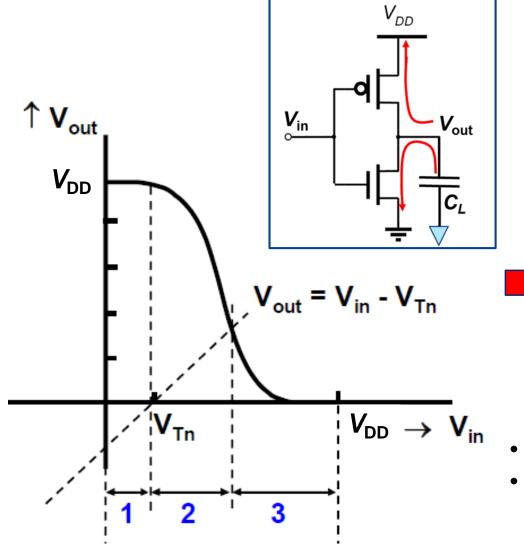


(b) resistive

- MOSFET各端的电压定义了 其工作状态。
- 因此在本章节后续的场景中可以先简单地这么理解,若MOSFET处在非关断的情况下,当 $|V_{DS}|$ 较小时,工作在Linear状态,当 $|V_{DS}|$ 较大时,工作在Saturation状态。



NMOS Operation Regions



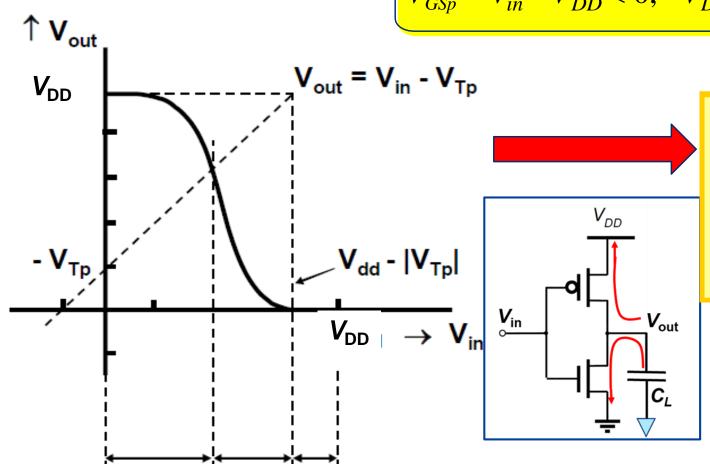
$$V_{GSn} = V_{in}, \qquad V_{DSn} = V_{out}, \qquad V_{Tn} > 0$$

NMOS

- $1 V_{
 m in} < V_{
 m Tn} \Rightarrow {
 m off}$
- 2 $V_{\rm Tn} \le V_{\rm in} \le V_{\rm out} + V_{\rm Tn}$ \Rightarrow saturation
- $V_{\rm in} > V_{\rm out} + V_{\rm Tn} \Rightarrow linear$
- V_{in} 从 低电平 -> V_{DD} , $|V_{DS}| = |V_{out}|$ 在初始时较大
- 此时NMOS首先由cut off状态,变为saturation状态,当 V_{out} 降低到一定程度后,再变为linear状态。

PMOS Operation Regions

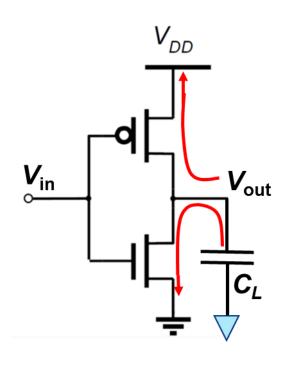
$$V_{GSp} = V_{in} - V_{DD} < 0, \quad V_{DSp} = V_{out} - V_{DD} < 0, \quad V_{Tp} < 0$$



PMOS

- $4 V_{
 m in} > V_{
 m DD} + V_{
 m Tp} \Rightarrow {
 m off}$
- 5 $V_{\mathrm{out}} + V_{\mathrm{Tp}} \le V_{\mathrm{in}} \le V_{\mathrm{DD}} + V_{\mathrm{Tp}}$ \Rightarrow saturation
- 6 $V_{\rm in} < V_{\rm out} + V_{\rm Tp} \Rightarrow {
 m linear}$
 - V_{in} 从 V_{DD} -> 低电平, $|V_{DS}| = |V_{DD} V_{out}|$ 在初始时较大。
 - 此时PMOS首先由cut off状态,变为 saturation状态,当 V_{out} 的电压升高到一 定程度后,再变为linear状态。

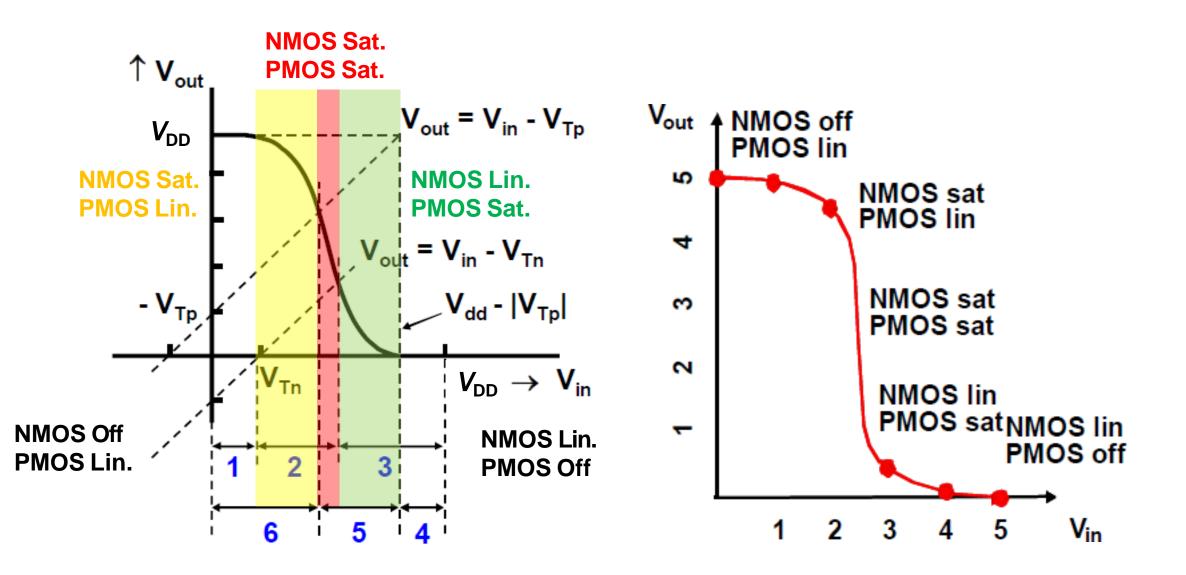
CMOS Inverter Operation Region



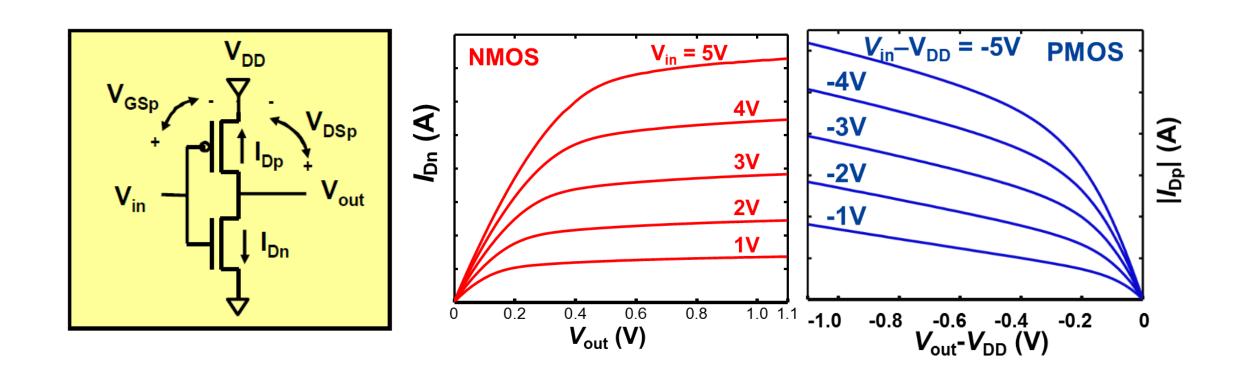
$$egin{aligned} V_{GSn} &= V_{in}, & V_{DSn} &= V_{out}, & V_{Tn} > 0, & V_{Tp} < 0 \ V_{GSp} &= V_{in} - V_{DD} < 0, & V_{DSp} = V_{out} - V_{DD} < 0 \end{aligned}$$

	Cutoff	Linear	Saturation
	<i>V</i> _{GS} < <i>V</i> _T	$ V_{GS} > V_{T} $ $ V_{DS} < V_{GS} - V_{T} $	$ V_{GS} > V_{T} $ $ V_{DS} > V_{GS} - V_{T} $
NMOS	$0 < V_{GS} < V_{Tn}$ $0 < V_{in} < V_{Tn}$	$V_{\text{Tn}} < V_{\text{in}} < V_{\text{DD}}$ $V_{\text{out}} < V_{\text{in}} - V_{\text{Tn}}$	$V_{\text{Tn}} < V_{\text{in}} < V_{\text{DD}}$ $V_{\text{out}} > V_{\text{in}} - V_{\text{Tn}}$
PMOS	V_{DD} - $ V_{Tp} $ < V_{in} < V_{DD}	$V_{\text{in}} < V_{\text{DD}} - V_{\text{Tp}} $ $V_{\text{out}} > V_{\text{in}} + V_{\text{Tp}} $	$V_{\text{in}} < V_{\text{DD}} - V_{\text{Tp}} $ $V_{\text{out}} < V_{\text{in}} + V_{\text{Tp}} $

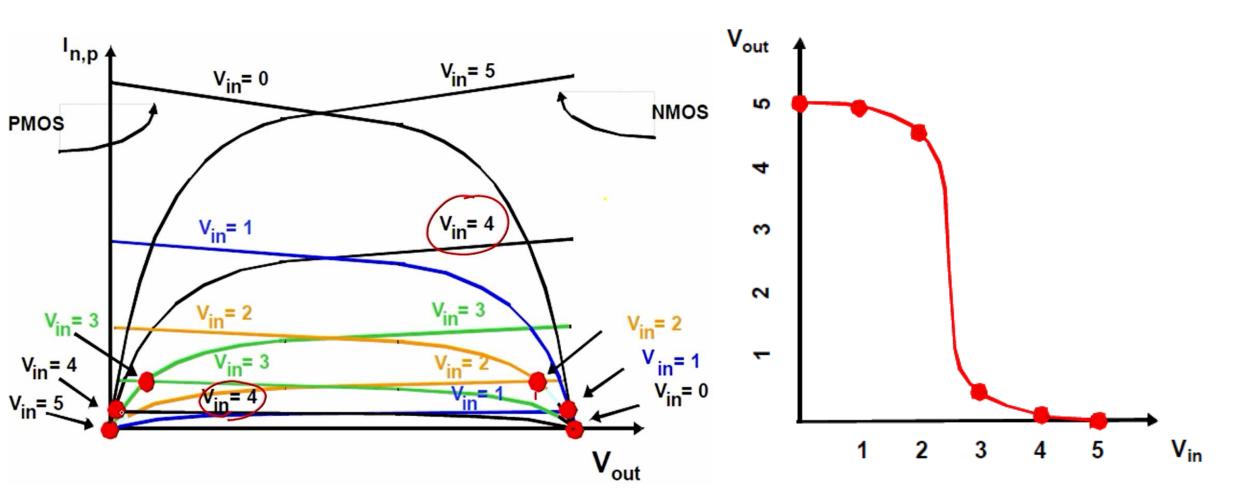
CMOS Inverter VTC



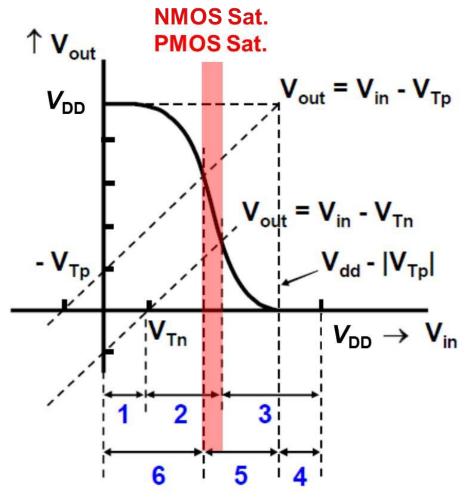
Construct the Inverter VTC



Construct the Inverter VTC



Comment on Inverter VTC



- □VTC of the CMOS inverter exhibits a very narrow transition zone;
- □In the transition region, both PMOS and NMOS are simultaneously on and in the saturation region \rightarrow large current from V_{DD} to GND.
- □In the transition region, a small change in input voltage results in a large output voltage variation → Unstable.
- □In other regions, static current can be neglected.

Comment on Inverter VTC

