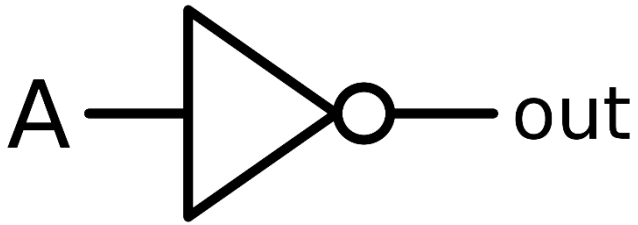
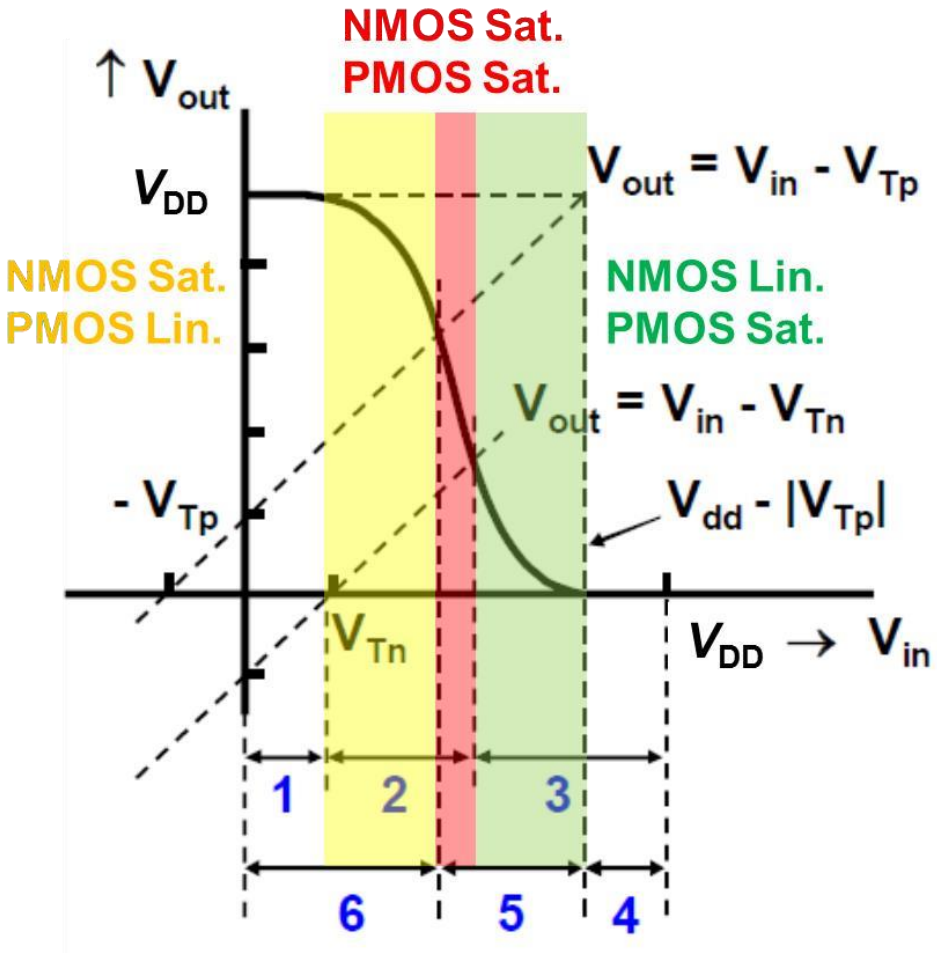
Lecture 3: Complementary Metal Oxide Semiconductor (CMOS)

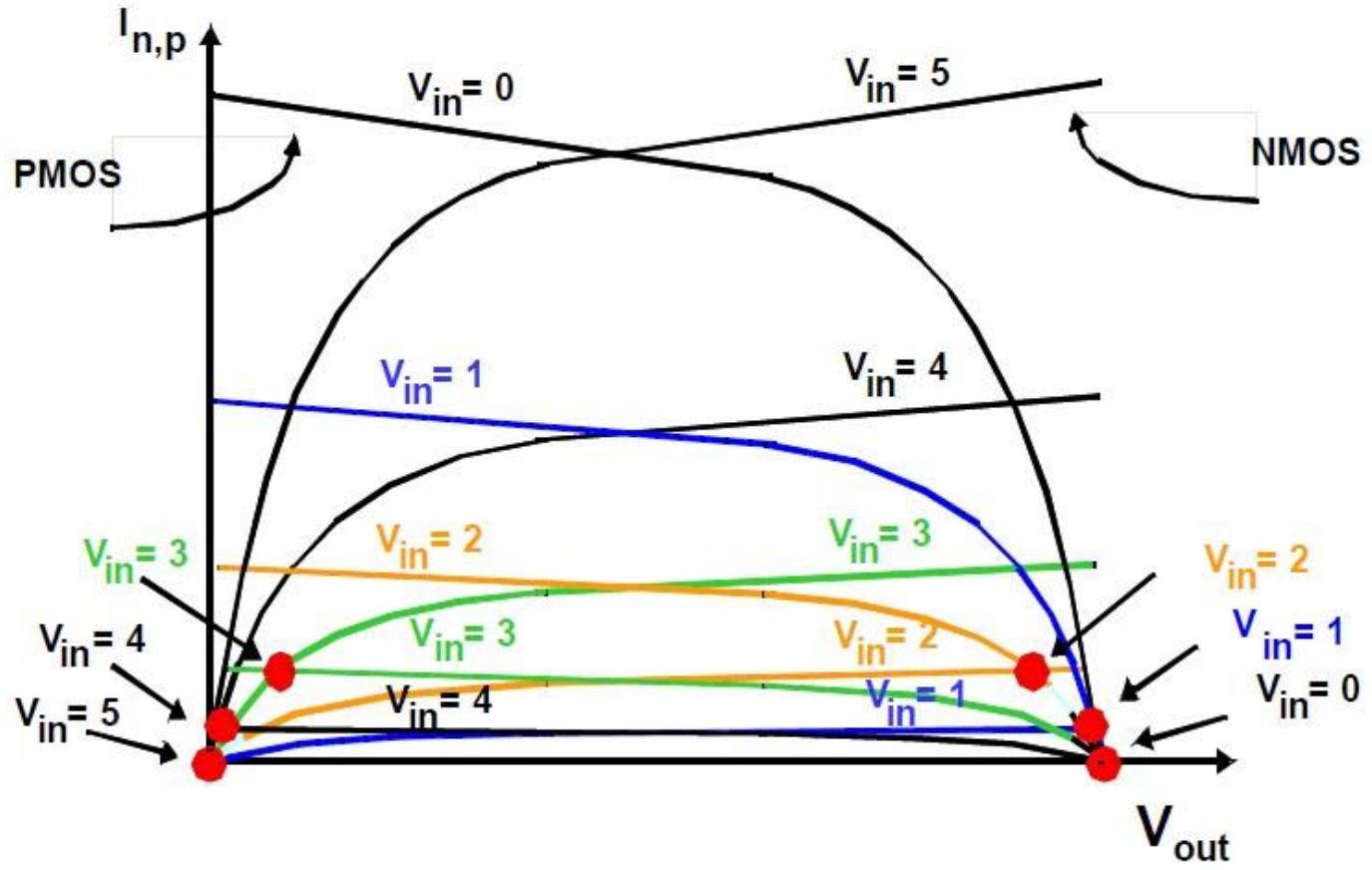


Outline

- **CMOS Inverter Operating Principle**
  - Operating in logical high, low and transitions
- **CMOS Inverter Voltage Transfer Characteristic (VTC)**
  - Five operating regions
  - VTC Construction
- **CMOS Inverter Reliability and Design Rules**
  - Switching Threshold
  - Noise Margin 噪声容忍门限

Review: Static CMOS VTC

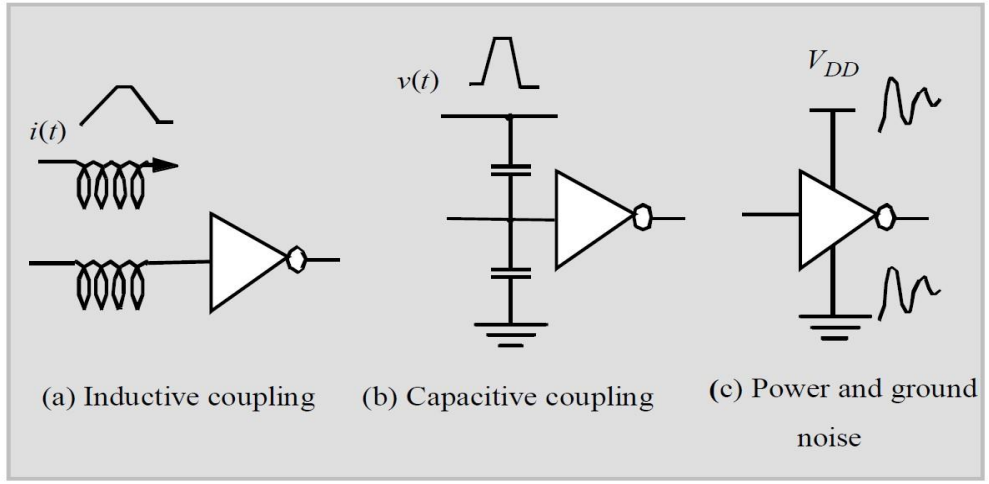


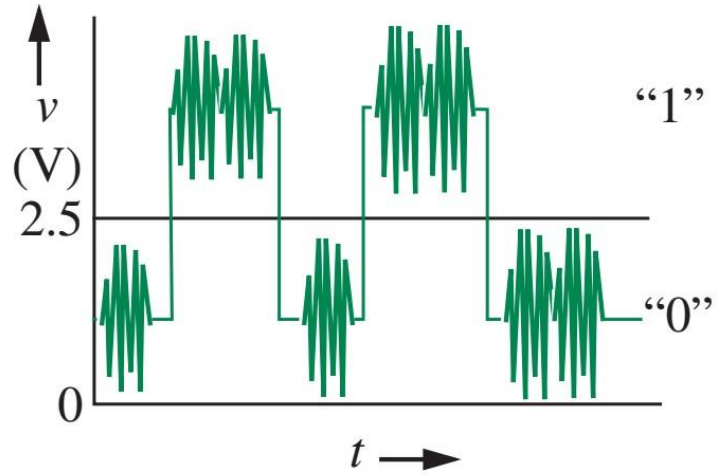


Noise in Digital ICs

- **Noise – unwanted variations of voltages and currents at the logic nodes.**

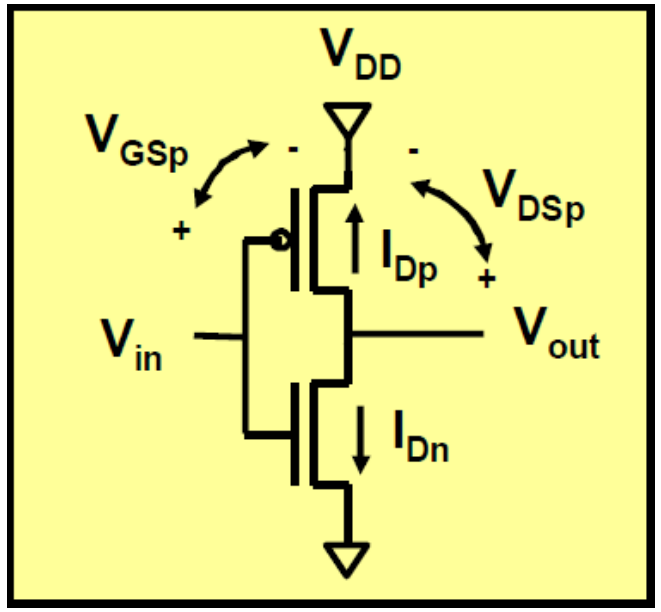
- **Digital system is one where:**
  - Analog signals are quantized to discrete values
  - All the elements (gates) can somehow reject noise
  - For sufficiently “small” noise, the system acts as if it was noise-free



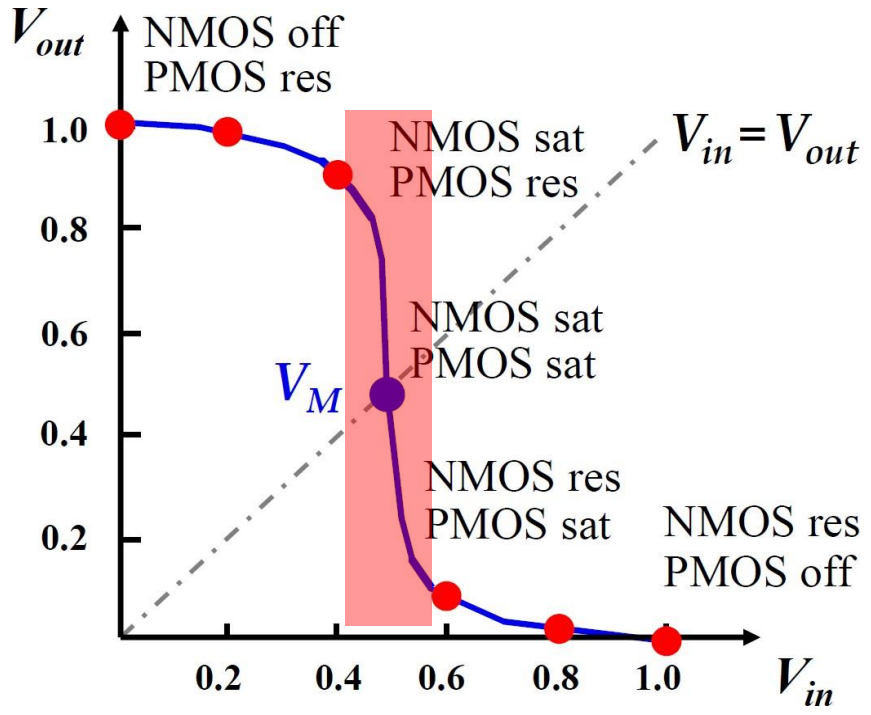


- **For large noise, the logic state may be changed!**

Switching Threshold of Inverter



- The switching threshold compares the ***relative driving strengths*** between the NMOS and PMOS
- At switching threshold: $V_{in} = V_{out} = V_M$
- $V_{DS} = V_{GS} \rightarrow$ Both PMOS & NMOS are ***saturated***



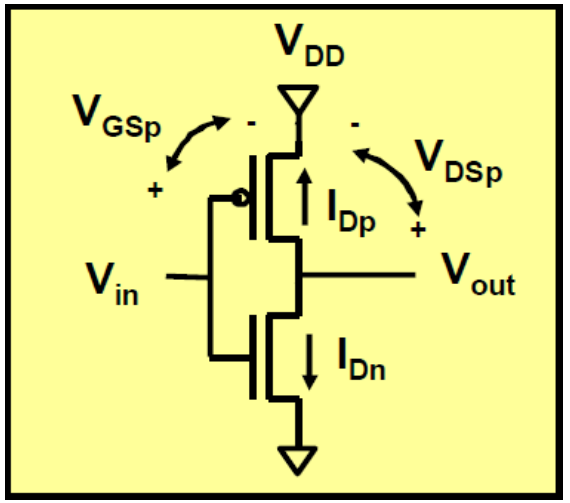
Switching Threshold Calculation

- **Apply Kirchhoff's Current Law & Velocity-Sat *I-V* Model (neglecting CLM)**

$$k_n \cdot V_{DSATn} \cdot \left(V_M - V_{Tn} - \frac{V_{DSATn}}{2} \right) + k_p \cdot V_{DSATp} \cdot \left(V_M - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2} \right) = 0$$

$$k_n = \mu_n C_{ox} \frac{W_n}{L} \qquad I_{Dn}$$

$$k_p = \mu_p C_{ox} \frac{W_p}{L} \qquad -I_{Dp}$$



- **Solving for V_M**

$$V_M = \frac{(V_{Tn} + \frac{V_{DSATn}}{2}) + r(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2})}{1 + r}$$

$$r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{v_{satp} W_p}{v_{satn} W_n}$$

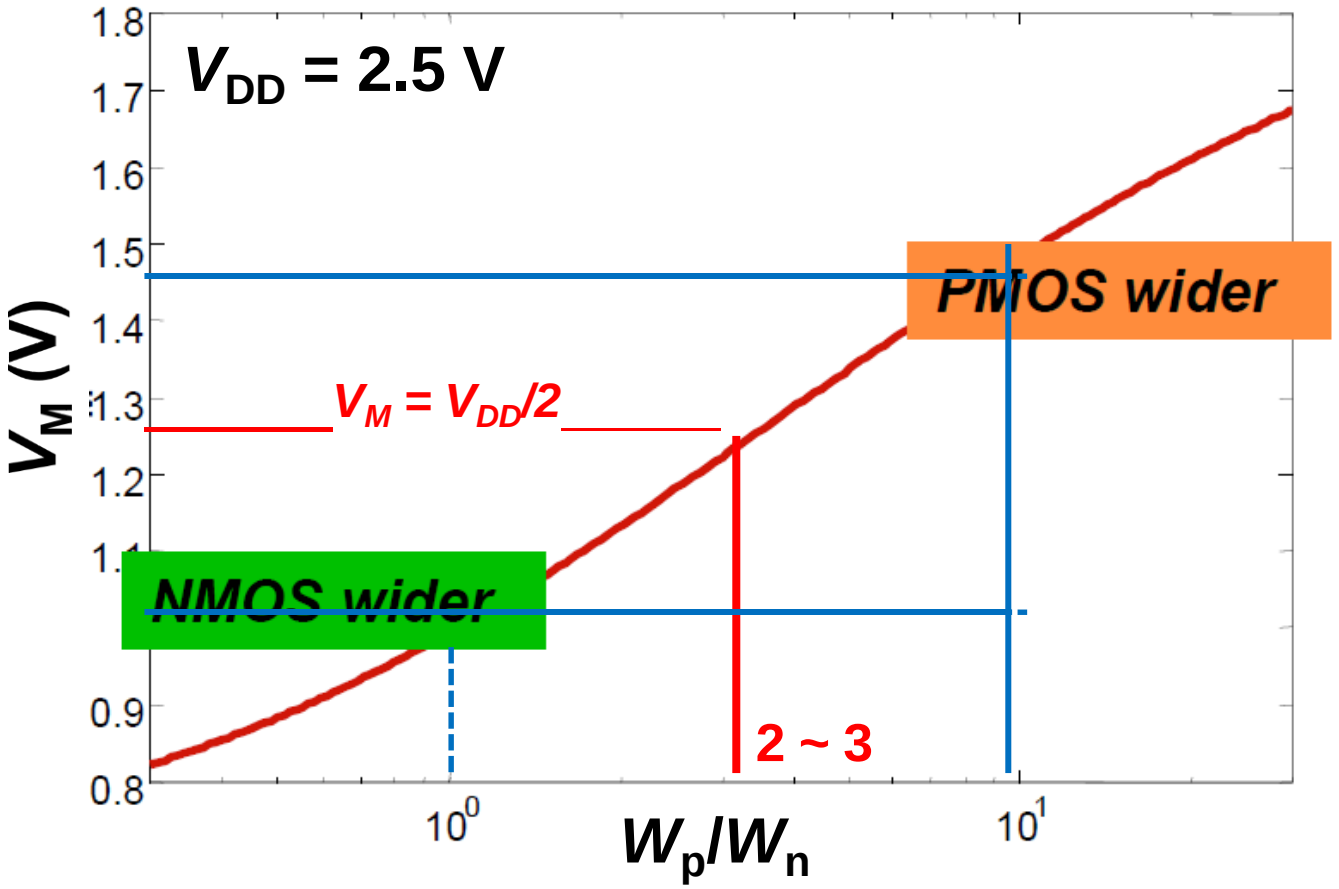
Key: $v_{sat} = \mu \cdot V_{DSAT}/L$

- **For large V_{DD}**

$$V_M \approx \frac{r V_{DD}}{1 + r}$$

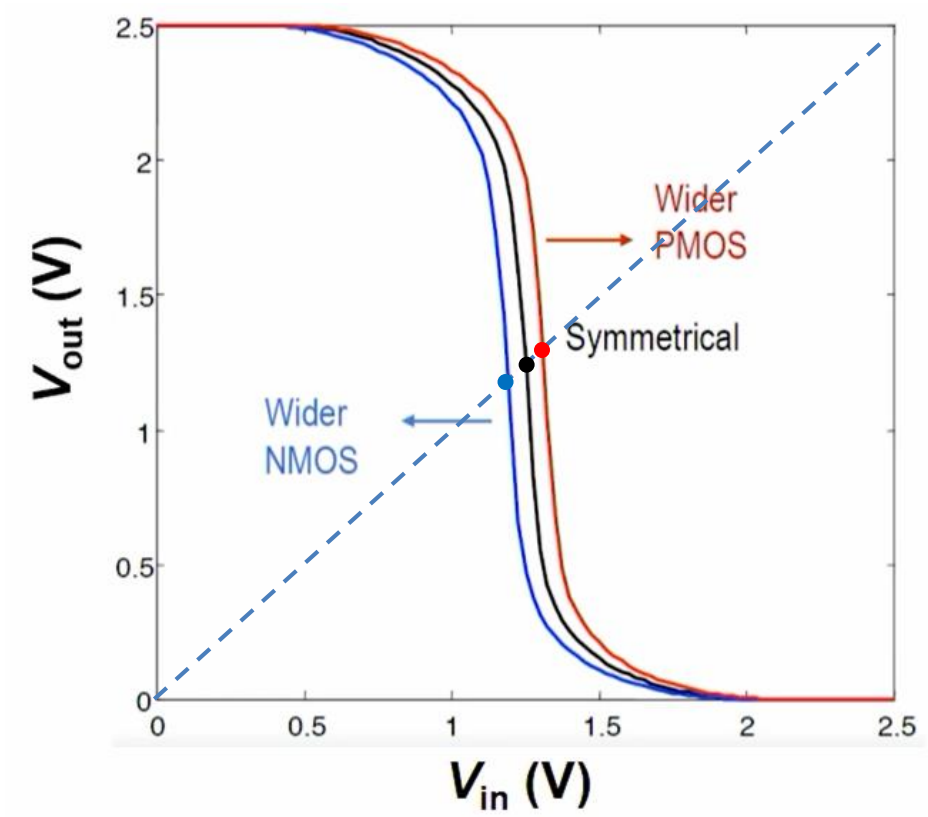
V_M can be controlled by transistor size!

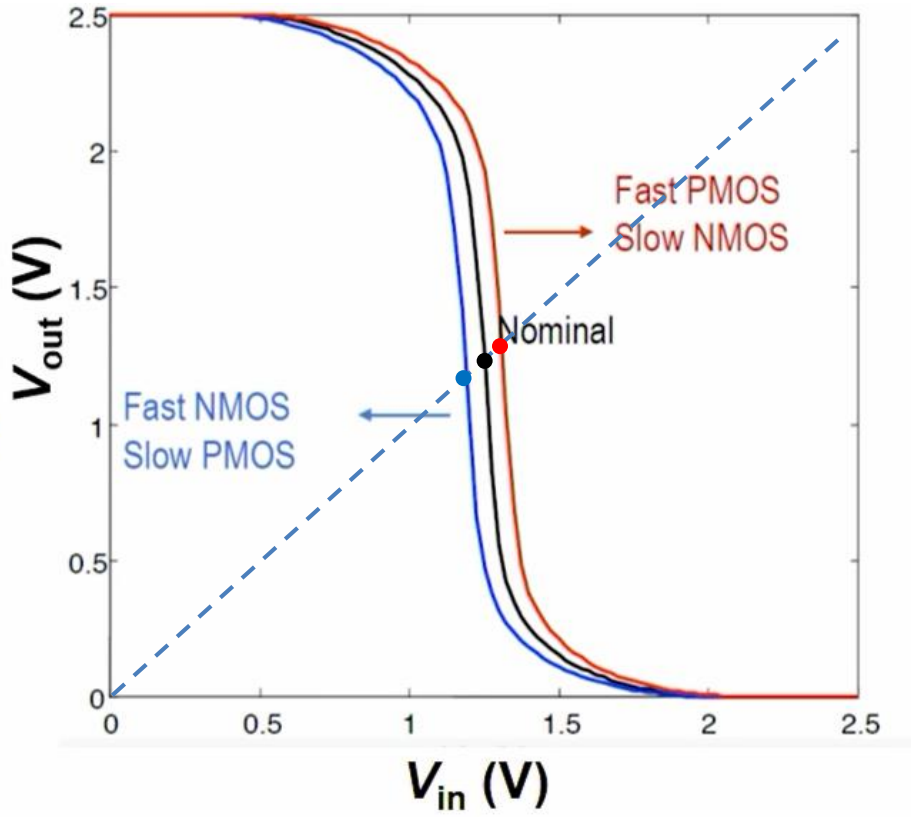
Real Case Switching Threshold Variation



- Increasing the width of PMOS moves V_M towards V_{DD} whereas increasing the width of NMOS moves V_M towards GND
- To make $V_M = V_{DD}/2$, we need to choose a wider PMOS.

Impact of Process Variations



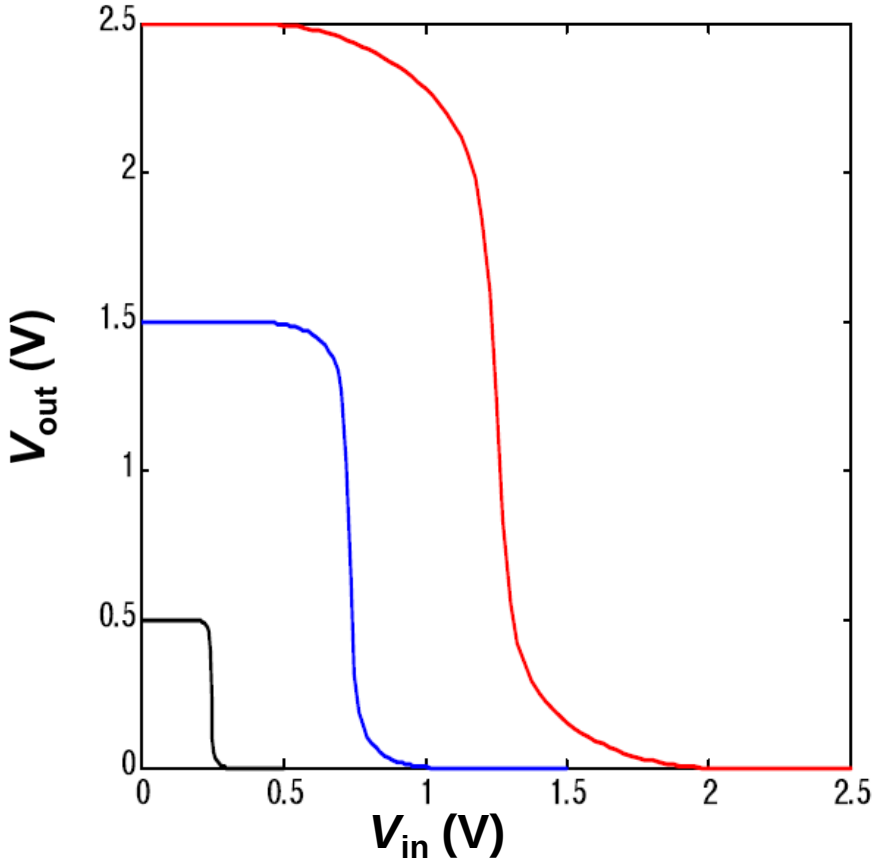


***r* decreases**
Strong NMOS

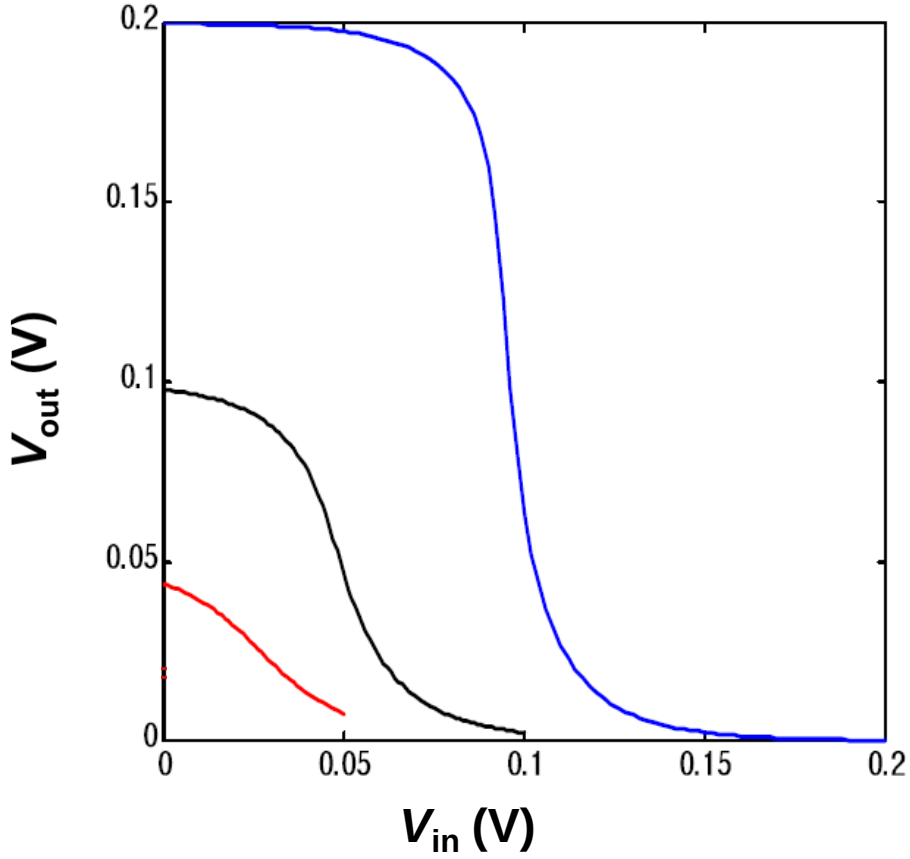
$$r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{v_{satp} W_p}{v_{satn} W_n}$$

***r* increases**
Strong PMOS

Impact of Supply Voltage V_{DD}



Large Supply Voltage

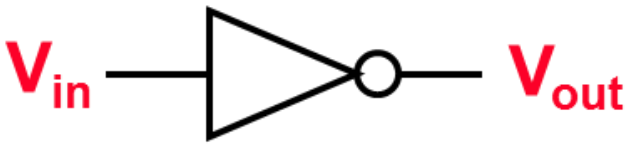


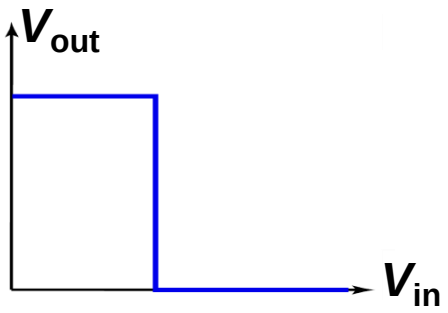
Small Supply Voltage

Noise Rejection

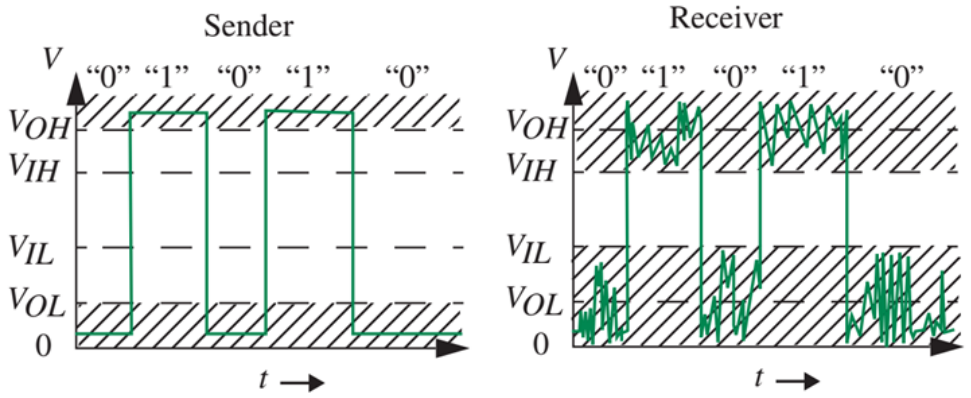
- To see if a gate rejects noise
  - Look at its DC voltage transfer characteristic (VTC)
  - See what happens when input is not exactly 1 or 0

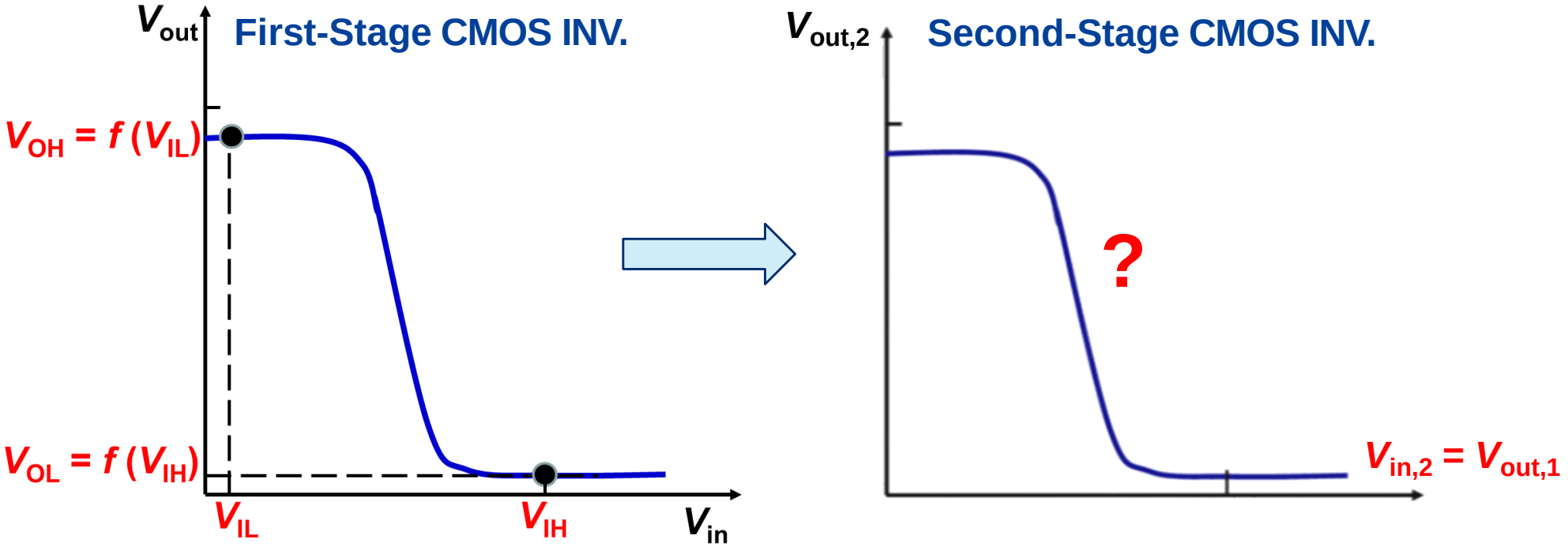
- Ideal digital gate:
  - Noise needs to be larger than $V_{DD}/2$ to have any effect on gate output



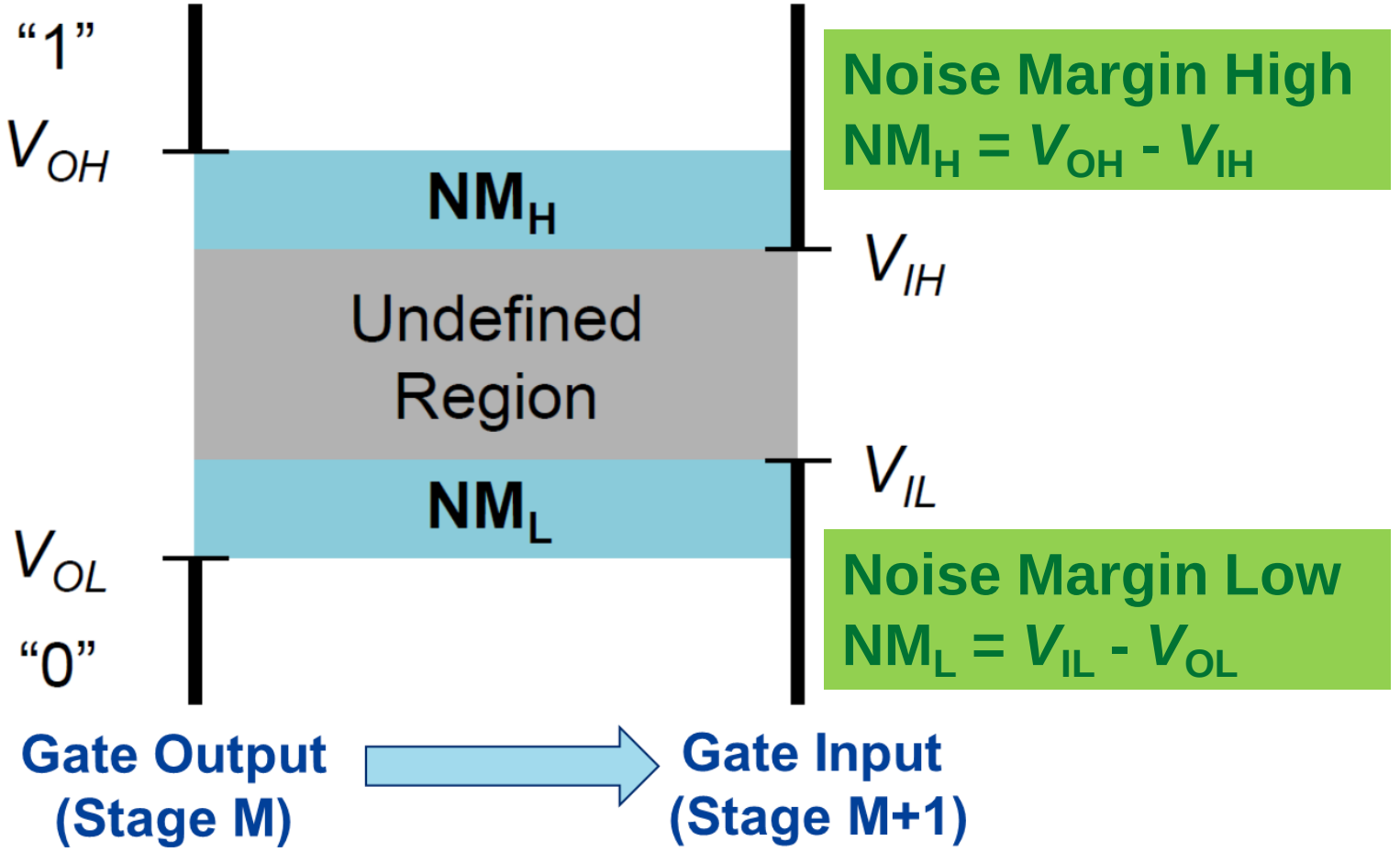


DC Operation – More Realistic VTC

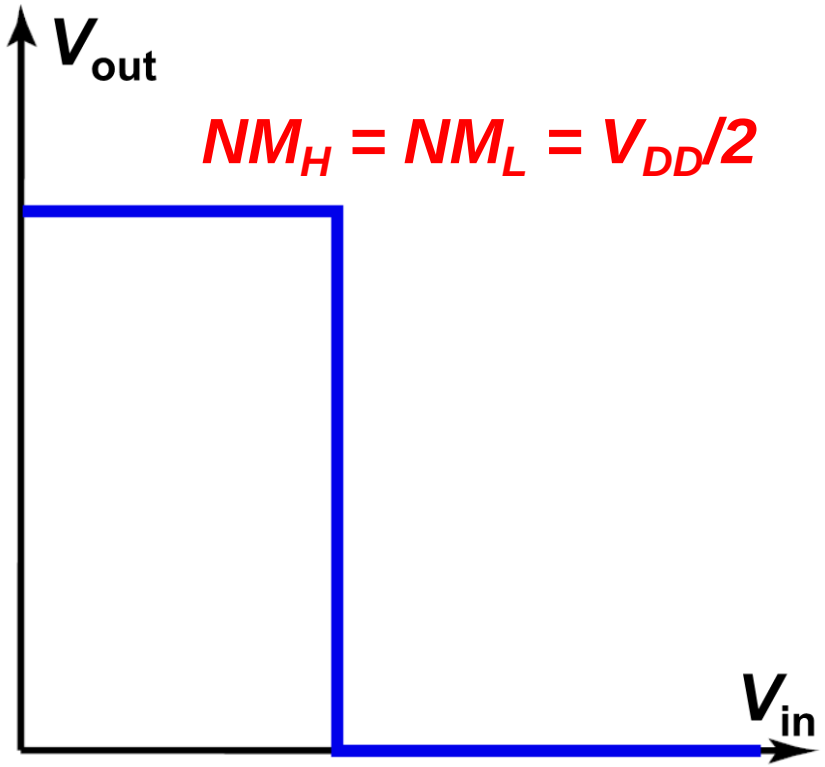


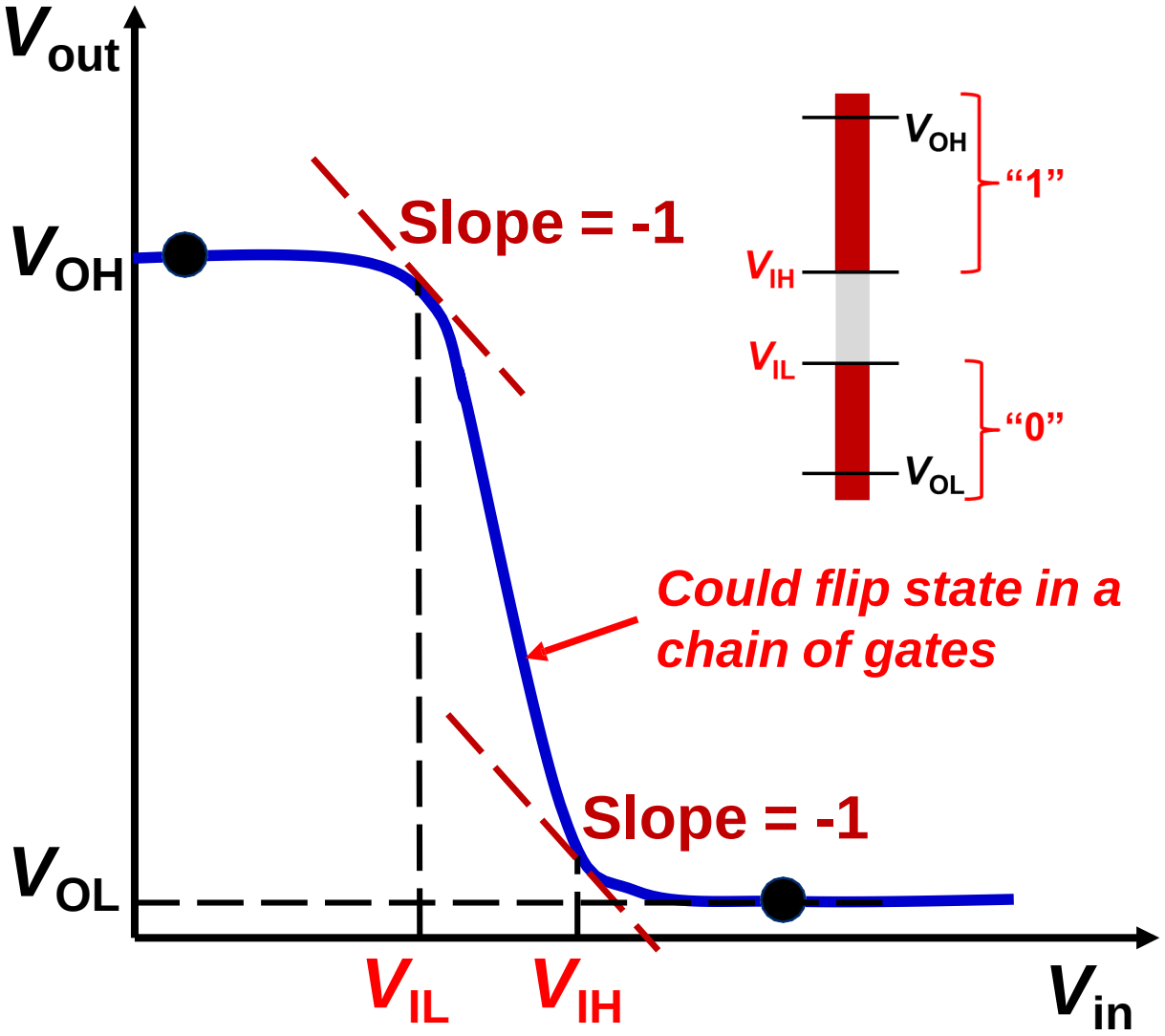


Noise Margin



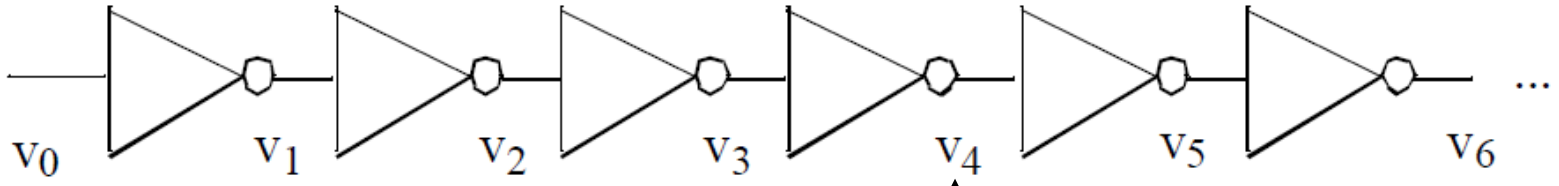
Ideal Case vs. Real Case

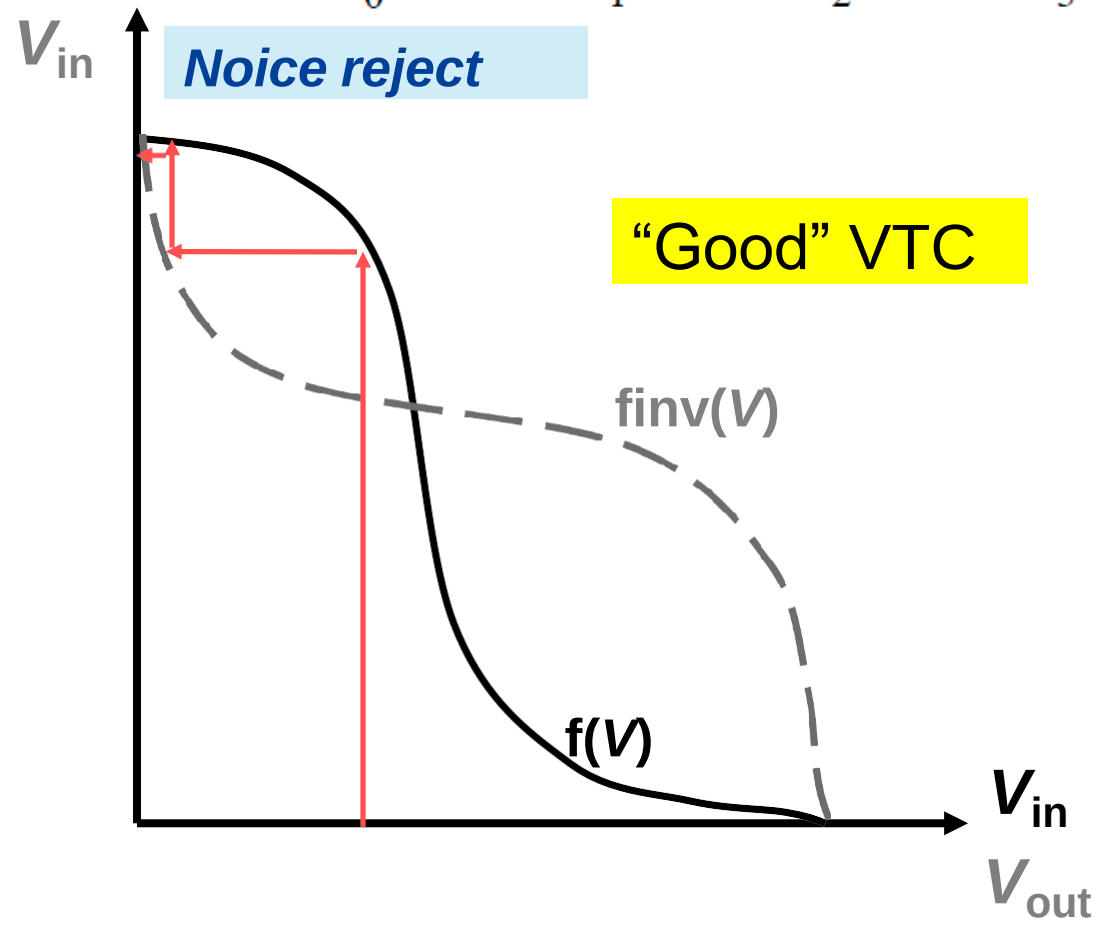


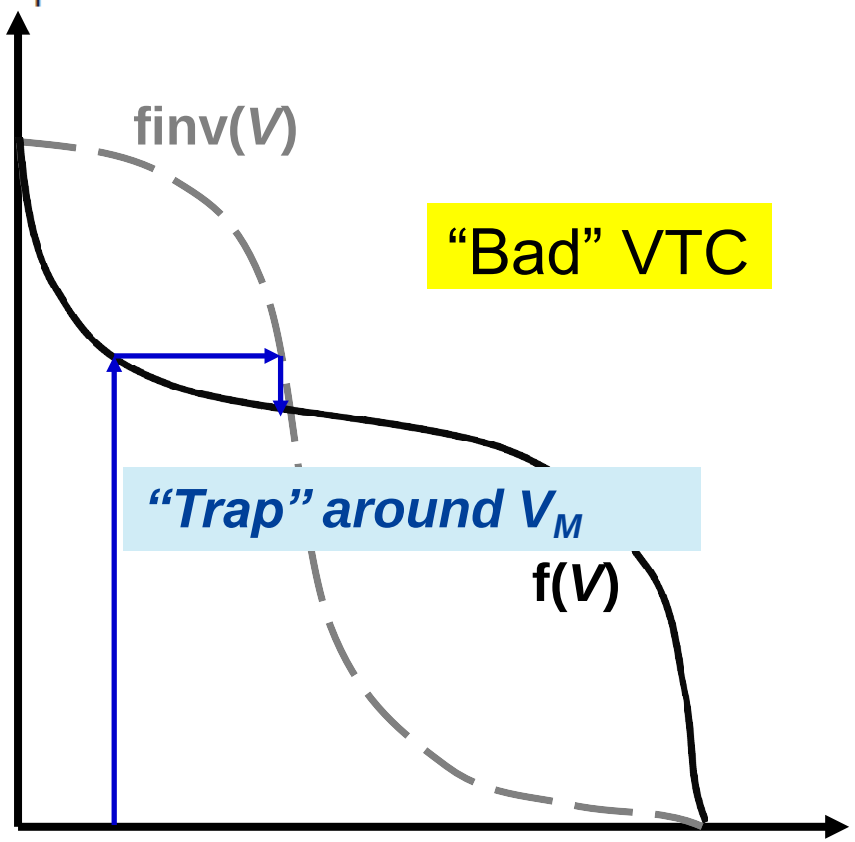


Noise Rejection of Inverter Chain

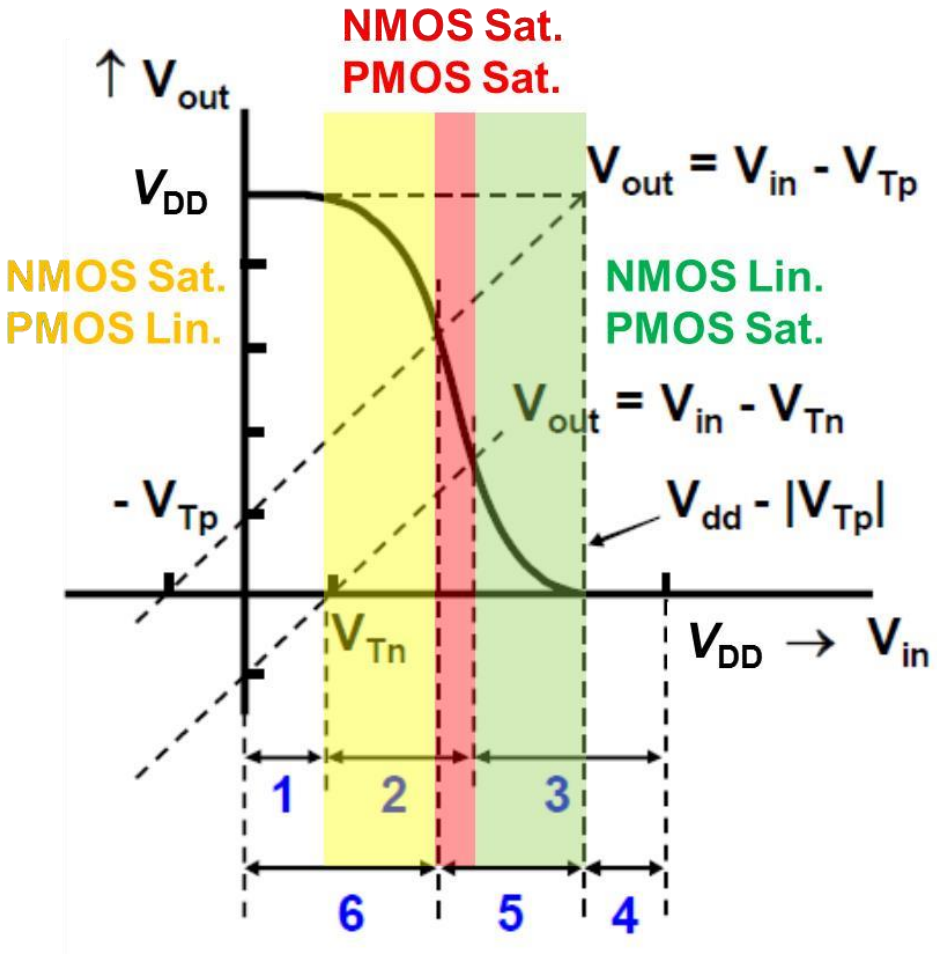
- A chain of inverters







Summary of Static CMOS Inverter



- Static CMOS inverter is the simplest logic gate for digital integrated circuit design.
- VTC of static CMOS inverter is obtained by analyzing the operation regions of NMOS & PMOS.
- Region 1 and region 4 are ideal operation regions.
- static CMOS inverter serves as the building block for static CMOS logic gates.