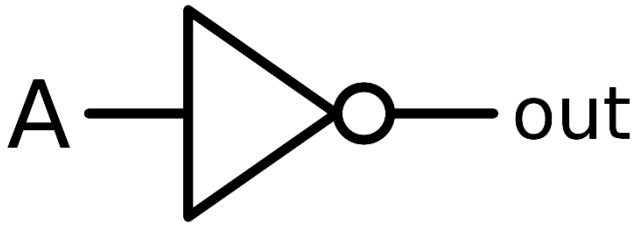
Lecture 3: Complementary Metal Oxide Semiconductor (CMOS)

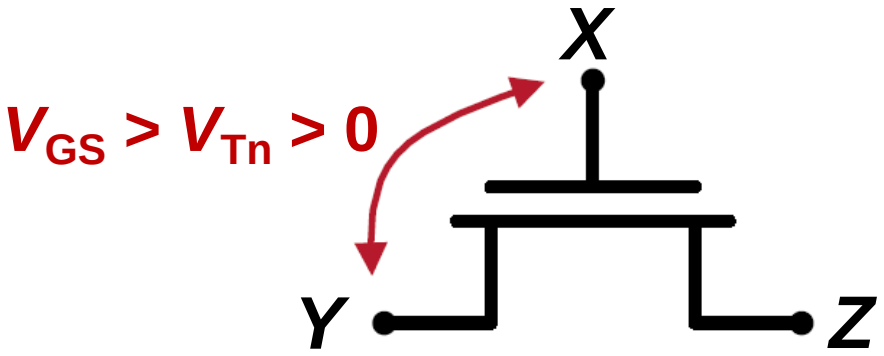


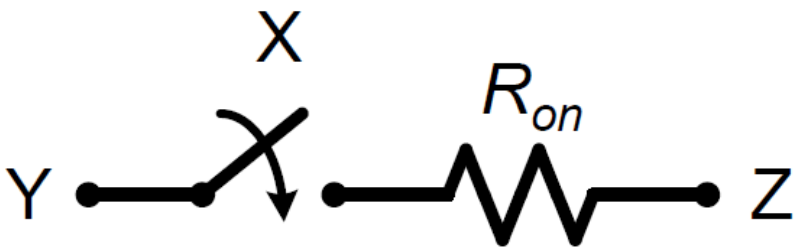
Outline

- **CMOS Inverter Operating Principle**
  - Operating in logical high, low and transitions
- **CMOS Inverter Voltage Transfer Characteristic (VTC)**
  - Five operating regions
  - VTC Construction
- **CMOS Inverter Reliability and Design Rules**
  - Switching Threshold
  - Noise Margin 噪声容忍门限

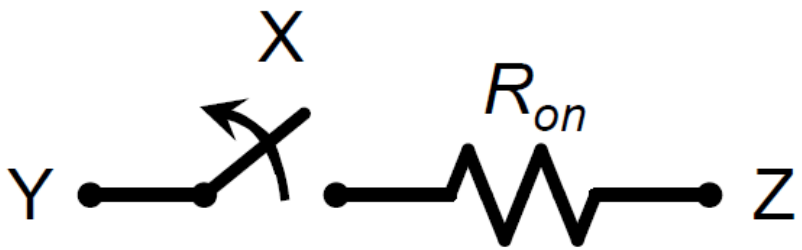
Review: Switch Model of MOSFET

NMOS Transistor



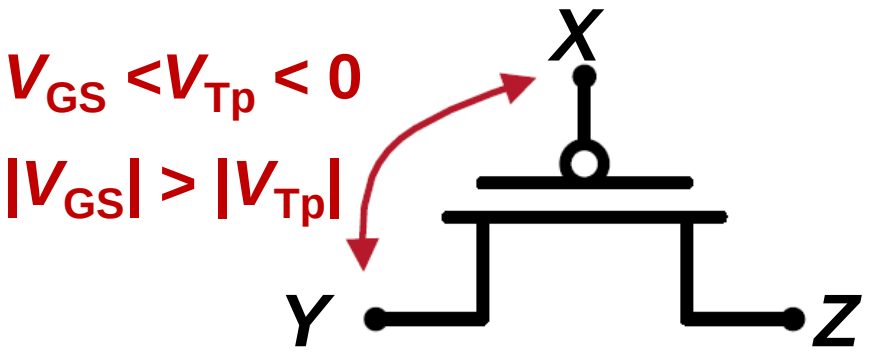


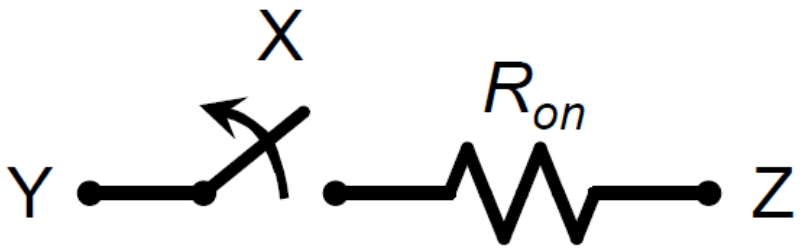
Y=Z if X=1



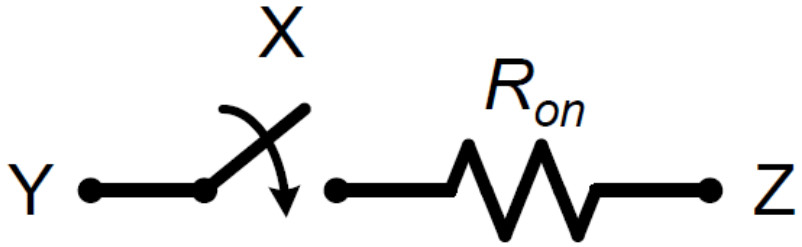
Y≠Z if X=0

PMOS Transistor



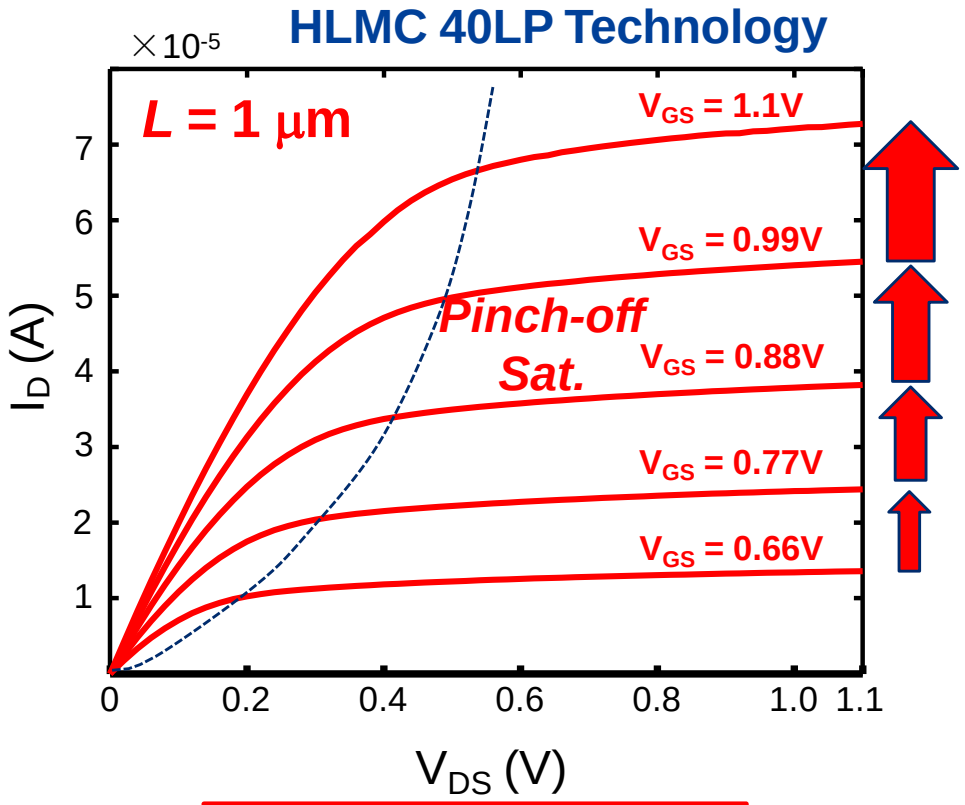


Y≠Z if X=1



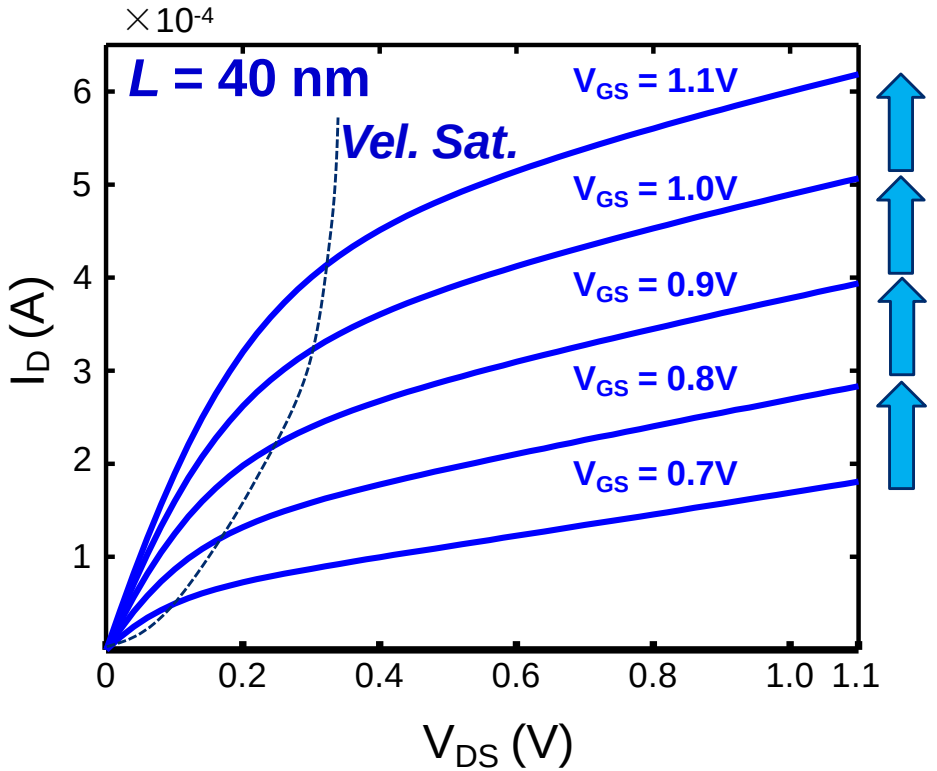
Y=Z if X=0

Review: *I-V* Curve of MOSFET



$$I_D(sat) = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

Long-Channel MOSFET
Pinch-Off Saturation



$$I_{DSAT} = v_{sat} \cdot C_{ox} \cdot W \cdot [V_{GS} - V_T - V_{DSAT}]$$

Short-Channel MOSFET
Velocity Saturation

Review: MOSFET Unified Model

$$V_{GT} = V_{GS} - V_T$$

- **Active region ($V_{GT} \geq 0$) Lin, Sat, V-Sat**

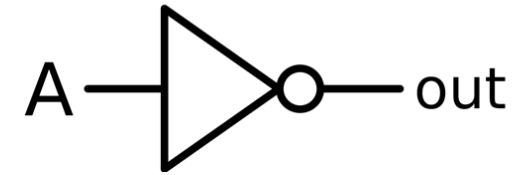
$$I_{DS} = \mu_n C_{ox} \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{\min} - \frac{V_{\min}^2}{2}\right) \cdot (1 + \lambda V_{DS})$$

$$V_{\min} = \min\left(V_{DS},\ V_{GT},\ V_{DSAT}\right)$$

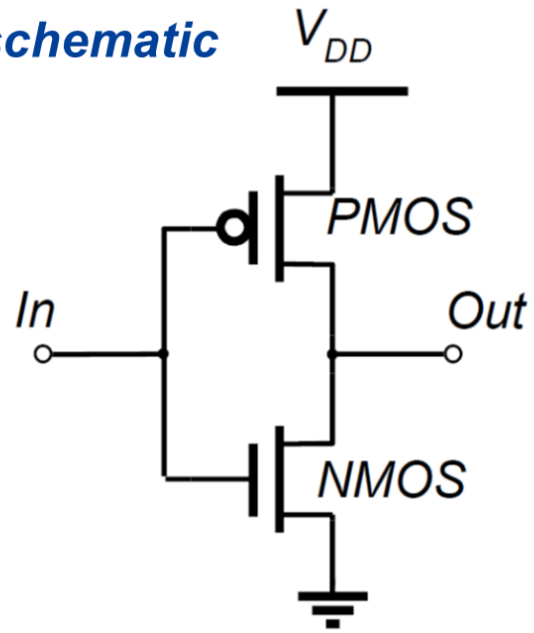
Lin Sat V-Sat

The CMOS Inverter

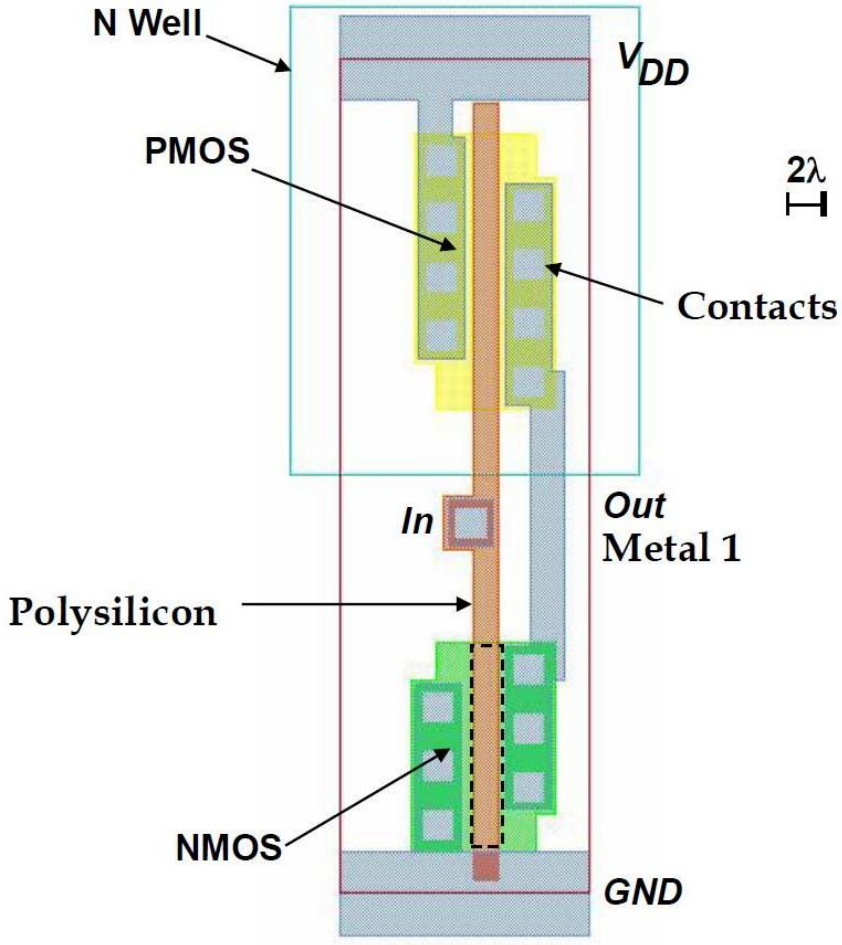
symbol



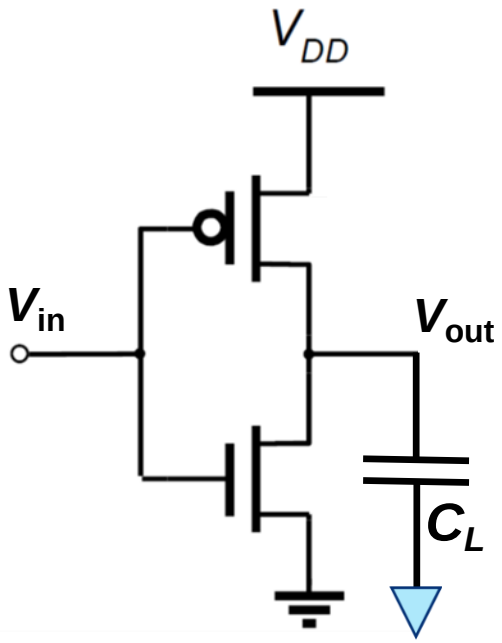
schematic



layout



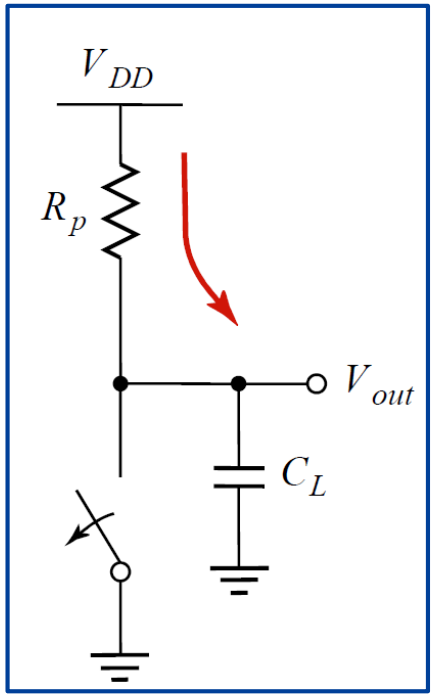
CMOS Inverter Operational Principle



$V_{in} = 0$

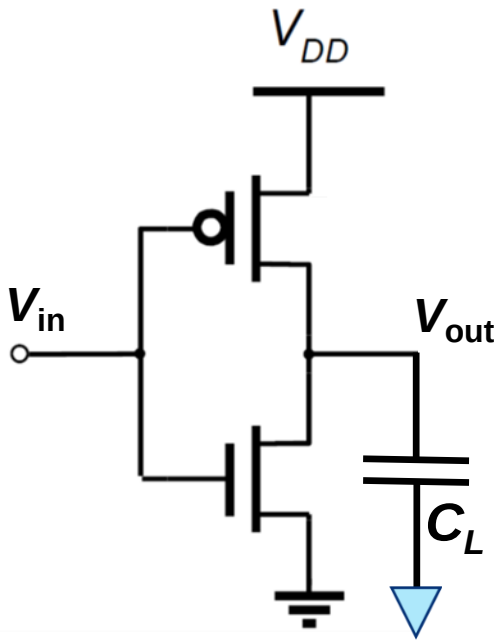
$V_{GSn} = V_{in} = 0 \rightarrow$ NMOS OFF

$|V_{GSp}| = V_{DD} - V_{in} > |V_{Tp}| \rightarrow$ PMOS ON



- The output is connected to V_{DD} through a low-impedance path.
- The equivalent circuit is an RC circuit.
- In steady state, $V_{out} = V_{DD}$, $V_{DSp} = 0$, NMOS OFF, PMOS in deep linear region, no static current.

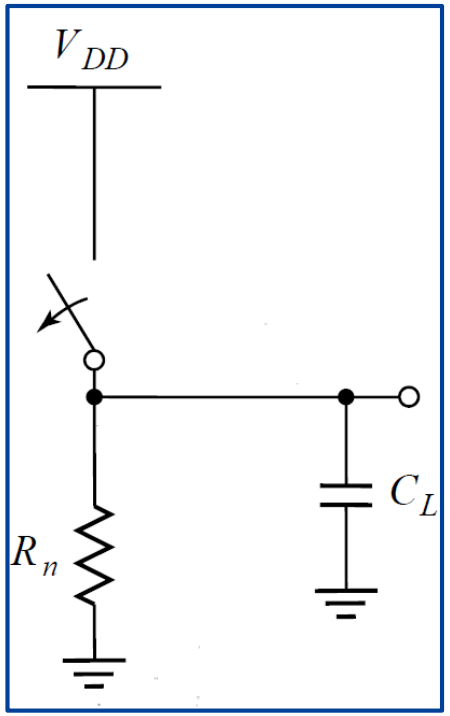
CMOS Inverter Operational Principle



$V_{in} = V_{DD}$

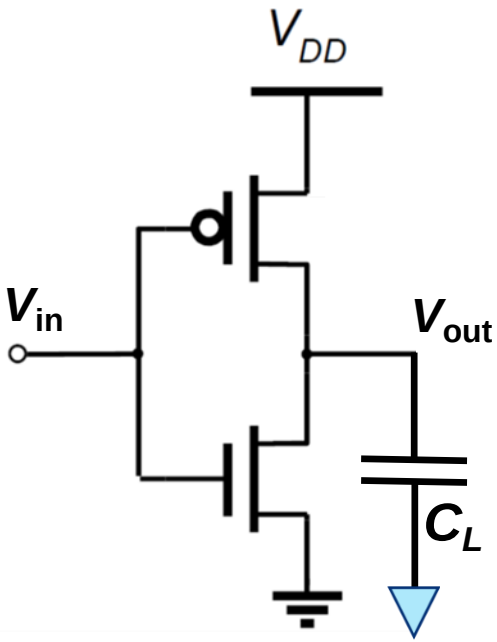
$V_{GSn} = V_{DD} > V_{Tn} \rightarrow$ NMOS ON

$|V_{GSp}| = V_{DD} - V_{DD} = 0 \rightarrow$ PMOS OFF

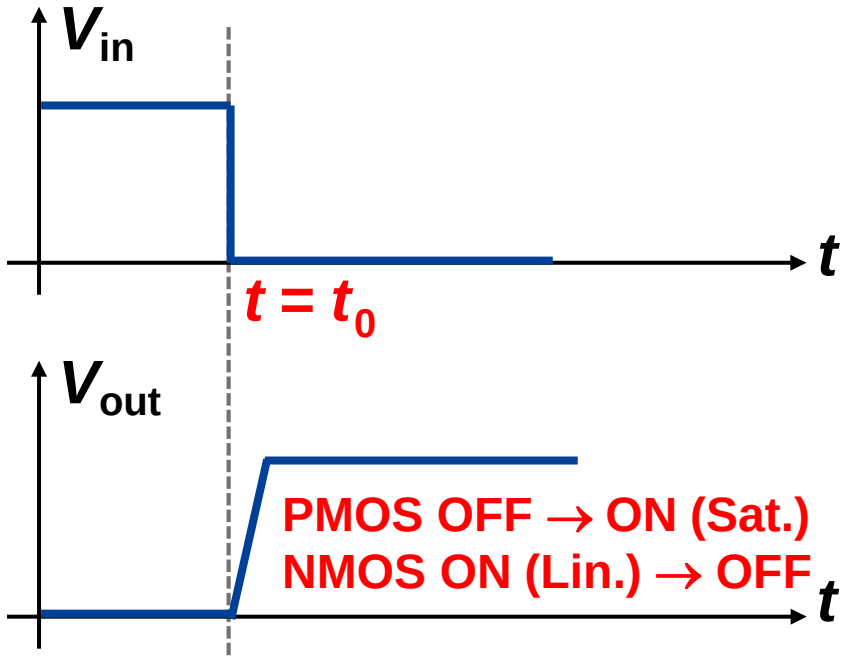


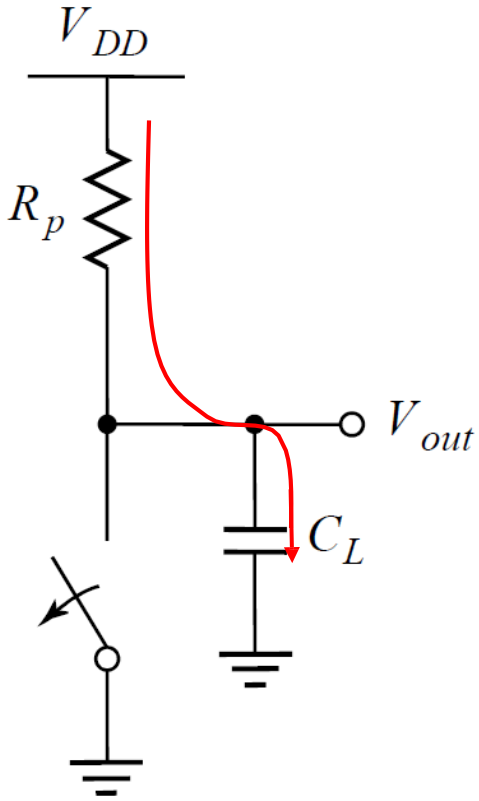
- The output is connected to GND through a low-impedance path.
- The equivalent circuit is an RC circuit.
- In steady state, $V_{out} = 0$, $V_{DSn} = 0$, PMOS OFF, NMOS in deep linear region, no static current.

CMOS Inverter Operational Principle



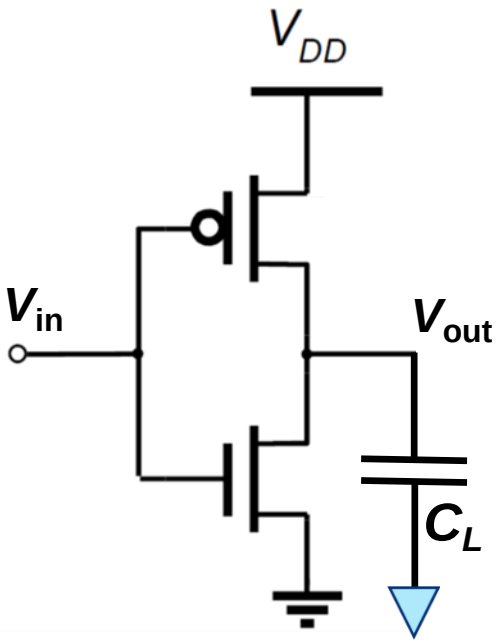
$V_{in} = V_{DD} \rightarrow 0$



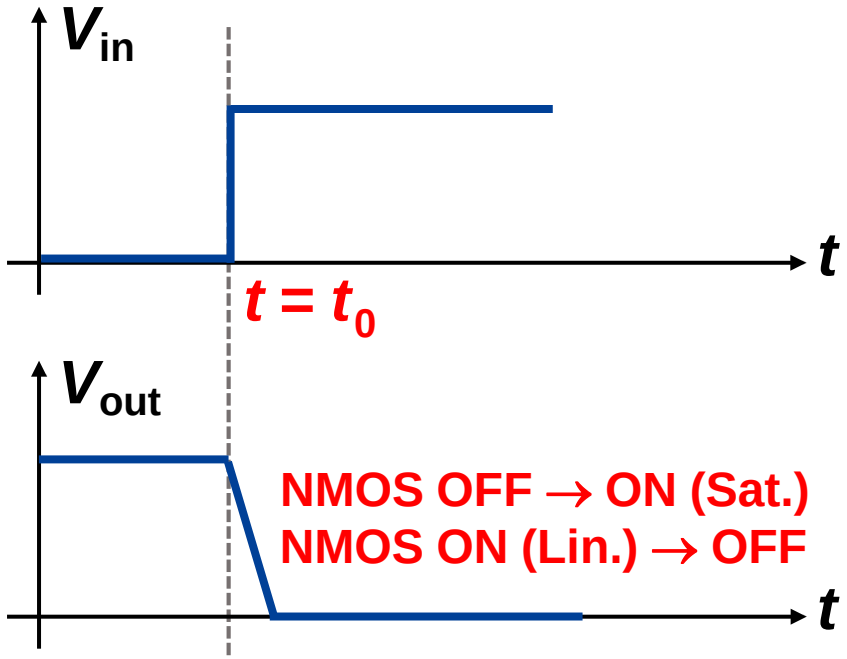


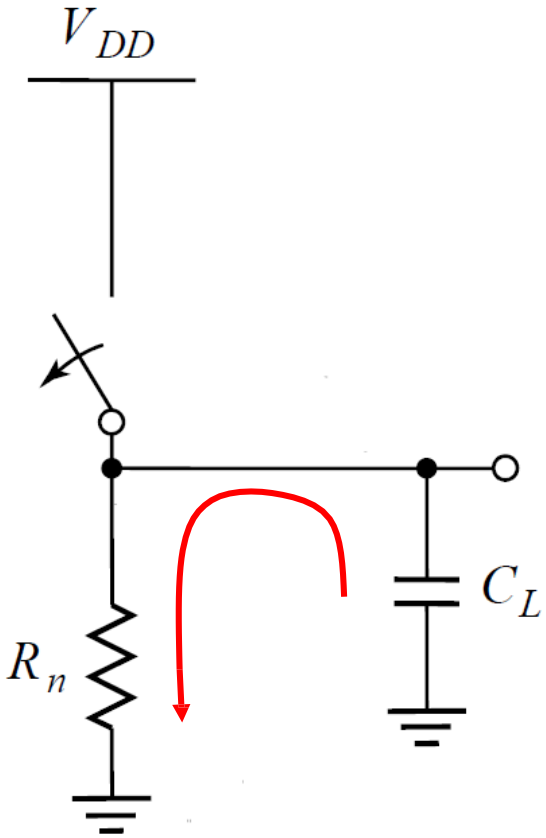
- The V_{DD} charges the output through PMOS → Pull-Up Process.
- Finally, $V_{out} = 0 \rightarrow V_{DD}$.

CMOS Inverter Operational Principle



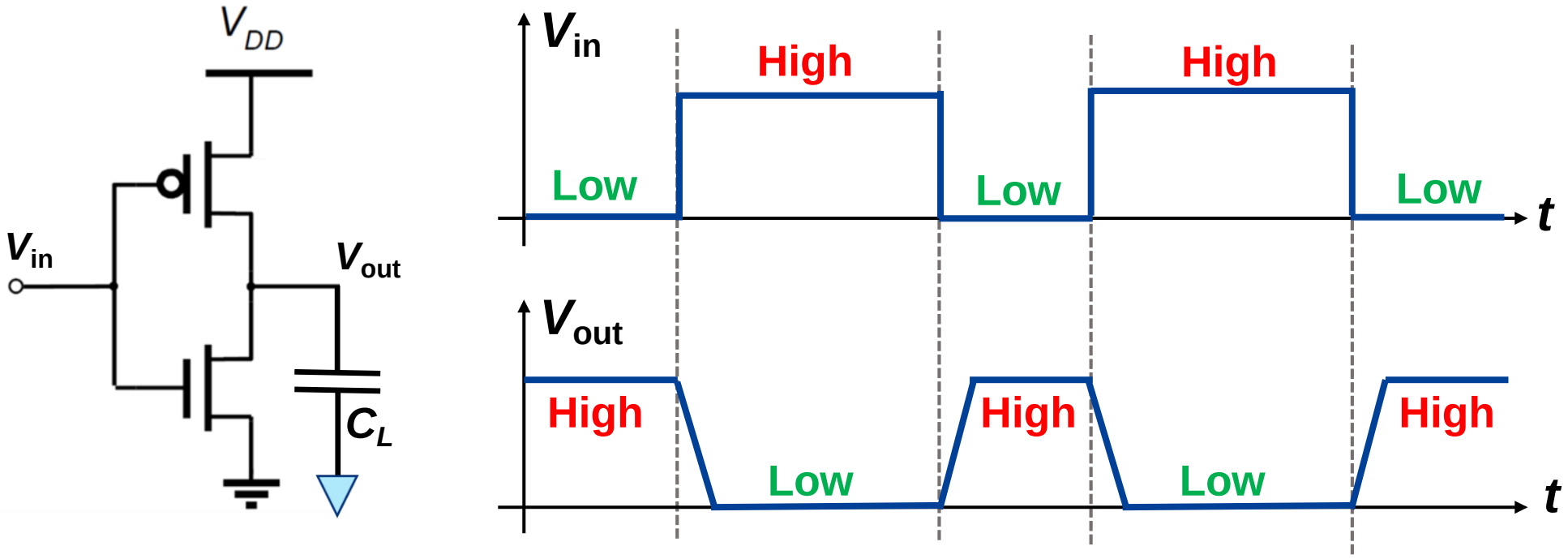
$V_{in} = 0 \rightarrow V_{DD}$





- The output discharges through NMOS to GND → Pull-Down Process.
- Finally, $V_{out} = V_{DD} \rightarrow 0$.

CMOS Inverter Operational Principle



- The Inversion function is realized → CMOS Inverter.
- Rather than directly connect output, input controls the on/off of MOSFET and charge/discharge of capacitance

Ideal Static CMOS Properties

- **Full rail-to-rail swing.**
  - **$V_{OL} = 0$, $V_{OH} = V_{DD}$**
- **Logic levels independent on transistor size.**
  - ***"Ratio-less"* logic**
- **Low output impedance (kΩ range).**
- **High input impendence (~∞).**
- **No direct-path current in steady state.**
  - ***No static power dissipation***