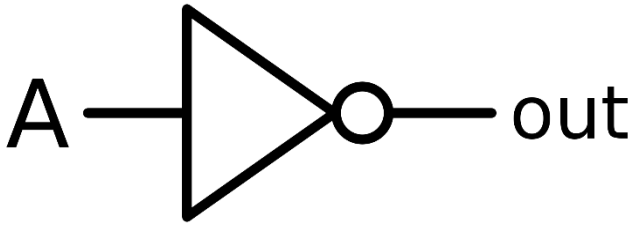
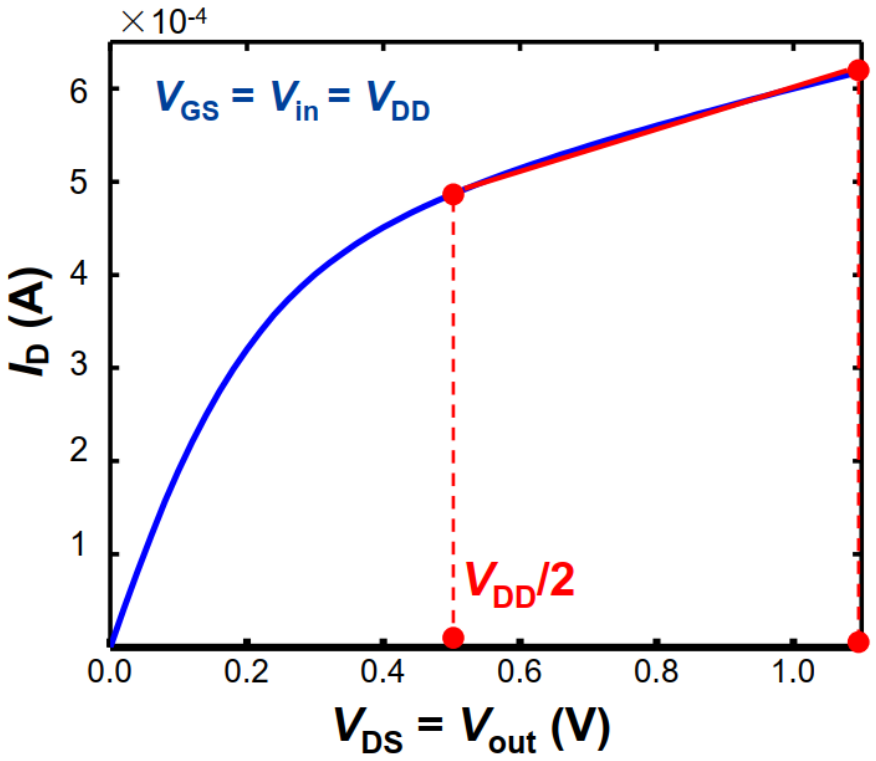
Lecture 4: CMOS Inverter Physical Characteristics



Outline

- **CMOS Inverter Equivalent Resistance and Capacitance**
  - Resistance vs. V_{DD}
  - Capacitance of Logic Circuit
- **CMOS Inverter Propagation Delay**
  - Delay vs. Resistance & Capacitance
  - Miller Theorem and C_{GD}
- **CMOS Inverter Power Consumption**
  - Static & Dynamic power
  - Switching Power Consumption
  - Short-circuit Power Consumption

Review: Equivalent Resistance



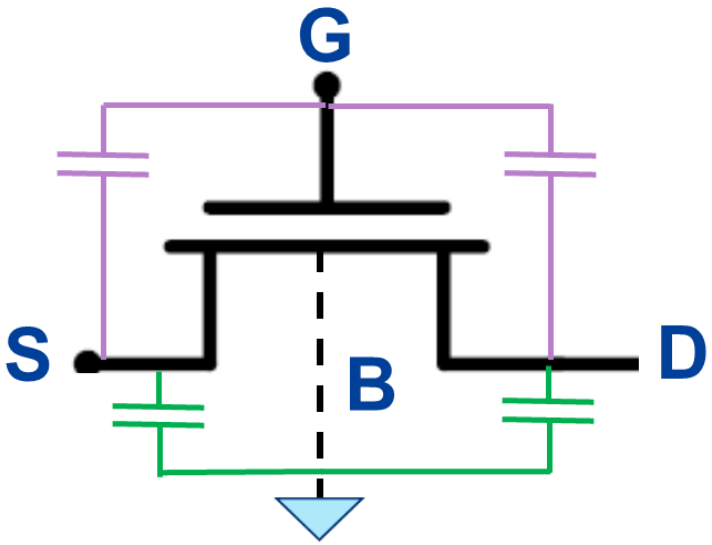
- **Method 1: Integration**

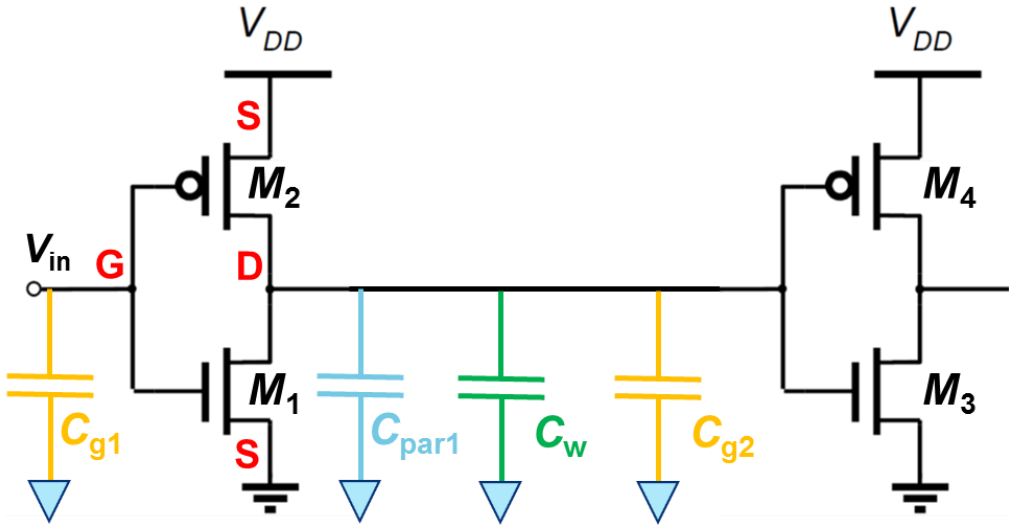
$$R_{on} = \frac{1}{-V_{DD}/2}\int_{V_{DD}}^{V_{DD}/2} \frac{V}{I_{DSAT}\cdot(1+\lambda V)}dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}(1-\frac{7}{9}\lambda V_{DD})$$

- **Method 2: Averaging**

$$R_{on} = \frac{1}{2}(\frac{V_{DD}}{I_{DSAT}\cdot(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}\cdot(1+\lambda V_{DD}/2)}) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}(1-\frac{5}{6}\lambda V_{DD})$$

Review: Capacitance of MOSFET

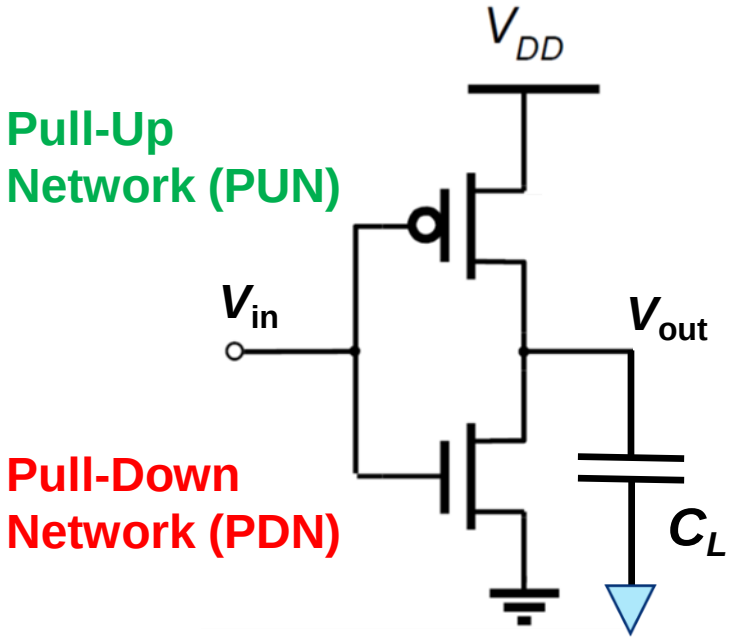


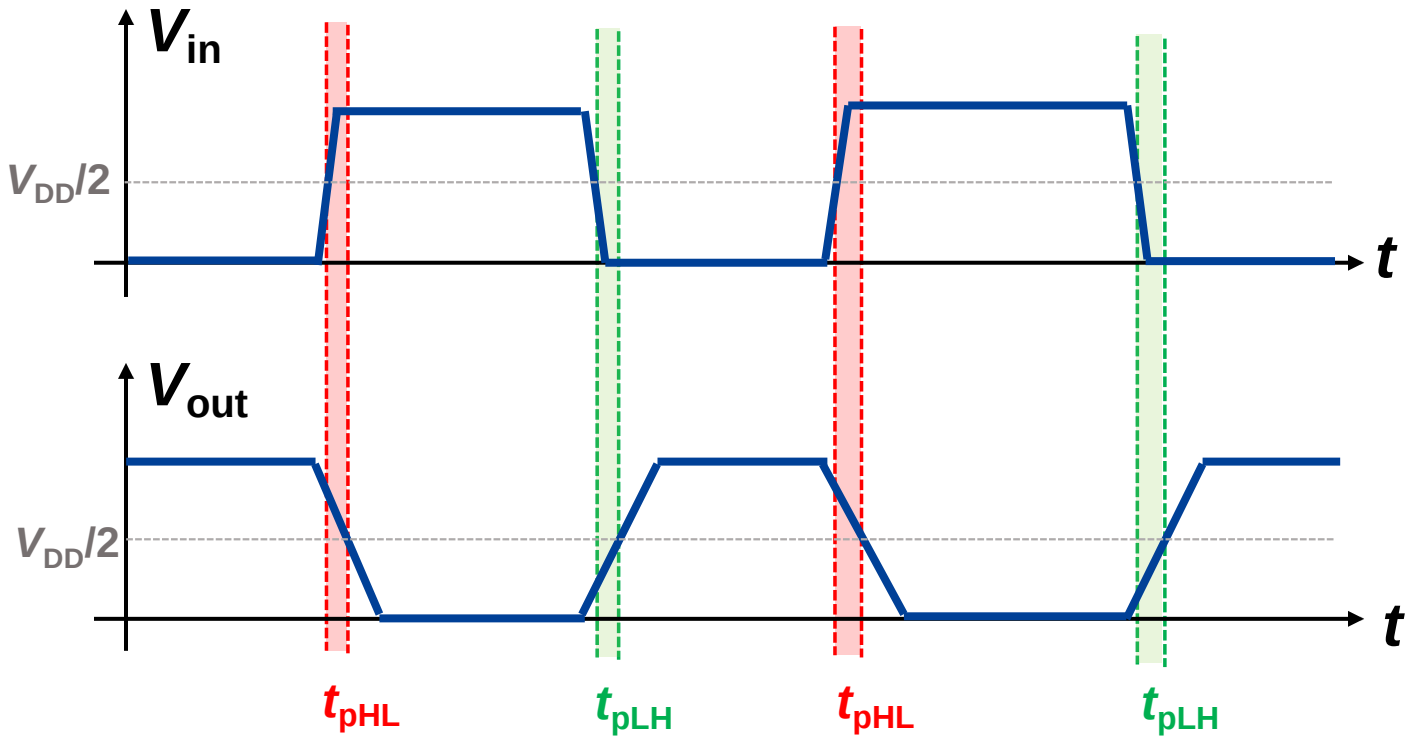


- Gate Capacitance C_{GC} – parallel capacitance.
- Parasitic Capacitance C_{SB} and C_{DB} – p-n junction diffusion capacitance.
- The capacitance counts ONLY when the voltage across it changes during the PUN and/or PDN process.

CMOS Inverter Delay Definitions

$$t_p = \left(t_{pHL} + t_{pLH}\right)/2$$

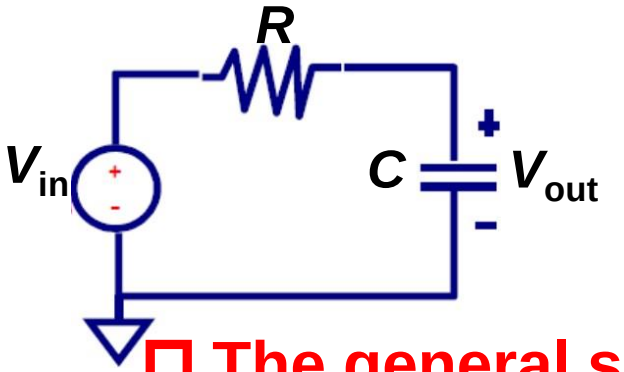




- Propagation time is the charge/discharge time of capacitance.
- During PDN functioning, C_L discharges, t_{pHL} relates to time difference of $V_{in} = V_{DD}/2$ -> $V_{out} = V_{DD}/2$.
- During PUN functioning, C_L charges, t_{pLH} relates to time difference of $V_{in} = V_{DD}/2$ -> $V_{out} = V_{DD}/2$.

Inverter Equivalent Circuit

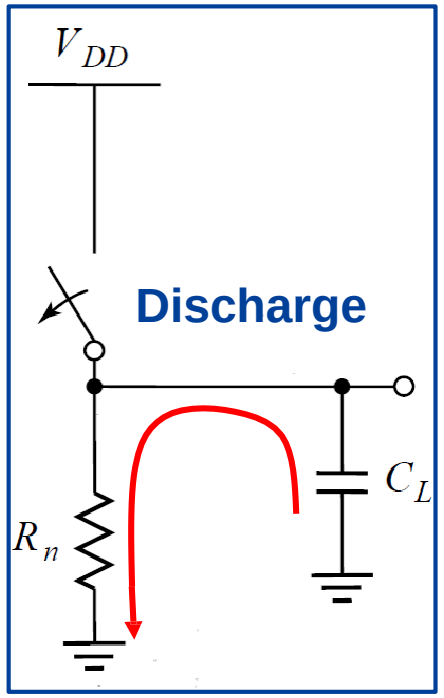
A first-order RC network: Step Response



Kirchhoff's Current Law

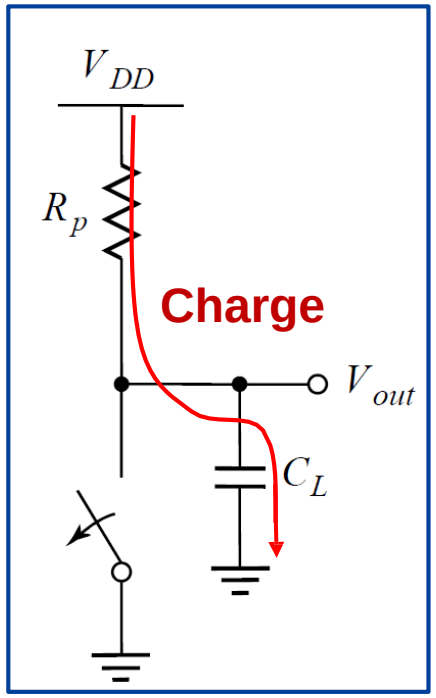
$$\frac{V_{in}-V_{out}}{R}=C_L\cdot\frac{dV_{out}}{dt}$$

PDN
$V_{out} = V_{DD} \rightarrow V_{DD}/2$



$$\tau_n = R_n \cdot C_L$$

PUN
$V_{out} = V_{DD}/2 \rightarrow V_{DD}$



$$\tau_p = R_p \cdot C_L$$

The general solution of linear first-order differential equation $\frac{dy}{dx}+P(x)y=Q(x)$ is:

$$y = e^{-\int P(x)dx}\left(\int Q(x)e^{\int P(x)dx}dx + C\right)$$

$$V_{out}(t=0)=V_o$$
$$V_{out}(t=\infty)=V_\infty$$

$$V_{out}(t) = V_\infty + (V_0 - V_\infty)\cdot e^{-t/\tau},\ \tau = RC$$

- For PDN: $V_0 = V_{DD}$ & $V_\infty = 0$ $\quad V_{out}(t) = V_{DD}e^{-t/\tau_n}$
- For PUN: $V_0 = 0$ & $V_\infty = V_{DD}$ $\quad V_{out}(t) = V_{DD}(1-e^{-t/\tau_p})$

$$V_{out}(t) = e^{-\int \frac{1}{RC} dt} \left(c_0 + \int \frac{V_{in}}{RC} e^{\int \frac{1}{RC} dt} dt \right)$$

$$= e^{-\frac{t}{RC}} \left[c_0 + \int \frac{V_{in}}{RC} e^{\frac{t}{RC}} dt \right]$$

$$= e^{-\frac{t}{RC}} \left[c_0 + V_{in} e^{\frac{t}{RC}} \right]$$

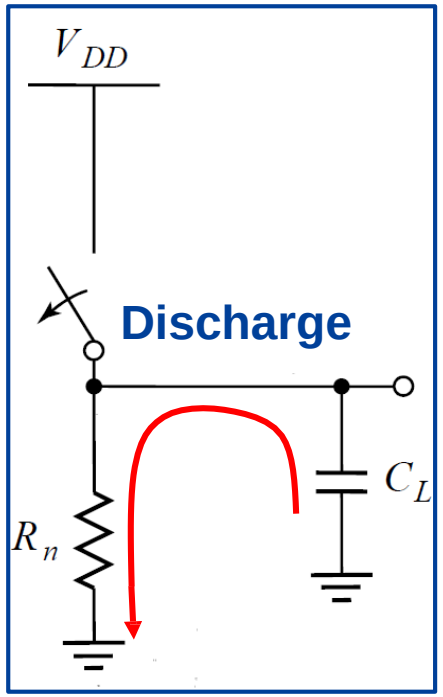
$$= V_{in} + c_0 e^{-\frac{t}{RC}}$$

$$\begin{cases} t = 0 \text{ 时}, \ V_{out}(0) = V_{in} + c_0 = V_0 \\ t = \infty \text{ 时}, \ V_{out}(\infty) = V_{in} = V_\infty \end{cases} \Rightarrow \begin{cases} c_0 = V_0 - V_\infty \\ V_{in} = V_\infty \end{cases}$$

$$\Rightarrow V_{out}(t) = V_\infty + (V_0 - V_\infty) e^{-\frac{t}{RC}}$$

Inverter Propagation Delay

PDN
$V_{out} = V_{DD} \rightarrow V_{DD}/2$



- **A first-order RC discharge network**

$$V_{out}(t) = V_{DD} e^{-t/\tau_n}, \quad \tau_n = R_n \cdot C_L$$

- **At $t = t_{pHL}$**

$$V_{out}(t_{pHL}) = V_{DD} e^{-t_{pHL}/\tau_n} = V_{DD}/2$$

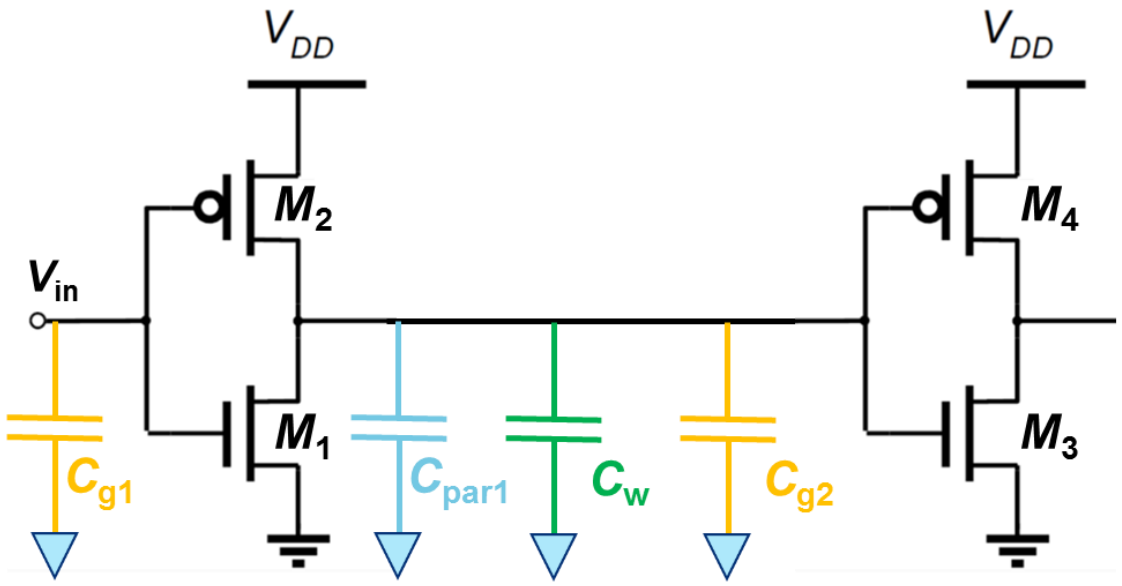
$$t_{pHL} = \tau_n \ln \frac{V_{DD}}{V_{DD}/2} = \tau_n \ln 2 = 0.69 R_n \cdot C_L$$

- **Similarly, for PUN**

$$V_{out}(t) = V_{DD}(1 - e^{-t/\tau_p}), \ \tau_p = R_p \cdot C_L$$

$$t_{pLH} = \tau_p \ln 2 = 0.69 R_p \cdot C_L$$

Inverter Propagation Delay



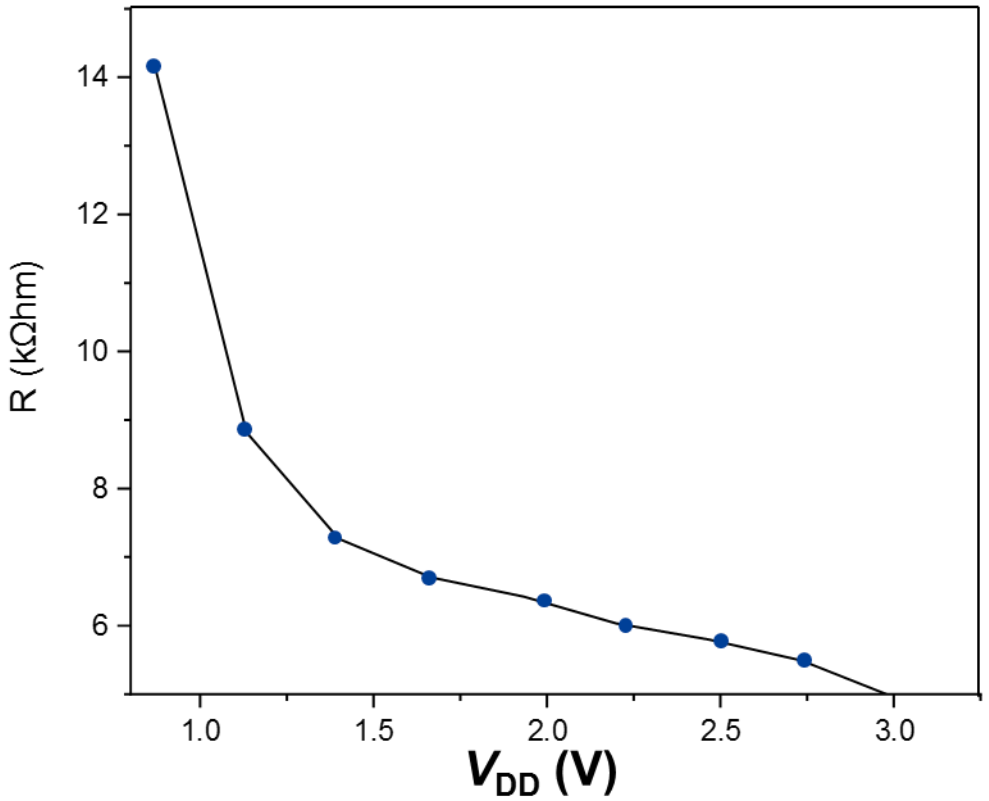
Goal: To optimize the propagation delay

- **Modifying supply voltage V_{DD} -- equivalent resistance**
- **Sizing PMOS/NMOS ratio -- Switching Threshold**

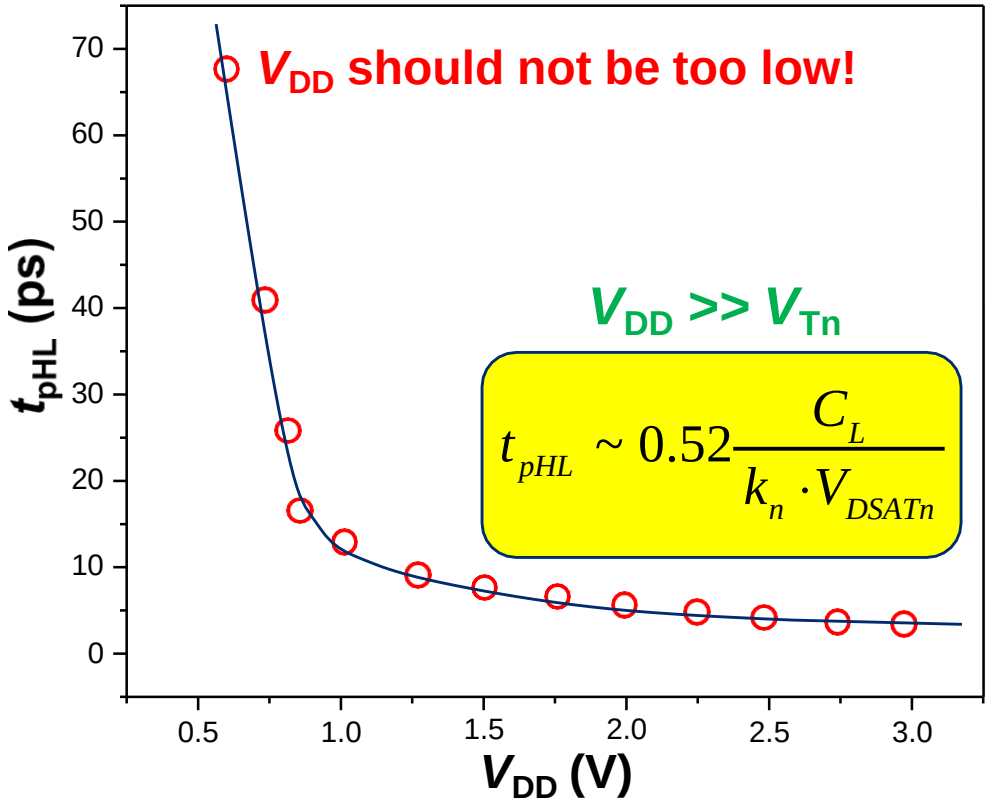
$$t_p = \left(t_{pHL} + t_{pLH}\right)/2 = 0.69R \cdot C_L = 0.69 \left(\frac{R_n + R_p}{2}\right) \cdot \left(C_{par1} + C_{g2} + C_w\right)$$

Inverter Delay as a Function of V_{DD}

Equivalent R_{on} vs. V_{DD}

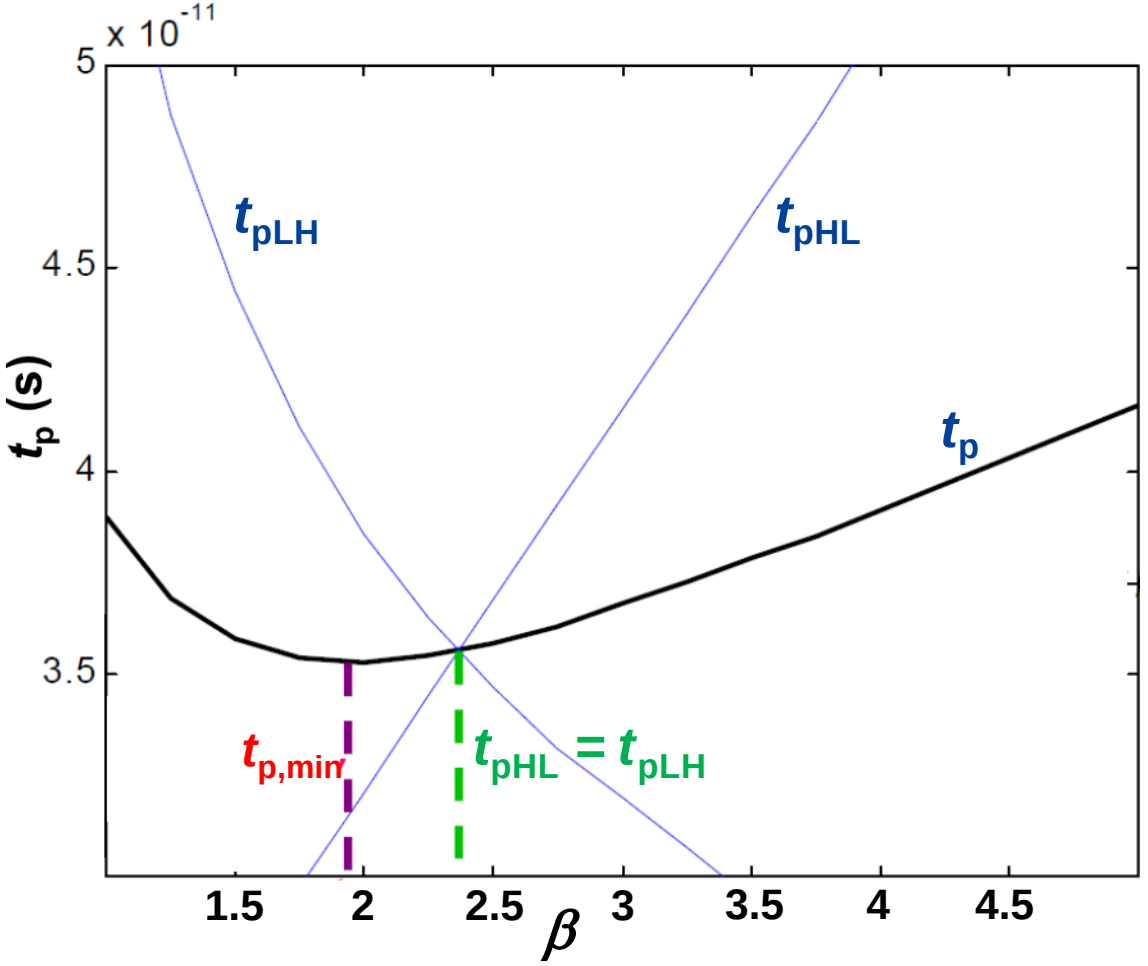


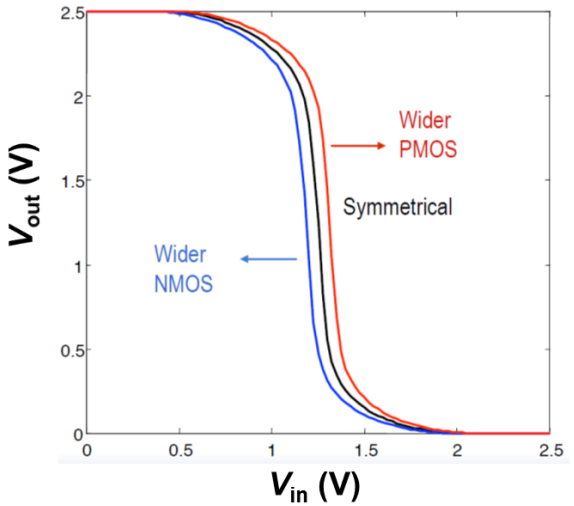
$$t_p \propto R_{on}$$

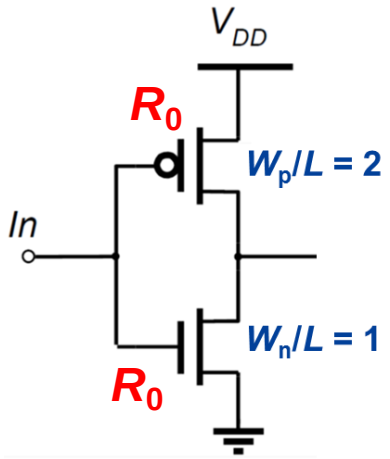


Inverter Delay vs. PMOS/NMOS Size Ratio

$$\beta = \frac{W_p}{L_p} / \frac{W_n}{L_n} = \frac{W_p}{W_n} \quad (L_n = L_p = L_0)$$

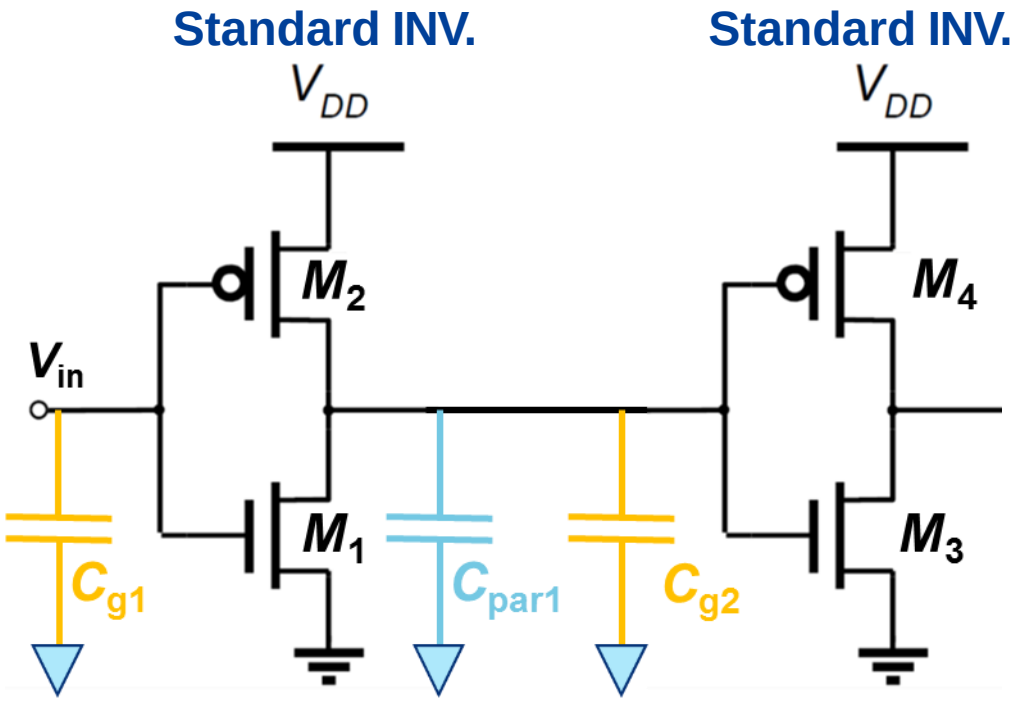






- Larger β (wider PMOS) means stronger PUN strength in terms of smaller R_p, higher V_M, and shorter t_{pLH}.
- We will choose $\beta = 2$ in this course as standard inverter for optimized t_p with almost equivalent NMOS/PMOS strength and resistance.

Propagation Delay vs. Inverter Sizing



Neglect C_w and C_{GD}

$$t_{p1} = t_{p,\text{int}} + t_{p,ext} = 0.69 \cdot [R_0 \cdot C_{par} + R_0 \cdot C_{g2}]$$

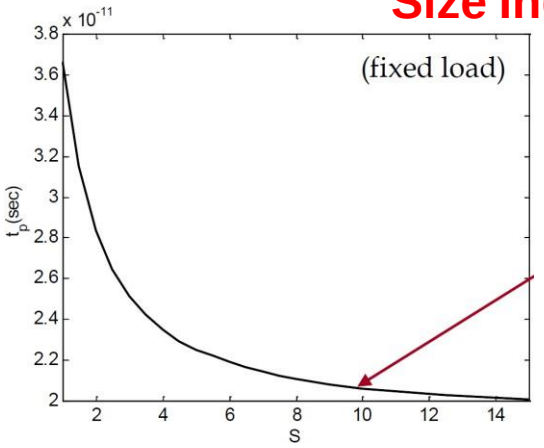
Increase the first INV. size by *S*

R_0 -> R_0/S

C_{par} -> $C_{par} \cdot S$, C_{g1} -> $C_{g1} \cdot S$

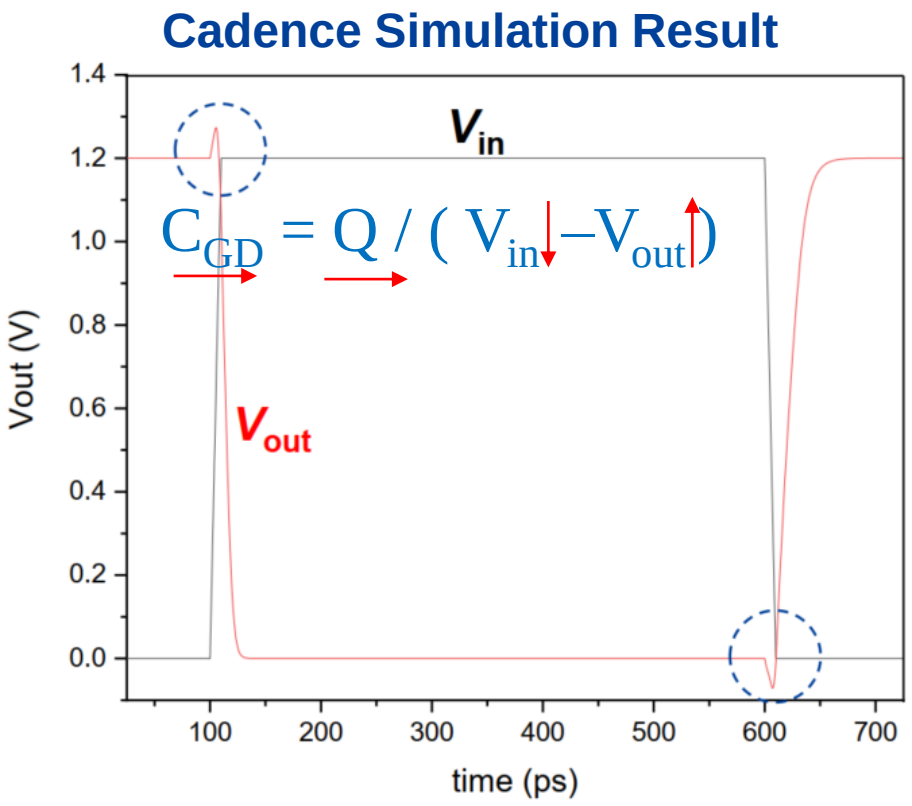
$$t_{p1} = t_{p,\text{int}} + t_{p,ext} = 0.69 R_0 \cdot C_{par1} + 0.69 \frac{R_0}{S} \cdot C_{g2}$$

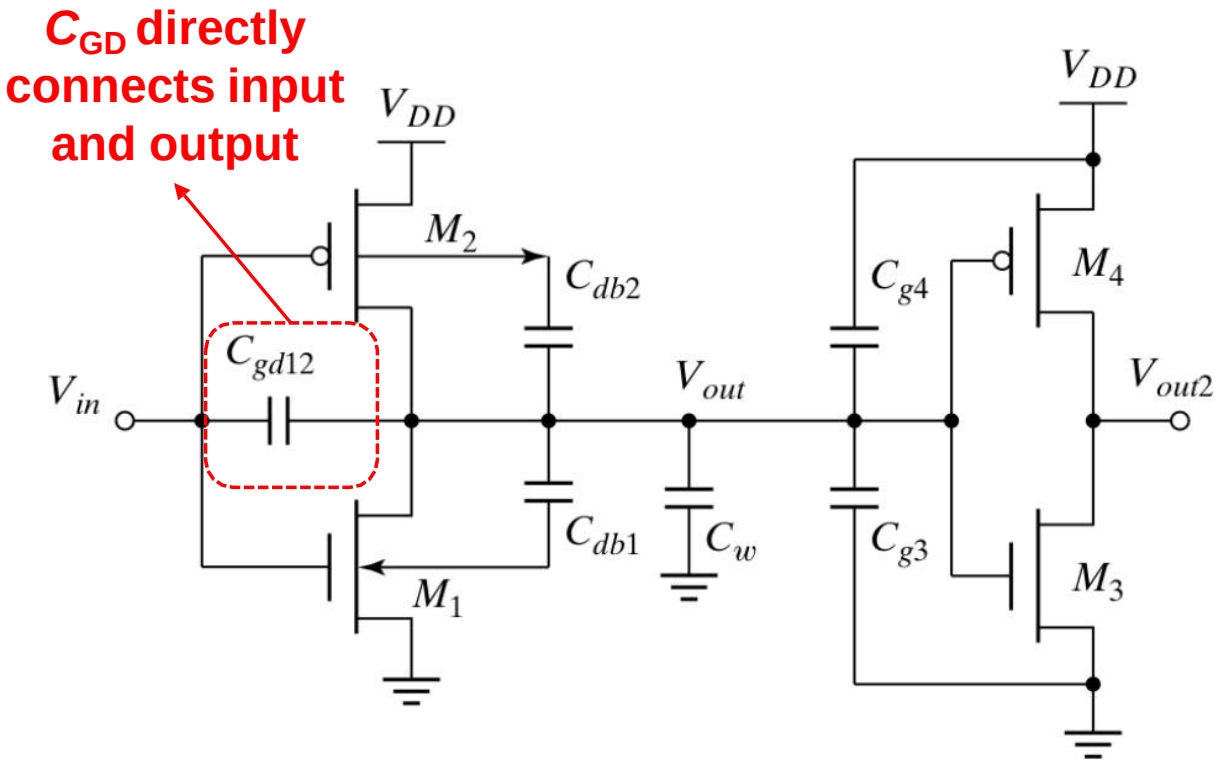
Size Independent **Reduce with Size**



Self-loading effect:
Intrinsic capacitance dominates

The Effect of C_{GD}

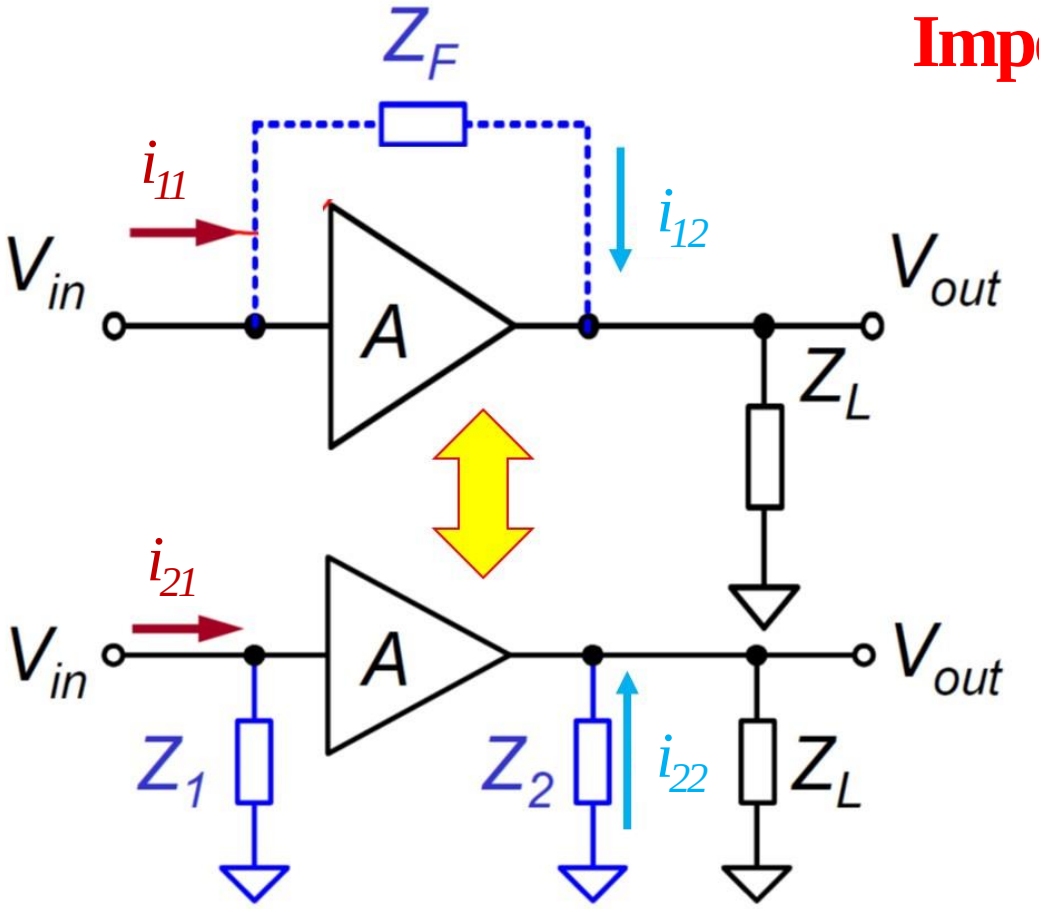




- When V_{in} changes abruptly, the nature of C_{GD} ensures relative stable voltage drop across it at that moment.

Miller Theorem

- In an amplifier circuit, if the impedance is connected in between the input & output nodes, then connected impedance can be changed to two separated impedances near input & output respectively, and Z1=Z/(1-A), Z2=Z/(1-1/A).



Impedance -> resistance / inductance / capacitance

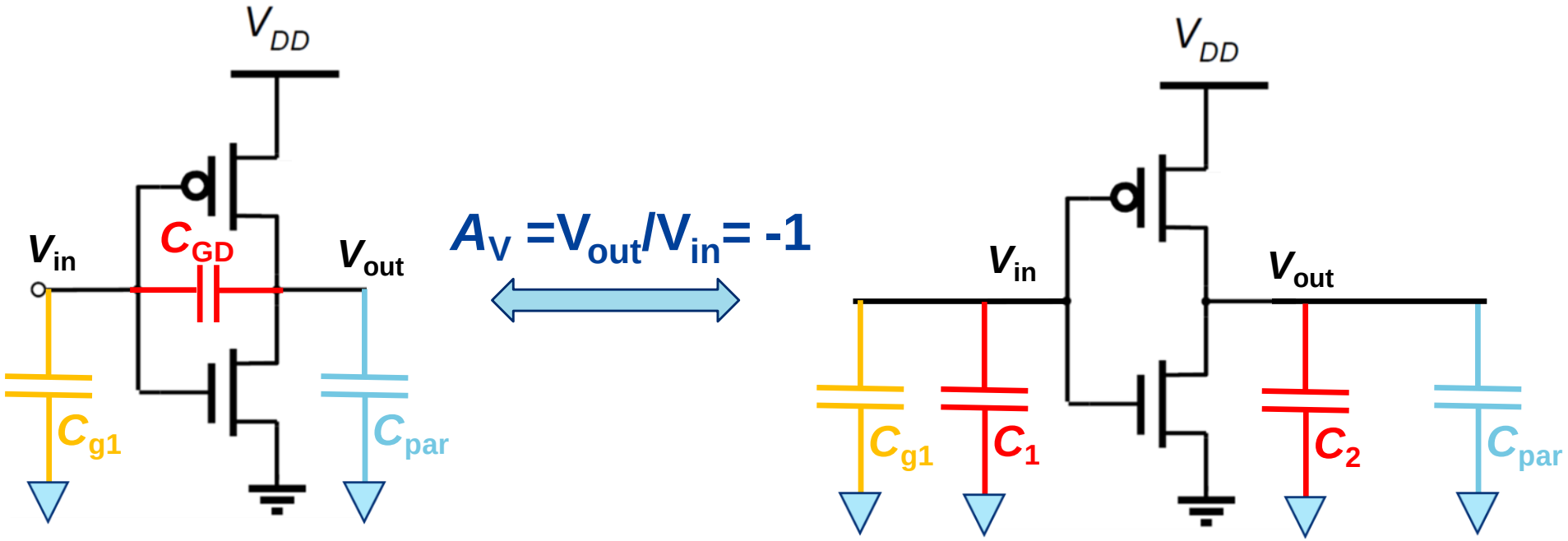
$$i_{11} = V_{in} \cdot \frac{1-A}{Z_F}, \qquad i_{12} = i_{11}$$

Equivalent circuit: $i_{11} = i_{21}$, $i_{12} = i_{22}$

$$i_{21} = V_{in} / Z_1$$
$$i_{22} = -AV_{in} / Z_2$$

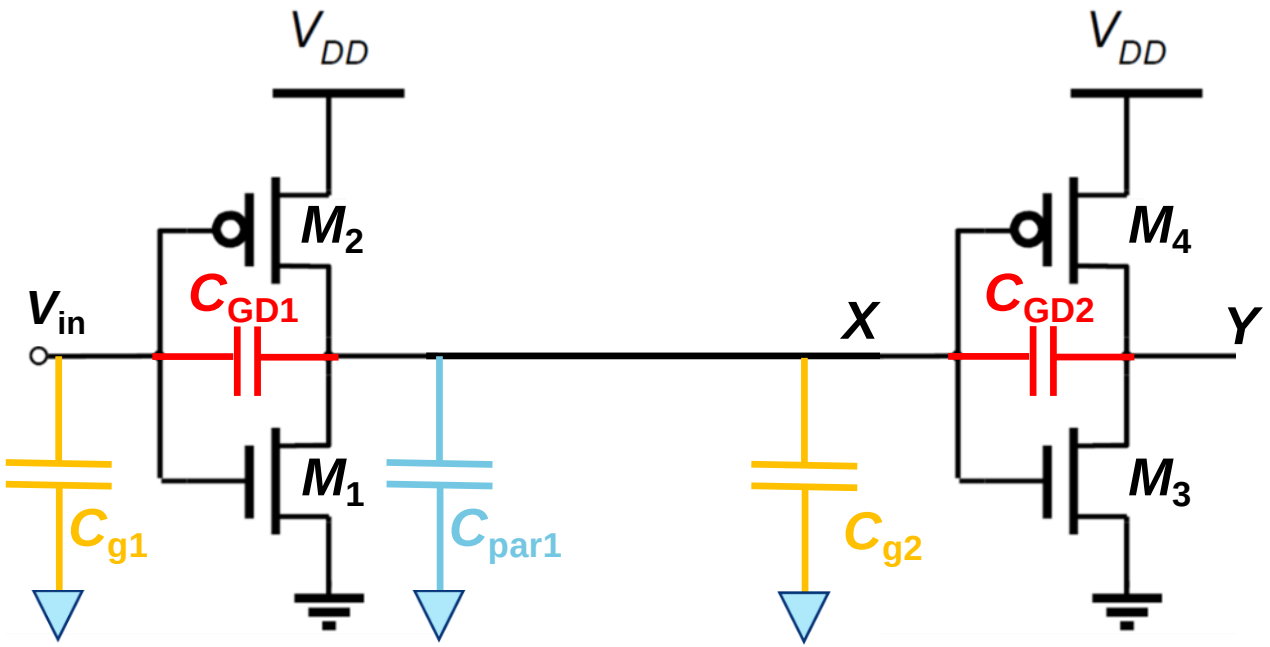
$$Z_1 = \frac{Z_F}{1-A}, \quad Z_2 = \frac{Z_F}{1-1/A}$$

Miller Theorem and CMOS Inverter



$$Z_1 = \frac{Z_F}{1-A}, \quad Z_2 = \frac{Z_F}{1-1/A} \rightarrow Z_1 = \frac{Z_F}{2}, \quad Z_2 = \frac{Z_F}{2} \xrightarrow{Z=1/\omega C} C_1 = C_2 = 2C_{GD}$$

Miller Theorem and CMOS Inverter



- C_{GD1} will contribute to t_{p1} by adding $2C_{GD1}$ to the output.
- Yet C_{GD2} will NOT affect t_{p1} due to the relatively constant voltage difference between X and Y during the process.