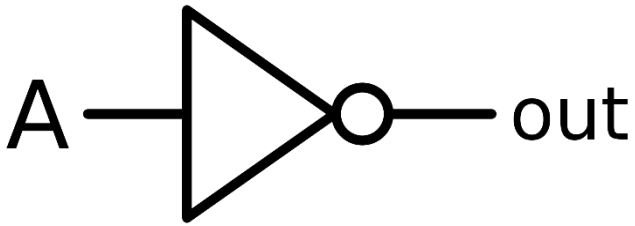
Lecture 4: CMOS Inverter Physical Characteristics



Outline

- **CMOS Inverter Equivalent Resistance and Capacitance**
  - Resistance vs. V_{DD}
  - Capacitance of Logic Circuit
- **CMOS Inverter Propagation Delay**
  - Delay vs. Resistance & Capacitance
  - Miller Theorem and C_{GD}
- **CMOS Inverter Power Consumption**
  - Static & Dynamic power
  - Switching Power Consumption
  - Short-circuit Power Consumption

Tsunami of Data Era has Come!

- Over 2.5 billion computers in the world
  - 1 PW (10^{15} W) of power dissipation
  - Equivalent to 160 nuclear plants!
  - 'Tsunami of data' could consume 1/5 of global electricity by 2025!

Google Data Center

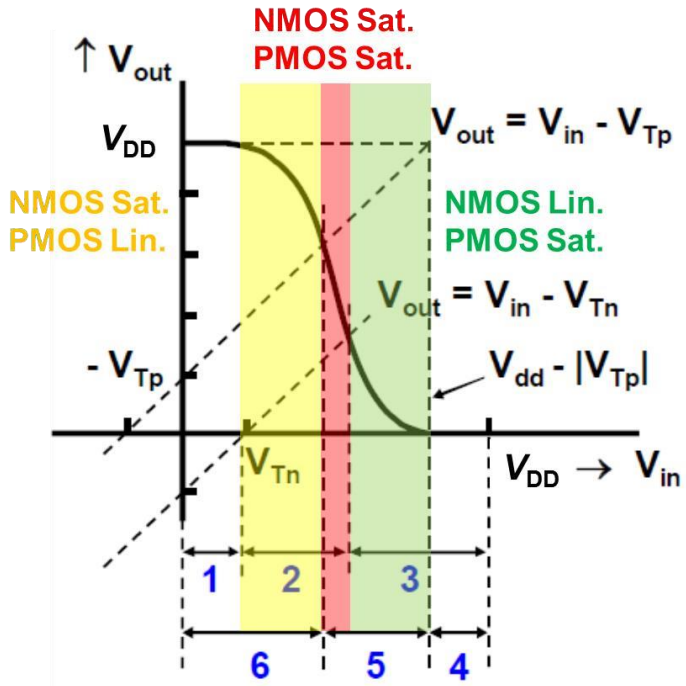
Facebook Data Center @ Sweden

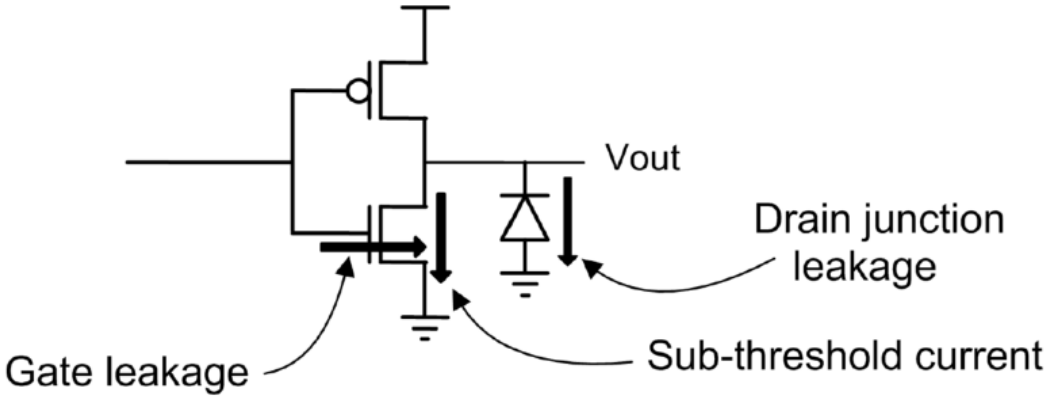
The Power in CMOS Inverter

Dynamic power

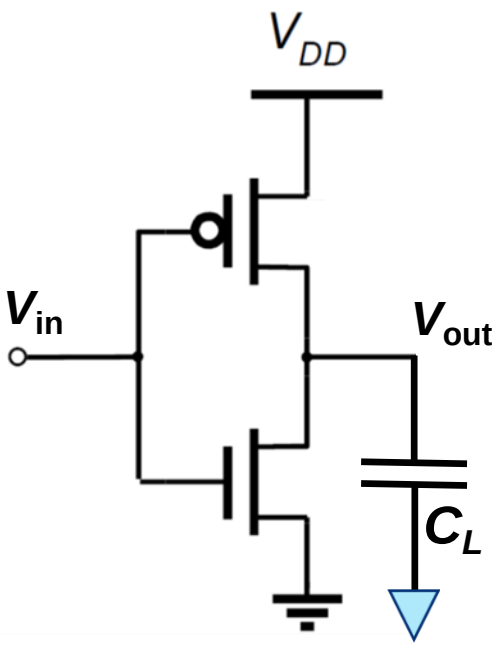
- **Switching power**
  - Charge/discharge capacitor
- **Short-circuit power**
  - Both NMOS and PMOS *ON* during transition
- **Gate / Junction Leakage power**
  - Gate / Drain to Body
  - Relatively small
- **Sub-threshold leakage power**
  - $I_{DS} > 0$ when $V_{GS} < V_T$
  - I_{DS} increases as V_T decreases

Static power

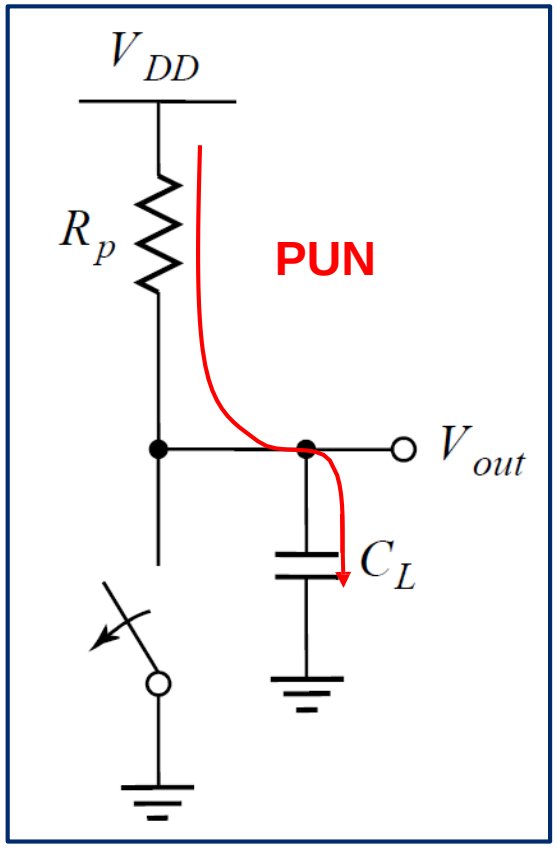




Charging/discharging Consumption



$V_{in} = V_{DD} \rightarrow 0$



$$E_{0\to1} = \int_{t=0}^{\infty} V_{DD} \cdot I_{Dp} \cdot dt$$

$$I_{Dp} = C_L \cdot \frac{dV_{out}}{dt}$$

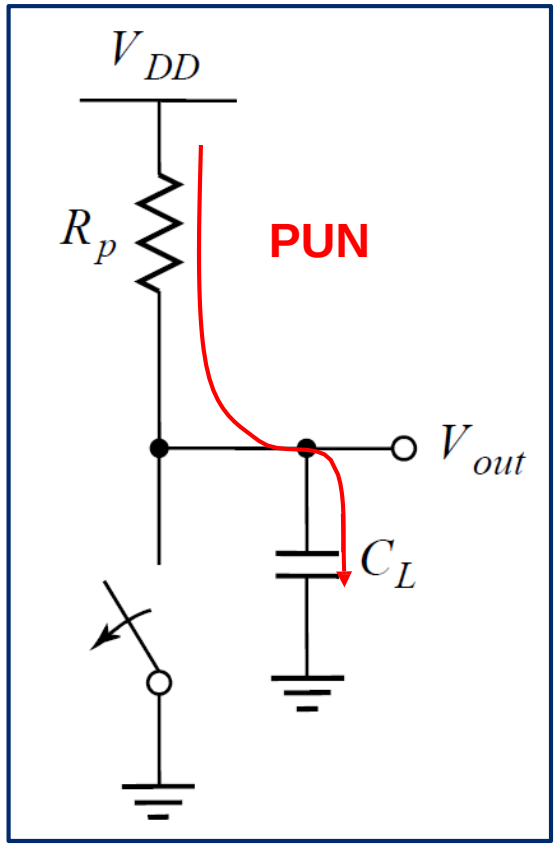
- CMOS Inverter $V_{OH} = V_{DD}$, $V_{OL} = 0$

$$E_{0\to1} = C_L \cdot V_{DD} \cdot \int_{V_{OL}}^{V_{OH}} dV_{out} = C_L \cdot V_{DD} \cdot (V_{OH} - V_{OL})$$
$$= C_L \cdot V_{DD}^{\,2}$$

Dynamic energy dissipation is NOT a function of transistor resistance or size!

Charging/discharging Consumption

$V_{in} = V_{DD} \rightarrow 0$



$$E_{0\rightarrow 1}(V_{DD}) = V_{DD} \cdot C_L \cdot \int_{V_{OL}}^{V_{OH}} dV_{out} = C_L \cdot V_{DD} \cdot (V_{OH} - V_{OL})$$

- Energy (V_{DD}) = Energy (heat) + Energy (C_L)

$V_{OH} = V_{DD}$, $V_{OL} = 0$

$$E_{C_L} = C_L \cdot \int_{V_{OL}}^{V_{OH}} V_{out} \cdot dV_{out} = \frac{1}{2} C_L \cdot (V_{OH}^2 - V_{OL}^2)$$

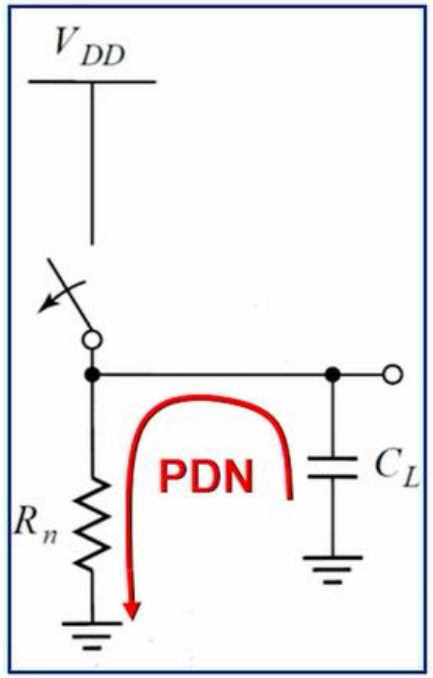
$$E_{heat} = E_{0\rightarrow 1}(V_{DD}) - E_{C_L}$$

$$E_{C_L} = E_{heat} = \frac{1}{2} C_L \cdot V_{DD}^2$$

- During the PUN, 50% energy dissipated in PMOS in the form of heat, the other 50% energy stored in the C_L.

Charging/discharging Consumption

$V_{in} = V_{DD}$
$V_{out} = V_{DD} \rightarrow 0$



- Pull-Down Network: V_{DD} is disconnected!
- Energy (C_L) = Energy (heat)
- The 50% energy stored in the C_L during the previous PUN will convert to heat dissipation in NMOS for PDN.
- Dynamic energy/power consumption ONLY occurs during the PUN process.

$$E_{0\rightarrow 1}(V_{DD}) = V_{DD} \cdot C_L \cdot \int_{V_{OL}}^{V_{OH}} dV_{out} = C_L \cdot V_{DD} \cdot (V_{OH} - V_{OL})$$

Transition Activity and Switching Power

- Consider switching a CMOS Invertor for *N* clock cycles

$$E_N = C_L \cdot V_{DD}^2 \cdot n(N)$$

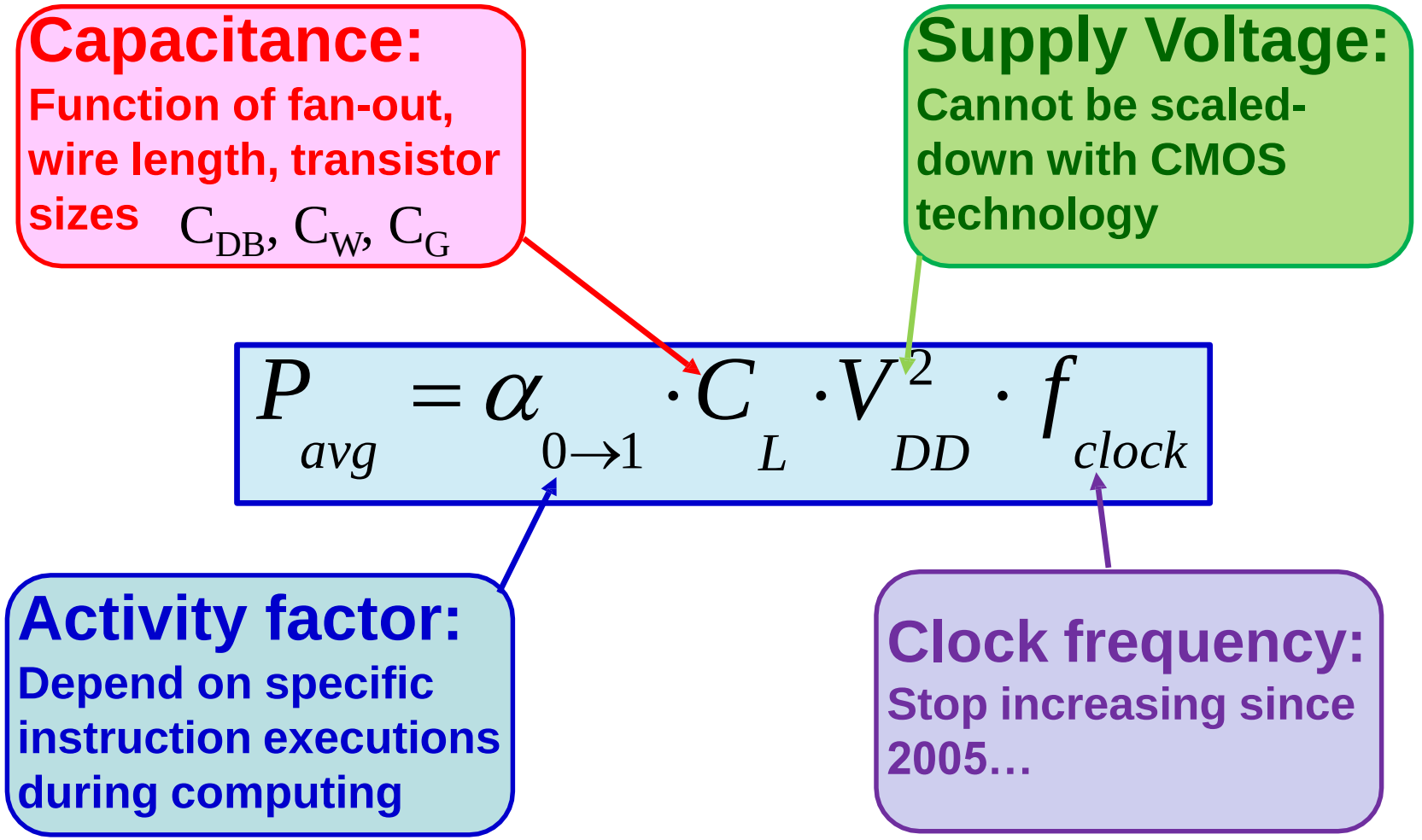
  - E_N: the energy consumed for *N* clock cycles
  - *n*(*N*): the number of 0->1 transitions in *N* clock cycles

- Average dynamic power $P_{avg} = \lim_{N\to\infty} \frac{E_N}{N} \cdot f_{clk} = (\lim_{N\to\infty} \frac{n(N)}{N}) \cdot C_L \cdot V_{DD}^2 \cdot f_{clk}$

Define activity factor $\alpha_{0\to1} = \lim_{N\to\infty} \frac{n(N)}{N}$

$$P_{avg} = \alpha_{0\to1} \cdot C_L \cdot V_{DD}^2 \cdot f_{clock}$$

Switching Power of CMOS Inverter

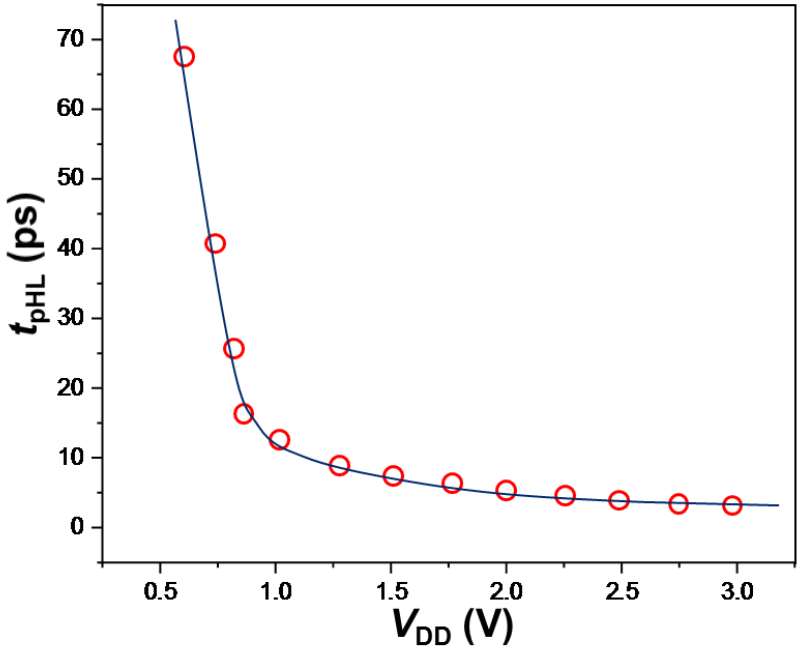


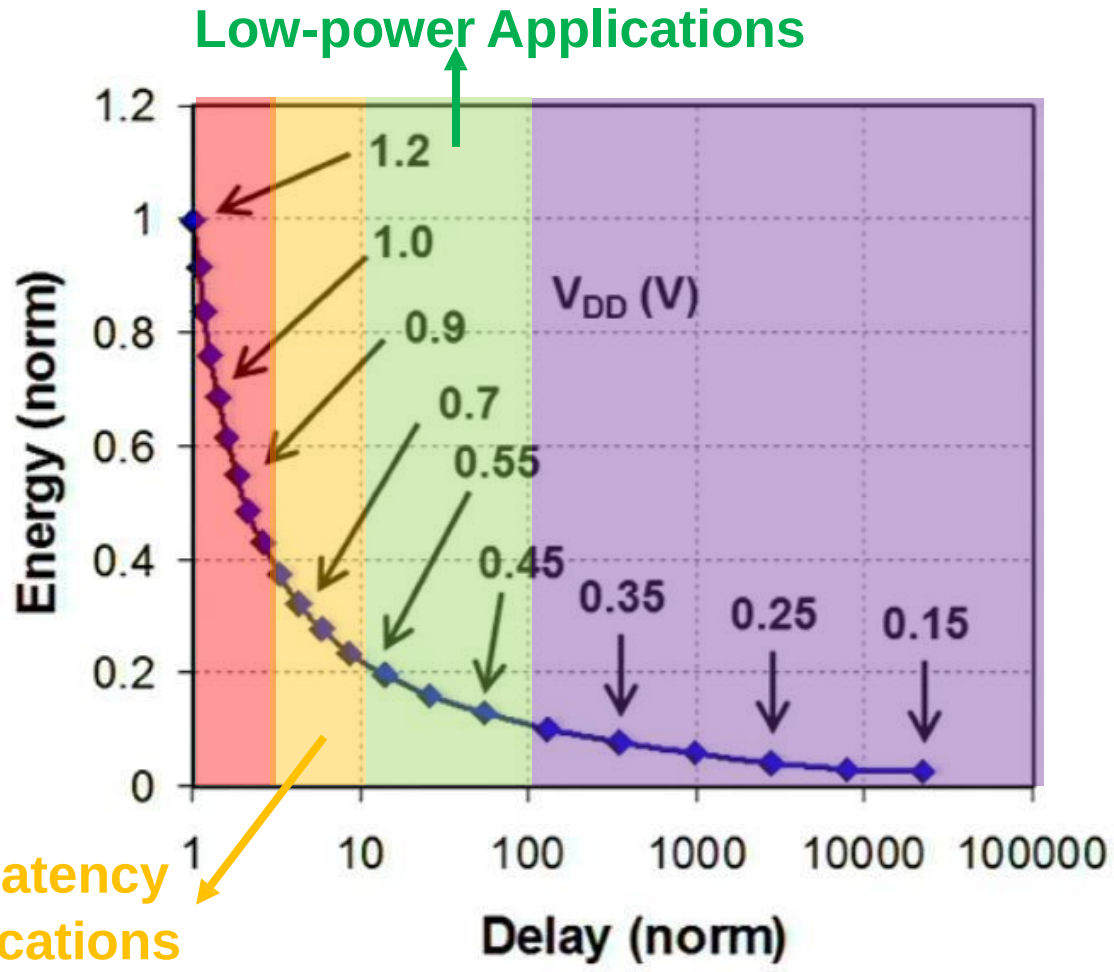
Switching Power as a Function of V_{DD}

- **Switching Power Consumption**

$$P_{avg} = \alpha_{0\to1} \cdot C_L \cdot V_{DD}^2 \cdot f_{clock}$$

- **Propagation Delay**





- **The essence of digital IC design is the compromise between power and delay!**

Dark Silicon Effect

- **Parameters**
  - Switched capacitance C_L=2fF/gate (V_{DD} = 1V) @ 90 nm node
  - Fan-out F = 4
  - Clock frequency f_{clock} = 2.5 GHz

- **Power per gate per switching**

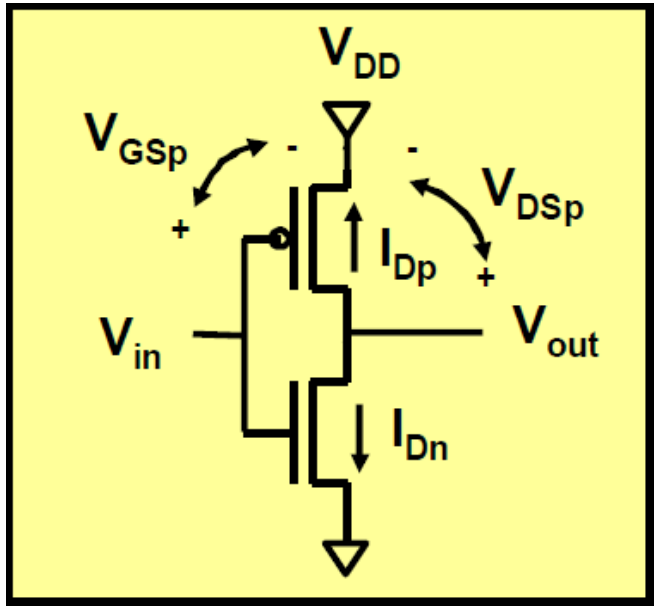
$$P = \mathrm{F} \cdot C_L \cdot V_{DD}^2 \cdot f_{clock} = 4 \times 2 \times 10^{-15} \times 2.5 \times 10^9 = 20 \mu W$$

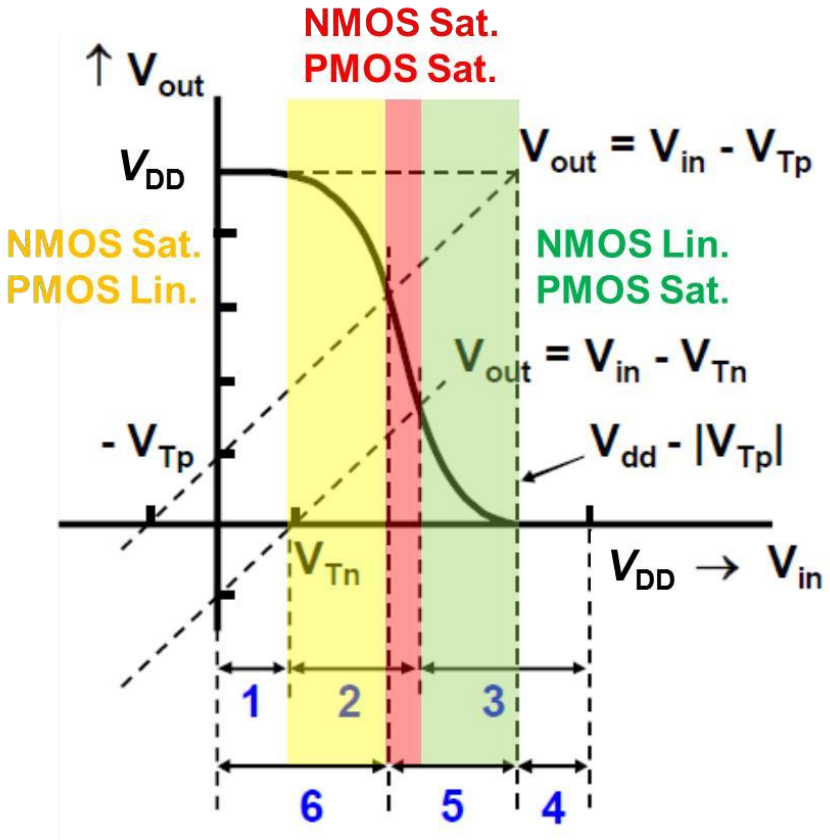
- **Assume**
  - Activity factor α= 0.1
  - N = 1 billion gates

$$P_{tot} = (C_L \cdot N) \cdot V_{DD}^2 \cdot (\alpha_{0 \to 1} \cdot f_{clock}) = 2000\ W$$

With the power budget of 200 W, only 10% transistors can only be switched simultaneously. → Dark Silicon Effect.

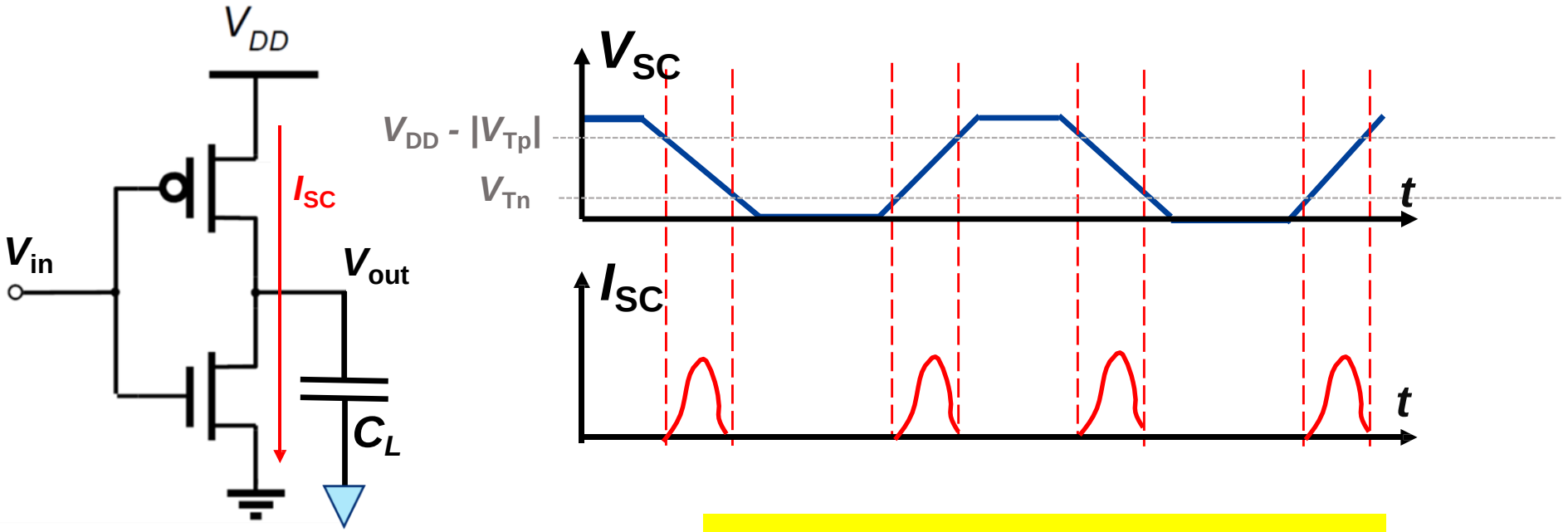
Short-Circuit Power Consumption





- In the colored region, both NMOS and PMOS are turned on, a low-impedance path formed between V_{DD} and GND → Short-Circuit Power Consumption.

Short-Circuit Power Consumption



$$t_{SC} = \frac{V_{DD} - 2V_T}{V_{DD}} \cdot t_{slope}(0 \rightarrow 100\%)$$

Triangular Approximation

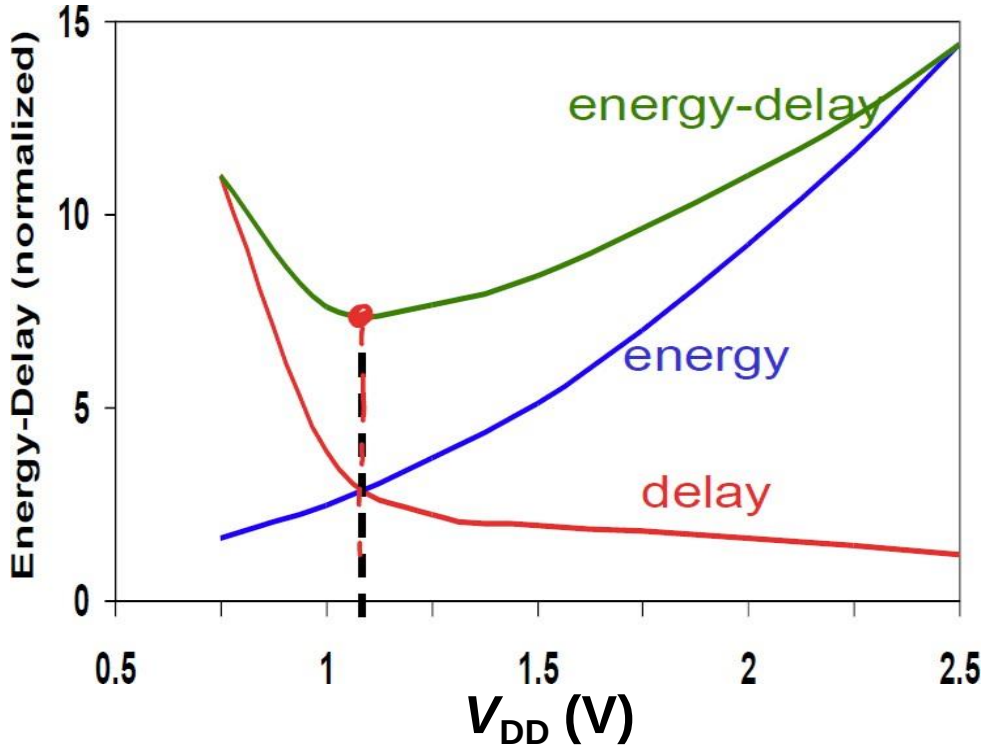
$$E_{sc} = V_{DD}\frac{I_{peak}t_{sc}}{2} + V_{DD}\frac{I_{peak}t_{sc}}{2} = t_{sc}V_{DD}I_{peak}$$

$$P_{SC} = t_{SC} \cdot V_{DD} \cdot I_{peak} \cdot f_{0\rightarrow 1}$$

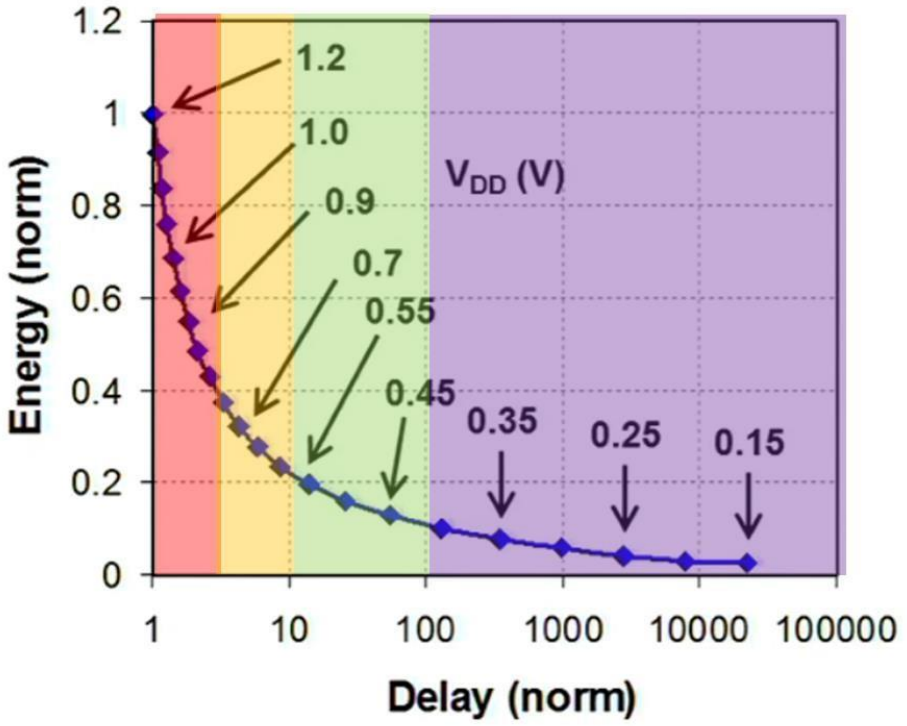
PDP and EDP

- **Power-delay product (PDP) = $P_{av} \times t_p = (C_L V_{DD}^2)/2$**
  - PDP is the average energy consumed per switching event (Watts × sec = Joule)

- **Energy-delay product (EDP)**
  - EDP = PDP × t_p = $P_{av} \times t_p^2$
  - PDP is the average energy consumed multiplied by the computation time required.



Summary of CMOS Inverter



$$t_{p1} = 0.69 R_0 \cdot [C_{par} + C_{g2}]$$

$$P_{avg} = \alpha_{0\to1} \cdot C_L \cdot V_{DD}^2 \cdot f_{clock}$$

- The equivalent circuit of the static CMOS inverter is the 1st-order RC network.
- Propagation delay depend on V_{DD}, power consumption depend on V_{DD} and gate size.
- Smaller voltage directly reduces power consumption, yet enlarge propagation delay.
- With a $\beta = W_p/W_n = 2$, the standard inverter reaches optimized condition, and it serves as the cornerstone for the following logic circuit design.