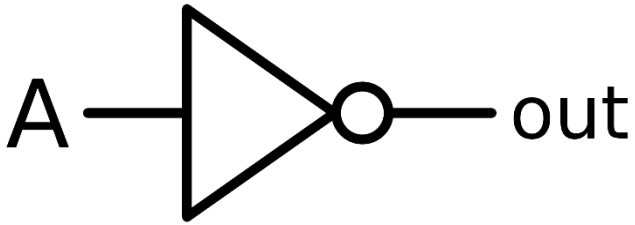
Lecture 4: CMOS Inverter Physical Characteristics

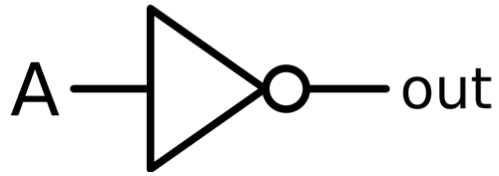


Outline

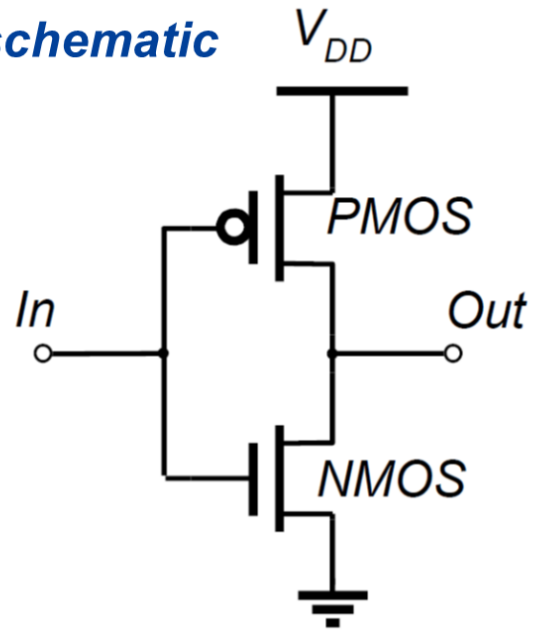
- **CMOS Inverter Equivalent Resistance and Capacitance**
  - Resistance vs. V_{DD}
  - Capacitance of Logic Circuit
- **CMOS Inverter Propagation Delay**
  - Delay vs. Resistance & Capacitance
  - Miller Theorem and C_{GD}
- **CMOS Inverter Power Consumption**
  - Static & Dynamic power
  - Switching Power Consumption
  - Short-circuit Power Consumption

The CMOS Inverter

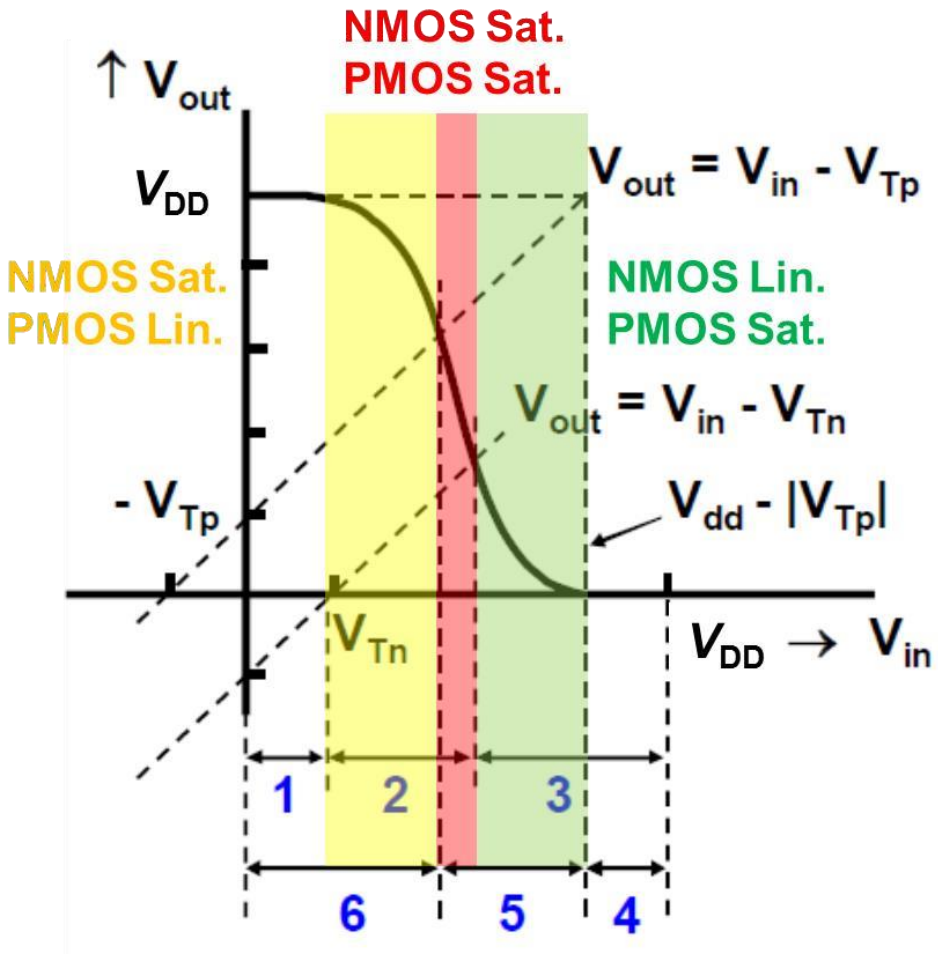
symbol



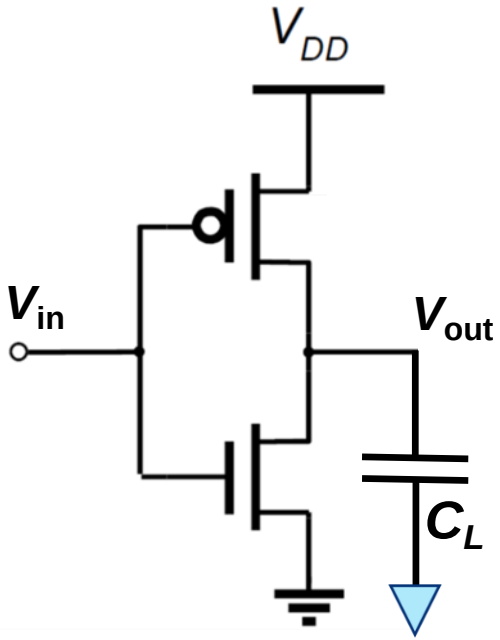
schematic



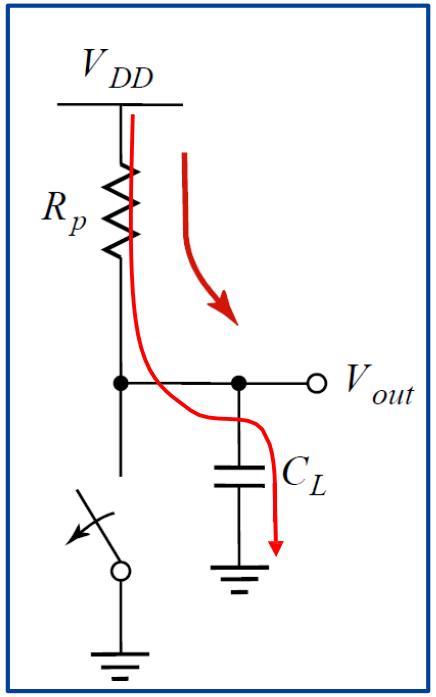
Voltage Transfer Characteristic (VTC)



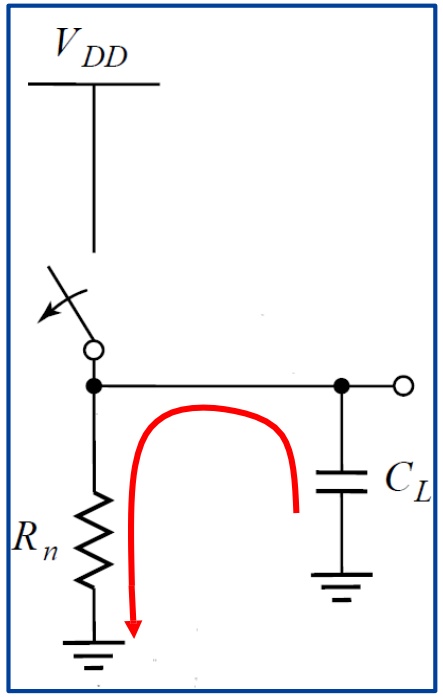
CMOS Inverter Operational Principle



$V_{in} = V_{DD} \rightarrow 0$

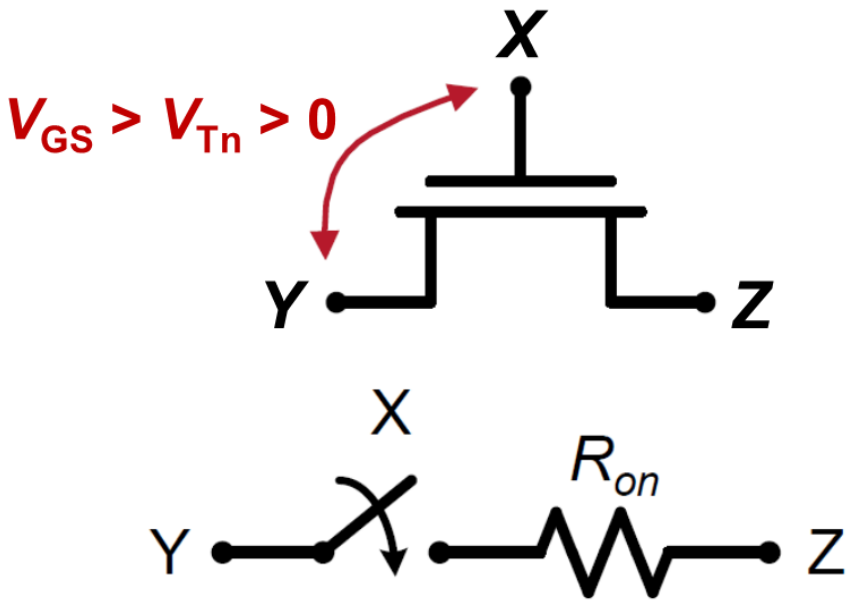


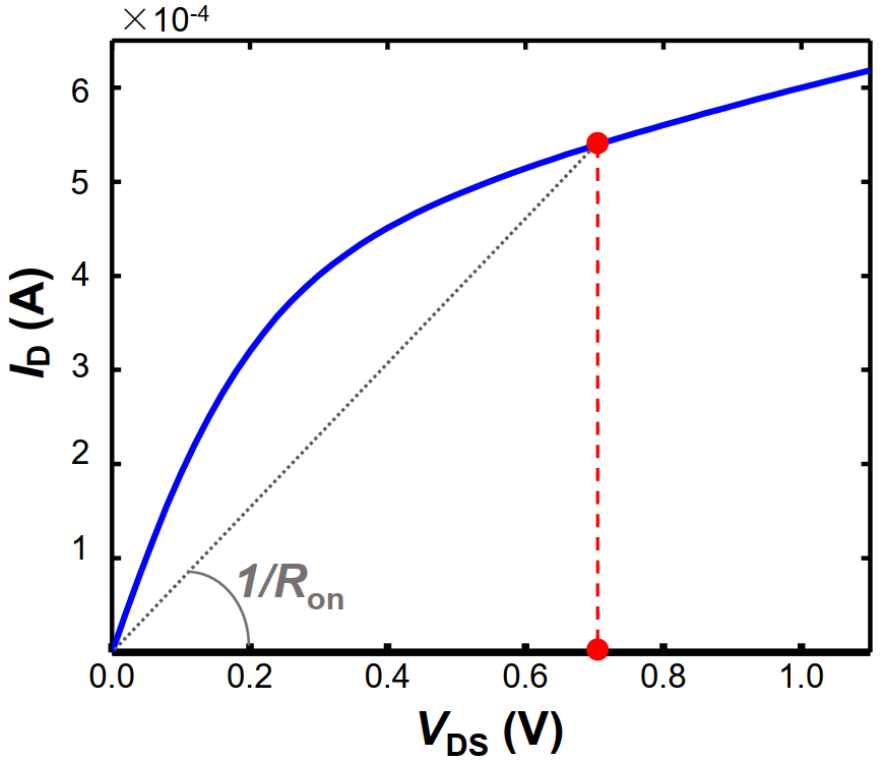
$V_{in} = 0 \rightarrow V_{DD}$



- The equivalent circuit of CMOS inverter is a first-order RC network.
- Need to know *R* and *C* first.

Review: *I-V* Characteristic of MOSFET





$$I_{DS} = \mu_n C_{ox} \cdot \frac{W}{L} \cdot (V_{GT} \cdot V_{\min} - \frac{V_{\min}^2}{2}) \cdot (1 + \lambda V_{DS})$$

take derivation of V_{DS}

$$1/R_{on} = \mu_n C_{ox} \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{\min} - \frac{V_{\min}^2}{2} \right) \lambda$$

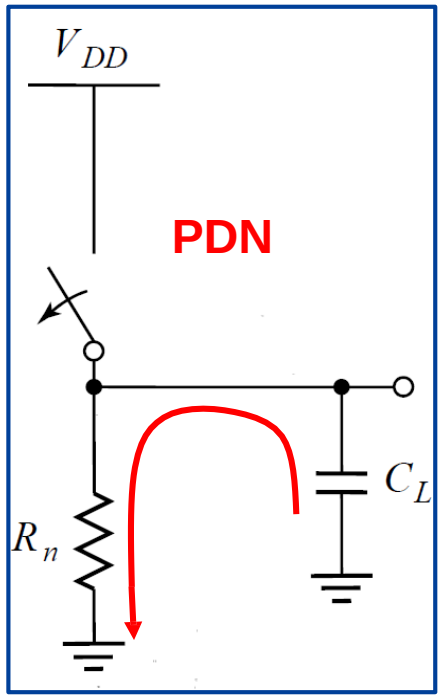
$$V_{\min} = \min (V_{DS},\ V_{GT},\ V_{DSAT})$$

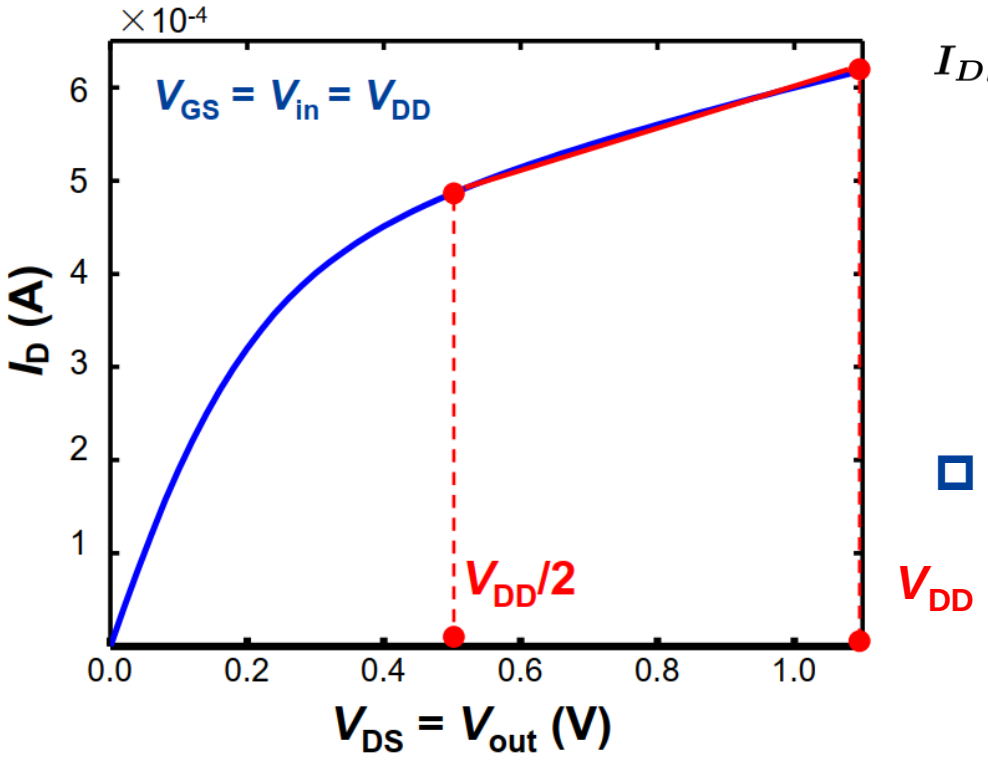
Lin Sat V-Sat

Equivalent Resistance of Inverter

$$I_{DS} = \mu_n C_{ox} \cdot \frac{W}{L} \cdot (V_{GT} \cdot V_{\min} - \frac{V_{\min}^2}{2}) \cdot (1 + \lambda V_{DS})$$

$V_{in} = V_{DD}$, $V_{out} = V_{DD} \rightarrow V_{DD}/2$





- NMOS in Vel. Sat. $V_{\min} = V_{DSAT}$

$$I_{DSAT} = \mu_n C_{ox} \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2} \right)$$

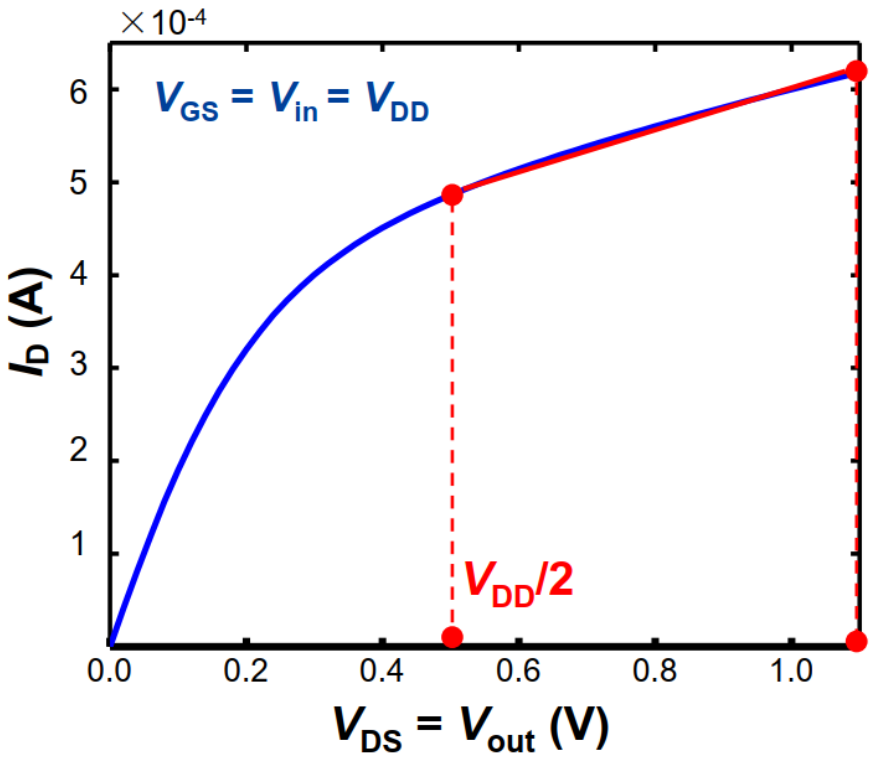
$$I_{DS}(V_{DS}) = I_{DSAT} \cdot (1 + \lambda V_{DS})$$

- Calculating equivalent resistance

$$R(V_{DS}) = \frac{V_{DS}}{I_{DSAT} \cdot (1 + \lambda V_{DS})}$$

Computing NMOS Equivalent Resistance

$$R(V_{DS}) = \frac{V_{DS}}{I_{DSAT} \cdot (1 + \lambda V_{DS})}$$



- **Method 1: Integration**

$$R_{on} = \frac{1}{-V_{DD}/2} \int_{V_{DD}}^{V_{DD}/2} \frac{V}{I_{DSAT} \cdot (1 + \lambda V)} dV \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{7}{9} \lambda V_{DD}\right)$$

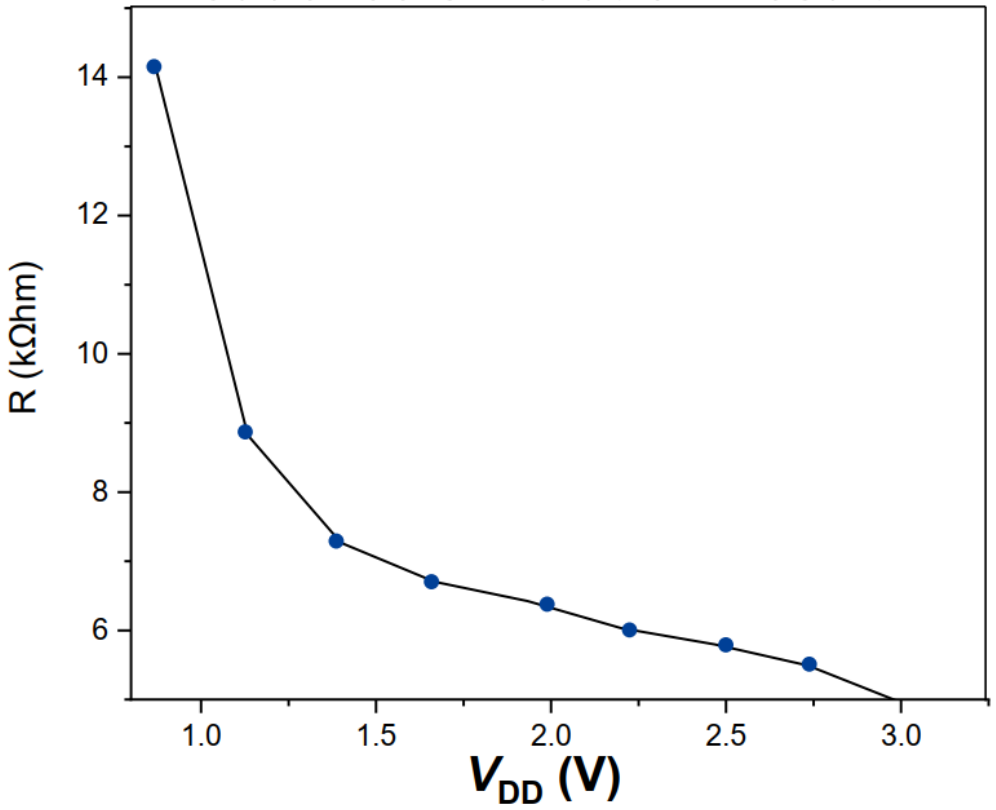
- **Method 2: Averaging**

$$R_{on} = \frac{1}{2} \left(\frac{V_{DD}}{I_{DSAT} \cdot (1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT} \cdot (1 + \lambda V_{DD}/2)} \right) \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{5}{6} \lambda V_{DD}\right)$$

R_{on} vs. V_{DD} – Simulation Results

- R_{on} increases linearly (yet with smooth slope) as V_{DD} reduces from large value.
- Tend to scale with $1/V_{DD}$ and increase dramatically as V_{DD} approaches V_T

Cadence Simulation Result



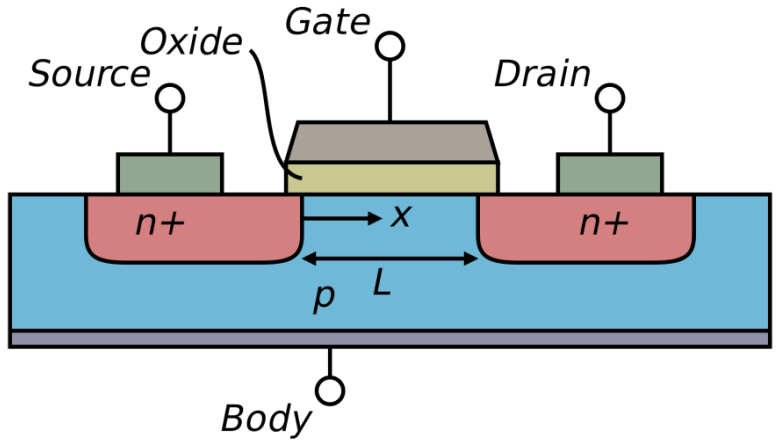
$$R_{on} = \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{7}{9}\lambda V_{DD}\right)$$

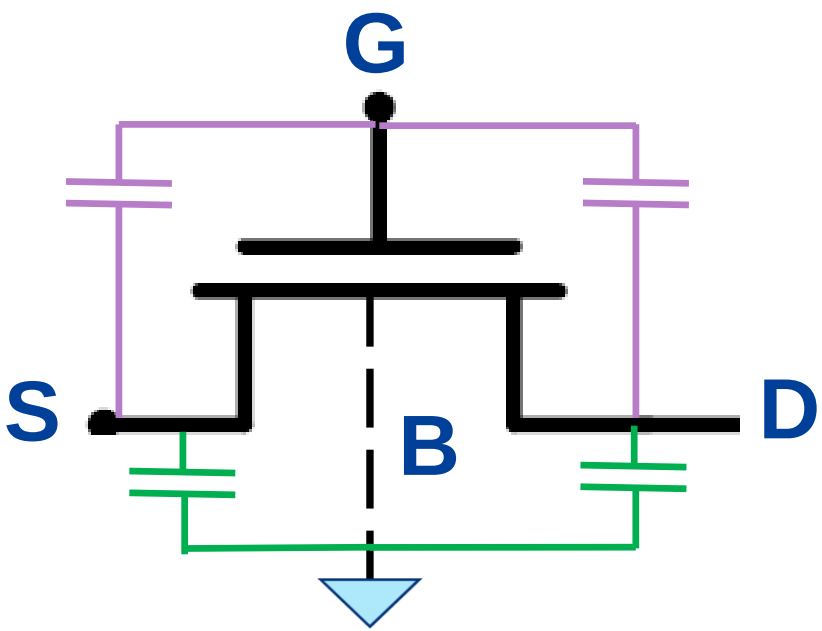
$$I_{DSAT} = \mu_n C_{ox}\cdot\frac{W}{L}\cdot\left((V_{GS}-V_T)\cdot V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$$

$(V_{GS} = V_G - V_{DD})$

- V_{DD} is large — $V_{DSAT}, V_G \ll V_{DD}$ — $I_{DSAT} \propto V_{DD}$
- V_{DD} is small — $V_{DSAT}, V_G \sim V_{DD}$ — $I_{DSAT} \propto V_{DD}^2$

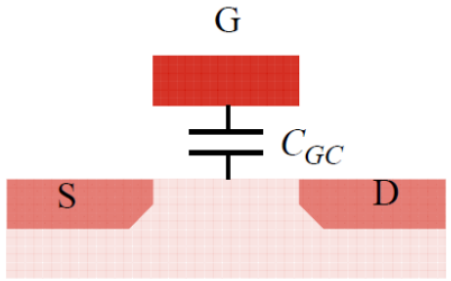
Capacitance of the MOSFET



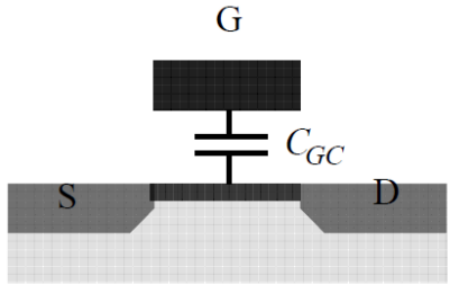


- Gate Capacitance C_{GC} – parallel capacitance.
- Parasitic Capacitance C_{SB} and C_{DB} – p-n junction diffusion capacitance.
- The capacitance counts only when the voltage across it changes during the PUN and/or PDN process.

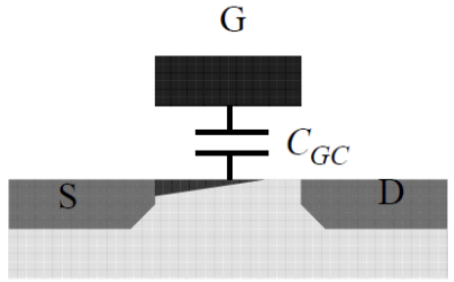
Gate Capacitance



Cut-Off



Linear/Resistive



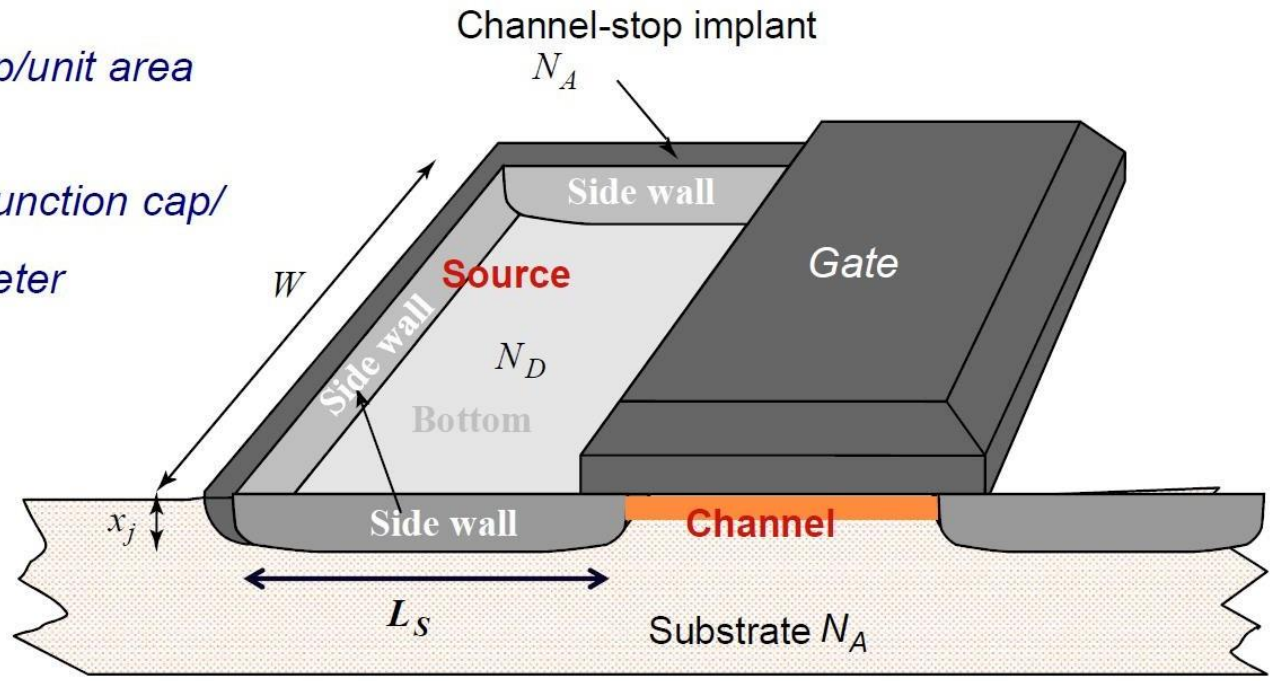
Saturation

Operation Region	C_{GCB}	C_{GCS}	C_{GCD}	C_{GC}
Cut-Off	$C_{ox}WL_{eff}$	0	0	$C_{ox}WL_{eff}$
Linear	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0	$(2/3)C_{ox}WL_{eff}$

Diffusion Capacitance

C_j junction cap/unit area

C_{jsw} side-wall junction cap/ unit perimeter

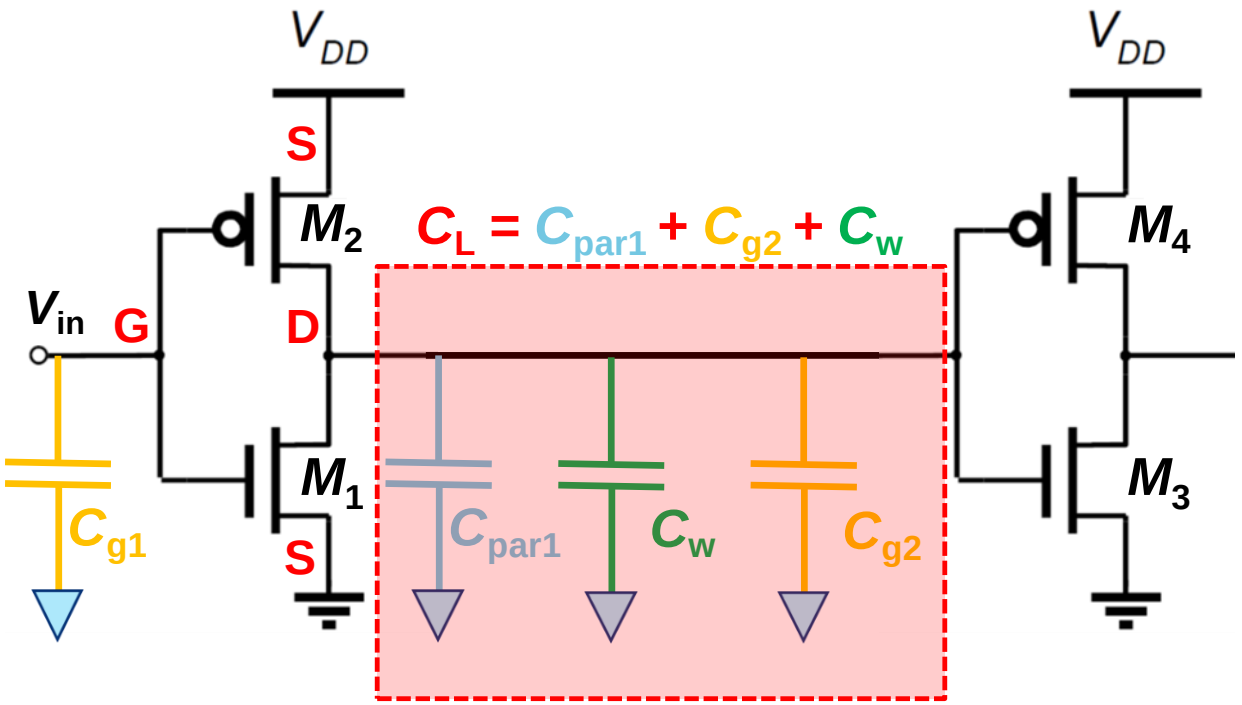


$$C_{diff} = C_{bottom} + C_{sw}$$

$$= C_j \cdot AREA + C_{jsw} \cdot PERIMETER$$ (周长)

$$= C_j \cdot L_s W + C_{jsw} \cdot (2L_S + W)$$

Capacitance in Logic Circuits



- C_{g1} – C_{GS} of M_1 and M_2.
- C_{g2} – C_{GS} of M_3 and M_4.
- C_{par1} – C_{DB} of M_1 and M_2.
- C_w – parasitic cap. of wire.

- The body terminal is always connected to GND (NMOS) or V_{DD} (PMOS).