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- *Gerez Jimenez, Juan Jose Armando*

Secuencial 16 x 16

– *Config.json*

```
{
   "DESIGN_NAME": "sequential_multiplier_16x16",
   "VERILOG_FILES": "dir::src/*.v",
   "CLOCK_PORT": "clk",
   "CLOCK_PERIOD": 10.0,
   "DESIGN_IS_CORE": true
}
```

– *Área*

Printing statistics.

```
=== sequential_multiplier_16x16 ===

   Number of wires:                253
   Number of wire bits:            314
   Number of public wires:          14
   Number of public wire bits:      75
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                280
     sky130_fd_sc_hd__a211o_2        1
     sky130_fd_sc_hd__a21bo_2        1
     sky130_fd_sc_hd__a21boi_2       1
     sky130_fd_sc_hd__a21o_2         2
     sky130_fd_sc_hd__a21oi_2       12
     sky130_fd_sc_hd__a221o_2        2
     sky130_fd_sc_hd__a22o_2         7
     sky130_fd_sc_hd__a2bb2o_2       1
     sky130_fd_sc_hd__a31o_2         5
     sky130_fd_sc_hd__a32o_2         1
     sky130_fd_sc_hd__a41o_2         1
     sky130_fd_sc_hd__and2_2        20
     sky130_fd_sc_hd__and2b_2        1
     sky130_fd_sc_hd__and3_2         5
     sky130_fd_sc_hd__and4b_2        1
     sky130_fd_sc_hd__buf_1         36
     sky130_fd_sc_hd__dfxtp_2       40
     sky130_fd_sc_hd__inv_2          7
     sky130_fd_sc_hd__mux2_2        47
     sky130_fd_sc_hd__nand2_2       17
     sky130_fd_sc_hd__nor2_2        19
     sky130_fd_sc_hd__nor3_2         1
```

sky130_fd_sc_hd__o211a_2 2
sky130_fd_sc_hd__o211ai_2 1
sky130_fd_sc_hd__o21a_2 6
sky130_fd_sc_hd__o21ai_2 6
sky130_fd_sc_hd__o221a_2 4
sky130_fd_sc_hd__o22a_2 2
sky130_fd_sc_hd__o2bb2a_2 1
sky130_fd_sc_hd__or2_2 16
sky130_fd_sc_hd__or2b_2 1
sky130_fd_sc_hd__or3_2 1
sky130_fd_sc_hd__or3b_2 1
sky130_fd_sc_hd__or4bb_2 1
sky130_fd_sc_hd__xnor2_2 4
sky130_fd_sc_hd__xor2_2 6

Chip area for module '\sequential_multiplier_16x16': 2822.707200

El área del circuito expresada en μm² es de 2822.707μm²

– Velocidad

("CLOCK_PERIOD": 10.0) * 16 ciclos = **160ns**

– Potencia

```
========================================================================
 report_power
========================================================================
======================== Typical Corner ===================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------
Sequential             2.63e-04   2.29e-04   3.38e-10   4.91e-04  45.8%
Combinational          3.89e-04   1.94e-04   7.29e-10   5.83e-04  54.2%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  6.52e-04   4.23e-04   1.07e-09   1.07e-03 100.0%
                          60.7%      39.3%       0.0%
```

<u>Secuencial 32 x 32</u>

– Config.json

```
{
   "DESIGN_NAME": "sequential_multiplier_32x32",
   "VERILOG_FILES": "dir::src/*.v",
   "CLOCK_PORT": "clk",
   "CLOCK_PERIOD": 10.0,
```

```
    "DESIGN_IS_CORE": true
}
```

– *Área*

Printing statistics.

```
=== sequential_multiplier_32x32 ===

   Number of wires:                444
   Number of wire bits:            569
   Number of public wires:          15
   Number of public wire bits:     140
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                503
     sky130_fd_sc_hd__a2111o_2       1
     sky130_fd_sc_hd__a211o_2        2
     sky130_fd_sc_hd__a21bo_2        4
     sky130_fd_sc_hd__a21boi_2       5
     sky130_fd_sc_hd__a21o_2        22
     sky130_fd_sc_hd__a21oi_2       28
     sky130_fd_sc_hd__a221o_2       35
     sky130_fd_sc_hd__a2bb2o_2       1
     sky130_fd_sc_hd__a311o_2        1
     sky130_fd_sc_hd__a31o_2         5
     sky130_fd_sc_hd__a31oi_2        1
     sky130_fd_sc_hd__and2_2        22
     sky130_fd_sc_hd__and2b_2        1
     sky130_fd_sc_hd__and3_2         4
     sky130_fd_sc_hd__and3b_2        1
     sky130_fd_sc_hd__and4_2         3
     sky130_fd_sc_hd__buf_1         43
     sky130_fd_sc_hd__dfxtp_2       73
     sky130_fd_sc_hd__inv_2          5
     sky130_fd_sc_hd__mux2_2        29
     sky130_fd_sc_hd__nand2_2       47
     sky130_fd_sc_hd__nand3_2        1
     sky130_fd_sc_hd__nor2_2        28
     sky130_fd_sc_hd__nor3_2         2
     sky130_fd_sc_hd__o211a_2        9
     sky130_fd_sc_hd__o21a_2        37
     sky130_fd_sc_hd__o21ai_2       13
     sky130_fd_sc_hd__o21ba_2        1
     sky130_fd_sc_hd__o221a_2       15
     sky130_fd_sc_hd__o22a_2         1
     sky130_fd_sc_hd__o311a_2        1
     sky130_fd_sc_hd__o31a_2         3
     sky130_fd_sc_hd__or2_2         27
     sky130_fd_sc_hd__or2b_2         6
     sky130_fd_sc_hd__or3_2          1
```

```
    sky130_fd_sc_hd__or3b_2         2
    sky130_fd_sc_hd__or4_2          1
    sky130_fd_sc_hd__xnor2_2        15
    sky130_fd_sc_hd__xor2_2         7
```

Chip area for module '\sequential_multiplier_32x32': 5213.750400

El área del circuito expresada en μm² es de 5213.7504 μm²

– Velocidad

("CLOCK_PERIOD": 10.0) * 32 ciclos = **320ns**

– Potencia

```
=========================================================================
 report_power
=========================================================================
======================== Typical Corner ===================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------
Sequential             4.99e-04   4.58e-04   6.16e-10   9.56e-04  41.8%
Combinational          8.51e-04   4.82e-04   1.30e-09   1.33e-03  58.2%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  1.35e-03   9.40e-04   1.92e-09   2.29e-03 100.0%
                          59.0%      41.0%       0.0%
```

Combinacional 16 x 16

– Config.json

```
{
   "DESIGN_NAME": "combinational_multiplier_16x16",
   "VERILOG_FILES": "dir::src/*.v",
   "CLOCK_PORT": "clk",
   "CLOCK_PERIOD": 20.0,
   "DESIGN_IS_CORE": true
}
```

Nota: Subimos el periodo del reloj ya que con 10.0ns el flujo fallaba

– Área

Printing statistics.

=== combinational_multiplier_16x16 ===

Number of wires: 1370
Number of wire bits: 1431
Number of public wires: 3
Number of public wire bits: 64
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 1399
sky130_fd_sc_hd__a211o_2 31
sky130_fd_sc_hd__a211oi_2 21
sky130_fd_sc_hd__a21bo_2 47
sky130_fd_sc_hd__a21boi_2 7
sky130_fd_sc_hd__a21o_2 104
sky130_fd_sc_hd__a21oi_2 47
sky130_fd_sc_hd__a221o_2 1
sky130_fd_sc_hd__a22o_2 68
sky130_fd_sc_hd__a22oi_2 33
sky130_fd_sc_hd__a2bb2o_2 4
sky130_fd_sc_hd__a311o_2 1
sky130_fd_sc_hd__a31o_2 15
sky130_fd_sc_hd__a31oi_2 5
sky130_fd_sc_hd__a32o_2 3
sky130_fd_sc_hd__a32oi_2 3
sky130_fd_sc_hd__and2_2 50
sky130_fd_sc_hd__and2b_2 38
sky130_fd_sc_hd__and3_2 54
sky130_fd_sc_hd__and3b_2 3
sky130_fd_sc_hd__and4_2 46
sky130_fd_sc_hd__and4b_2 5
sky130_fd_sc_hd__and4bb_2 8
sky130_fd_sc_hd__buf_1 94
sky130_fd_sc_hd__inv_2 13
sky130_fd_sc_hd__nand2_2 94
sky130_fd_sc_hd__nand2b_2 2
sky130_fd_sc_hd__nand3_2 92
sky130_fd_sc_hd__nand4_2 50
sky130_fd_sc_hd__nor2_2 68
sky130_fd_sc_hd__nor3_2 9
sky130_fd_sc_hd__nor3b_2 5
sky130_fd_sc_hd__nor4_2 3
sky130_fd_sc_hd__nor4b_2 1
sky130_fd_sc_hd__o2111a_2 2
sky130_fd_sc_hd__o211a_2 27
sky130_fd_sc_hd__o211ai_2 24
sky130_fd_sc_hd__o21a_2 17
sky130_fd_sc_hd__o21ai_2 18
sky130_fd_sc_hd__o21ba_2 20
sky130_fd_sc_hd__o21bai_2 4
sky130_fd_sc_hd__o22a_2 3
sky130_fd_sc_hd__o22ai_2 2
sky130_fd_sc_hd__o2bb2a_2 10

```
    sky130_fd_sc_hd__o31a_2        3
    sky130_fd_sc_hd__o31ai_2       1
    sky130_fd_sc_hd__o32ai_2       1
    sky130_fd_sc_hd__or2_2        33
    sky130_fd_sc_hd__or2b_2       21
    sky130_fd_sc_hd__or3_2        16
    sky130_fd_sc_hd__or3b_2        5
    sky130_fd_sc_hd__or4_2         3
    sky130_fd_sc_hd__or4b_2        1
    sky130_fd_sc_hd__or4bb_2       2
    sky130_fd_sc_hd__xnor2_2     112
    sky130_fd_sc_hd__xor2_2       49
```

Chip area for module '\combinational_multiplier_16x16': 13435.385600

El área del circuito expresada en μm² es de 13435.3856 μm²

– *Velocidad*

```
===========================================================================
report_checks -unconstrained
===========================================================================
======================== Typical Corner ===================================

Startpoint: mcand[10] (input port clocked by clk)
Endpoint: product[30] (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout     Cap    Slew   Delay    Time   Description
---------------------------------------------------------------------------

                  0.00   20.00   20.00   clock clk (rise edge)
                         0.00   20.00   clock network delay (ideal)
                        -0.25   19.75   clock uncertainty
                         0.00   19.75   clock reconvergence pessimism
                        -4.00   15.75   output external delay
                                15.75   data required time
---------------------------------------------------------------------------
                                15.75   data required time
                               -10.75   data arrival time
---------------------------------------------------------------------------
                                 5.00   slack (MET)
```

– *Potencia*

```
===========================================================================
 report_power
===========================================================================
======================== Typical Corner ===================================
```

Group	Internal Power	Switching Power	Leakage Power	Total Power (Watts)	
Sequential	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Combinational	5.11e-04	5.78e-04	5.14e-09	1.09e-03	100.0%
Macro	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Total	**5.11e-04**	**5.78e-04**	**5.14e-09**	**1.09e-03**	**100.0%**
	46.9%	53.1%	0.0%		

Combinacional 32 x 32

– *Config.json*

```
{
   "DESIGN_NAME": "combinational_multiplier_32x32",
   "VERILOG_FILES": "dir::src/*.v",
   "CLOCK_PORT": "clk",
   "CLOCK_PERIOD": 20.0,
   "DESIGN_IS_CORE": true
}
```

Nota: Subimos el periodo del reloj ya que con 10.0ns el flujo fallaba

– *Área*

Printing statistics.

=== combinational_multiplier_32x32 ===

```
   Number of wires:               5703
   Number of wire bits:           5828
   Number of public wires:           3
   Number of public wire bits:     128
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:               5764
     sky130_fd_sc_hd__a2111o_2       1
     sky130_fd_sc_hd__a2111oi_2      1
     sky130_fd_sc_hd__a211o_2      167
     sky130_fd_sc_hd__a211oi_2     170
     sky130_fd_sc_hd__a21bo_2      167
     sky130_fd_sc_hd__a21boi_2      18
     sky130_fd_sc_hd__a21o_2       358
     sky130_fd_sc_hd__a21oi_2      187
     sky130_fd_sc_hd__a221oi_2       1
     sky130_fd_sc_hd__a22o_2       357
     sky130_fd_sc_hd__a22oi_2       96
```

sky130_fd_sc_hd__a2bb2o_2 11
sky130_fd_sc_hd__a2bb2oi_2 6
sky130_fd_sc_hd__a31o_2 54
sky130_fd_sc_hd__a31oi_2 9
sky130_fd_sc_hd__a32o_2 65
sky130_fd_sc_hd__a32oi_2 1
sky130_fd_sc_hd__a41o_2 11
sky130_fd_sc_hd__and2_2 165
sky130_fd_sc_hd__and2b_2 109
sky130_fd_sc_hd__and3_2 243
sky130_fd_sc_hd__and3b_2 15
sky130_fd_sc_hd__and4_2 165
sky130_fd_sc_hd__and4b_2 13
sky130_fd_sc_hd__and4bb_2 45
sky130_fd_sc_hd__buf_1 433
sky130_fd_sc_hd__inv_2 70
sky130_fd_sc_hd__mux2_2 1
sky130_fd_sc_hd__nand2_2 366
sky130_fd_sc_hd__nand3_2 334
sky130_fd_sc_hd__nand3b_2 3
sky130_fd_sc_hd__nand4_2 259
sky130_fd_sc_hd__nand4b_2 1
sky130_fd_sc_hd__nor2_2 194
sky130_fd_sc_hd__nor3_2 71
sky130_fd_sc_hd__nor3b_2 4
sky130_fd_sc_hd__nor4_2 22
sky130_fd_sc_hd__o2111ai_2 1
sky130_fd_sc_hd__o211a_2 179
sky130_fd_sc_hd__o211ai_2 154
sky130_fd_sc_hd__o21a_2 63
sky130_fd_sc_hd__o21ai_2 76
sky130_fd_sc_hd__o21ba_2 29
sky130_fd_sc_hd__o21bai_2 16
sky130_fd_sc_hd__o22a_2 11
sky130_fd_sc_hd__o22ai_2 18
sky130_fd_sc_hd__o2bb2a_2 42
sky130_fd_sc_hd__o311a_2 1
sky130_fd_sc_hd__o311ai_2 3
sky130_fd_sc_hd__o31a_2 5
sky130_fd_sc_hd__o32a_2 2
sky130_fd_sc_hd__o32ai_2 2
sky130_fd_sc_hd__or2_2 168
sky130_fd_sc_hd__or2b_2 97
sky130_fd_sc_hd__or3_2 69
sky130_fd_sc_hd__or3b_2 11
sky130_fd_sc_hd__or4_2 23
sky130_fd_sc_hd__or4b_2 2
sky130_fd_sc_hd__or4bb_2 15
sky130_fd_sc_hd__xnor2_2 352
sky130_fd_sc_hd__xor2_2 232

Chip area for module '\combinational_multiplier_32x32': 55353.088000

El área del circuito expresada en μm² es de 55353.088 μm²

– *Velocidad*

```
============================================================================
report_checks -unconstrained
============================================================================
======================= Typical Corner ===================================

Startpoint: mplier[25] (input port clocked by clk)
Endpoint: product[63] (output port clocked by clk)
Path Group: clk
Path Type: max

  Fanout     Cap    Slew   Delay    Time   Description
---------------------------------------------------------------------------

                          0.00   20.00   20.00   clock clk (rise edge)
                          0.00   20.00   clock network delay (ideal)
                         -0.25   19.75   clock uncertainty
                          0.00   19.75   clock reconvergence pessimism
                         -4.00   15.75   output external delay
                                 15.75   data required time
---------------------------------------------------------------------------
                                 15.75   data required time
                                -13.40   data arrival time
---------------------------------------------------------------------------
                                  2.35   slack (MET)
```

– *Potencia*

```
============================================================================
 report_power
============================================================================
======================= Typical Corner ===================================

Group                  Internal  Switching    Leakage      Total
                       Power     Power        Power        Power (Watts)
----------------------------------------------------------------
Sequential             0.00e+00  0.00e+00     0.00e+00     0.00e+00   0.0%
Combinational          3.43e-03  4.11e-03     2.10e-08     7.54e-03 100.0%
Macro                  0.00e+00  0.00e+00     0.00e+00     0.00e+00   0.0%
Pad                    0.00e+00  0.00e+00     0.00e+00     0.00e+00   0.0%
----------------------------------------------------------------
Total                  3.43e-03  4.11e-03     2.10e-08     7.54e-03 100.0%
                       45.6%     54.4%        0.0%
```