Revision History

Project: helix_4

Description:
Embedded Cyclone IV Module
DDR2, SRAM, Cyclone IV F256 package 6,10,15,22 KLE Densities Linear Power

Revision History

Rev A	B. Singer	17/01/2013	Many changes to pinout, added BA2 to allow 1Gbit DRAM ICs, switched sram IO11 & A17 pins, added 0.2mm to outer dimensions.
Rev B	B. Singer	20/02/2013	Moved PLL4 +2 pins, simplified SRAM pinning to add better test coverage Swapped naming of clkin left/right to reflect pin numbering better. PCB released.
Rev C	B. Singer	08/04/2013	Removed gnd pad from design for reliability reasons. Another pinning redesign.
Rev D	B. Singer	18/05/2014	Prepared relase for Open Source

Notes

Compatible FPGA PNs
EP4CEaaF17xyz
aa = 6, 10, 15 or 22
x = C or I
y = 6, 7, 8 or 9
z = N for RoHS, otherwise Non-Rohs Leaded
Package is F17 1mm pitch 256 ball, 16 rows and 16 columns

PCB Technology
5mil trace, 5mil space
4 Layers
No impedance control
Via holes are 8mil drilled and plated
Via annular ring diameter is 18mil
Max fill - any board space not routed contains GND or power fills
Care is taken to manage return currents and avoid slot antennae

DDR2 Layout
Traces are very short with no stubs
No termination or matching is required
ODT may be used on the device, but is not necessary

Power
All power is linear
1V2, 1V8 and 2V5 supplies are 150mA regs
3V3 supply is 1A

Decoupling
At the time of writing all 0402 1uF Caps were Digikey PN 587-1231-2-ND
Note there are two different types of 0402 ferrite, one for high power, and one for low power with better filtering properties.

License and Conditions of Use

helix_4 Module Project Title Page

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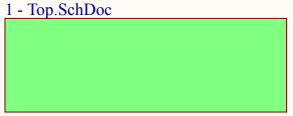


LOGO

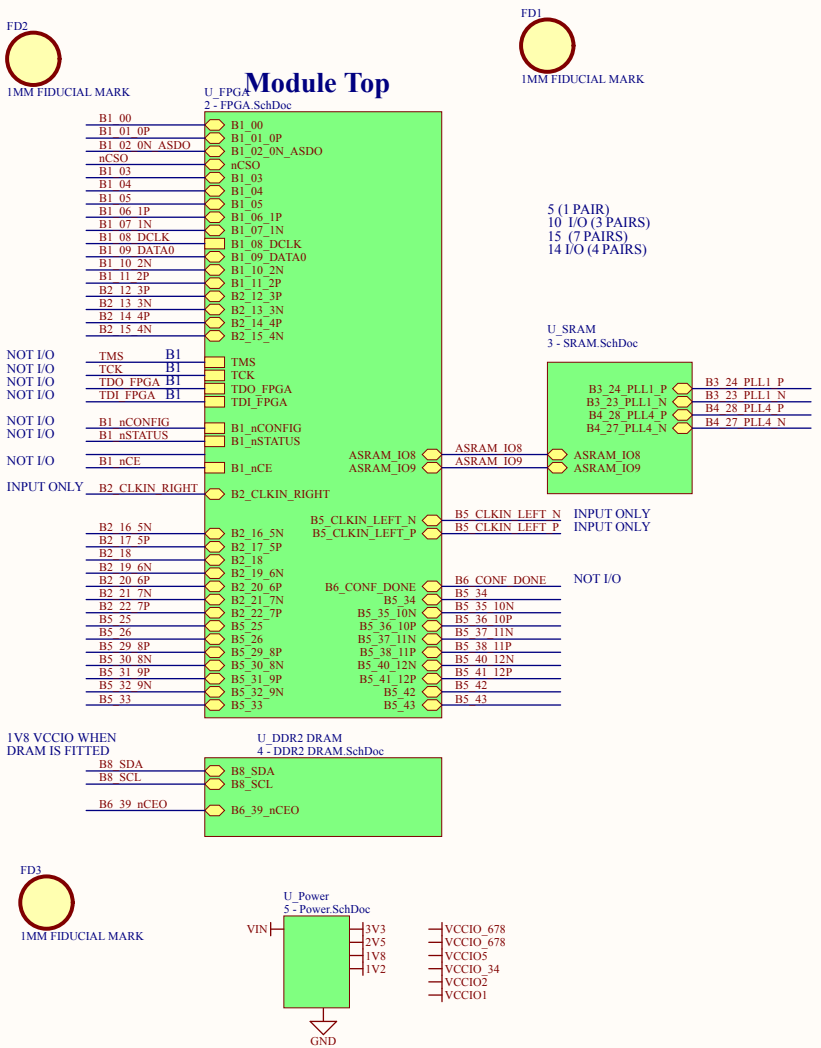
LOGO

Support

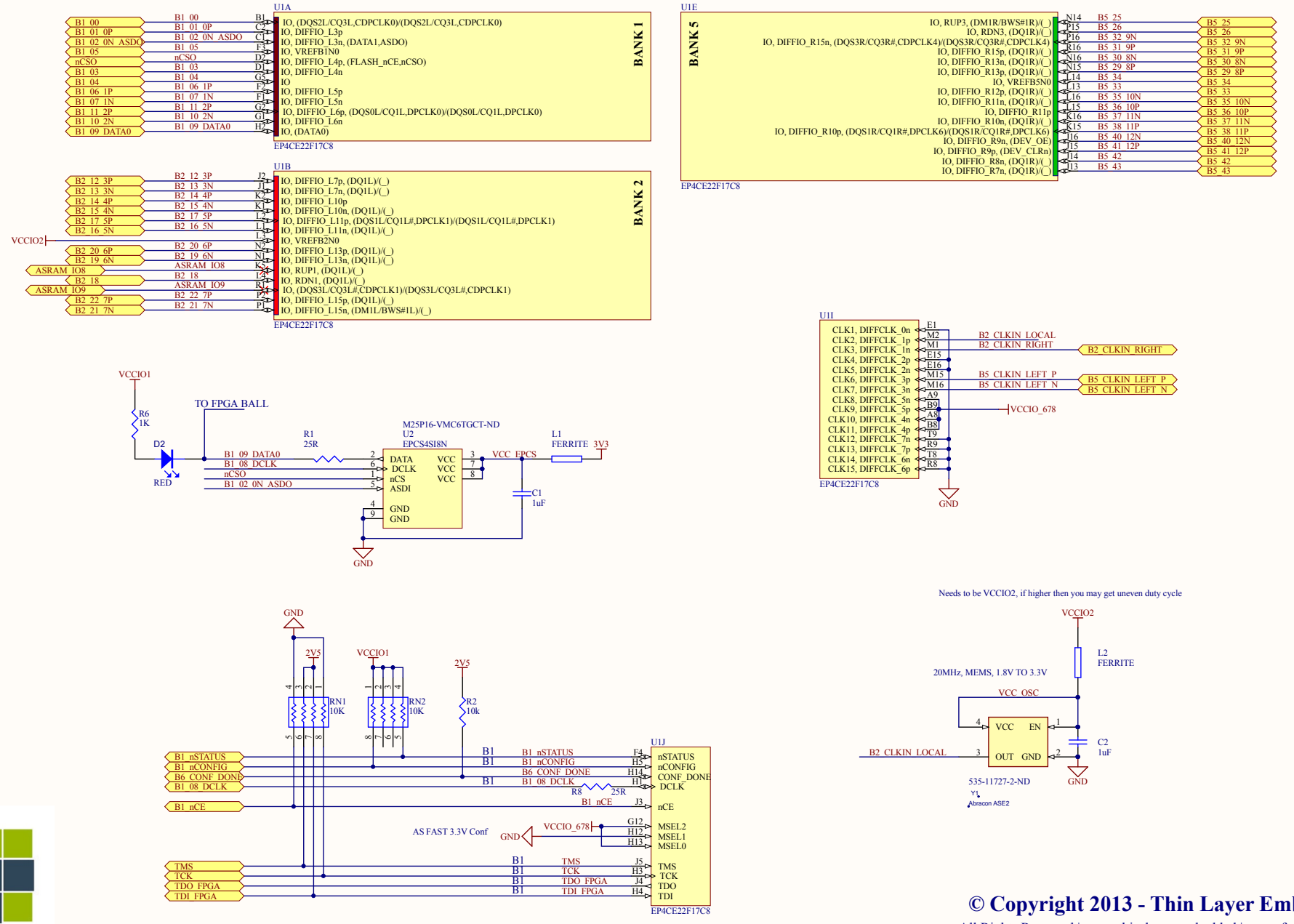
Support material for this project can be found at:
www.thin-layer-embedded.com

Or email:
support@thin-layer-embedded.com

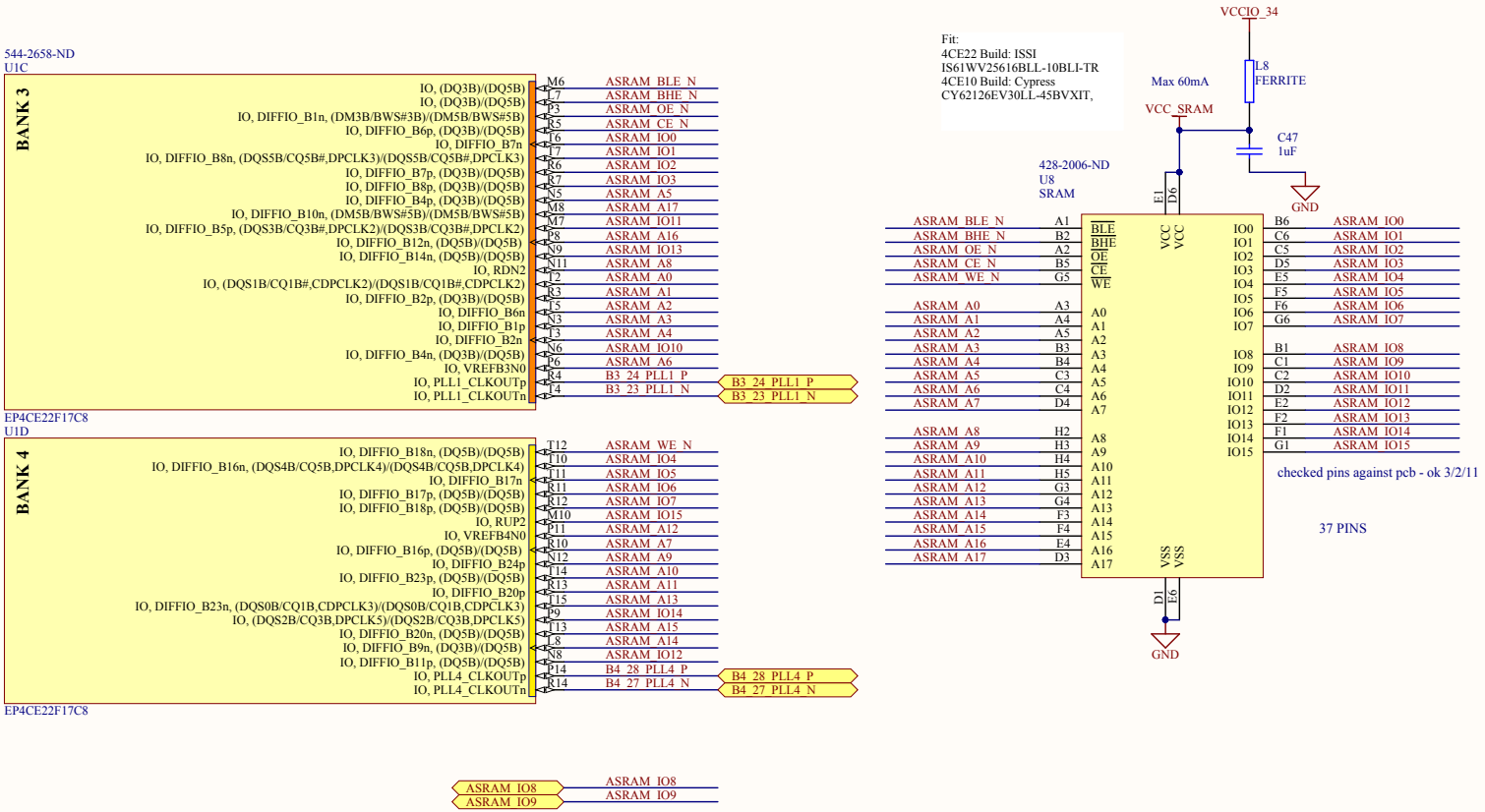
This project is supplied with out any warranty or claims of suitability for any purpose. Support may limited, and the user should take this account before using this design.



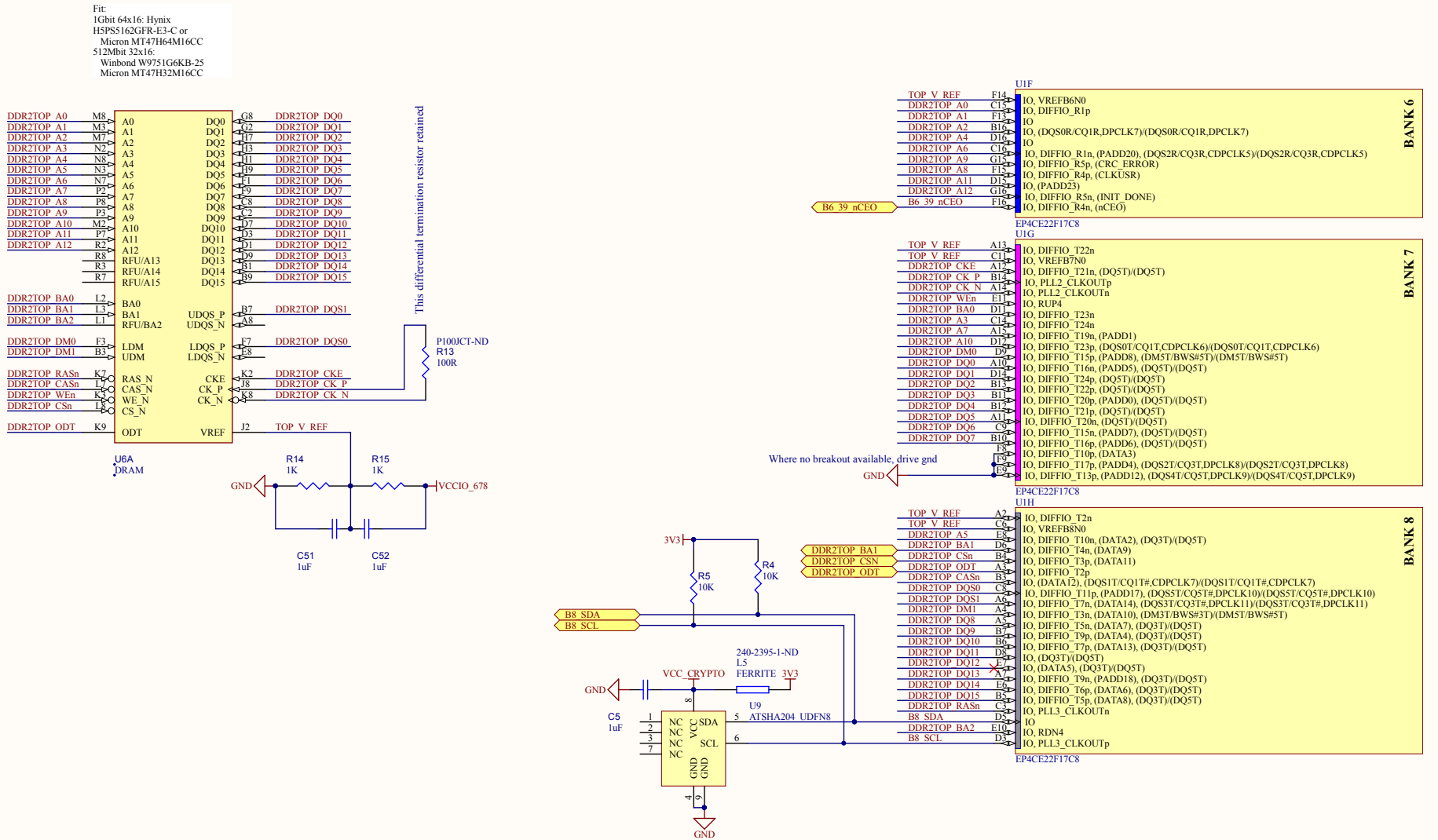
FPGA, Altera EP4CExxF17 - 8 or 9L Speed Grades Only



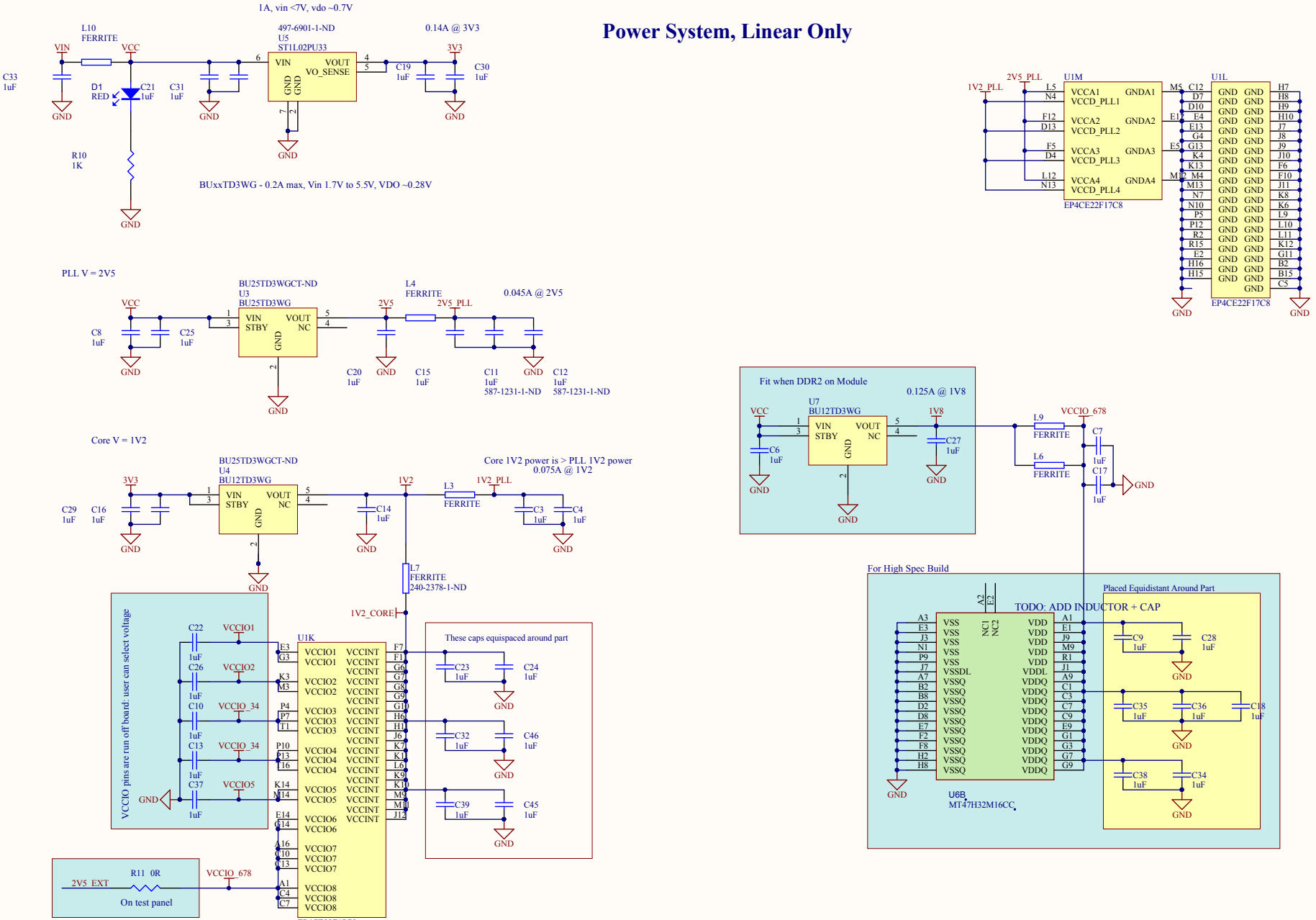
SRAM, 128kByte Asynchronous



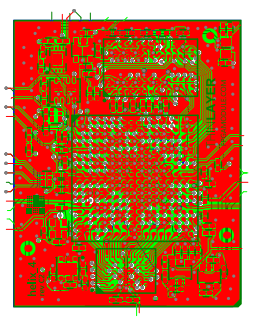
DRAM, 64Mbytes DDR2, up to 167MHz



Power System, Linear Only



NB. IF YOU SEE SOMETHING WEIRD,
A DESIGN FEATURE THAT DOESN'T
IMMEDIATELY MAKE SENSE, REMEMBER
THAT THIS DESIGN WAS FOR A MODULE
AND THIS CONSTRAINED THE LAYOUT
SEVERLY. SO YOU CAN SAFELY DELETE
MOST THINGS YOU DON'T LIKE HERE.



HELIX_4 REV C2 RELEASE FOR OPEN SOURCE
  B.SINGER - PASS DRC ON 19-05-2014
  RELEASED 19-MAY-2014

BOARD NOTES:
  MATERIAL:
    4 LAYERS
    SINGLE CORE + FOIL
    5MIL TRACE / 5MIL CLEARANCE
    1.0MM FINISHED THICKNESS
    FR4 TG170
    NO IMPEDANCE CONTROL

  PAD FINISH:
    ENIG GOLD

Layer Stackup
  TOP SILK

  TOP COPPER LAYER
  MID-TOP COPPER LAYER
  MID-BOT COPPER LAYER
  BOTTOM COPPER LAYER

  NOTE: THERE IS NO BOTTOM SILK OR PASTE

BOARD FINISH
  TOP PASTE / SILK ONLY - USE *BLACK* SILK MARKING
  TOP / BOT SOLDER MASK
  YELLOW DRY FILM OR WET PHOTO-IMAGABLE SOLDER MASK
  MAX SOLDER MASK THICKNESS 3MIL

CLOCKS
  TWO CLOCK RULES HAVE BEEN MADE, AND ARE TURNED
  ON DURING POLY POURS. IT'S NOT POSSIBLE TO PASS DRC
  WITH THE RULES ENABLED. SO TURN THEM OFF FOR DRC

POWER
  POWER TO VCCIO BANKS IS GENERALLY NOT CONNECTED
  ALL VCCIOx NETS NEED TO CONNECT TO A VOLTAGE RAIL
  FOLLOW THE CYCLONE IV PIN CONNECTION GUIDELINES

Mechanical Layers

  PCB OUTLINES
  PANEL OUTLINE
  FAB NOTES