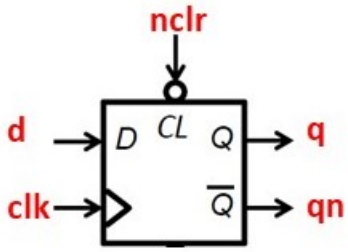
FUNDAMENTOS DE COMPUTADORES I
CUADERNO DE LA PRÁCTICA 3

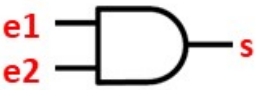
```
ENTITY ffd IS
PORT( clk, d, nclr: in bit; q, qn : out bit );
END ffd;

ARCHITECTURE comportamiento OF ffd IS
BEGIN
PROCESS(clk,nclr)
BEGIN
IF (nclr='0') THEN
q <= '0';
ELSIF (clk'event and clk='1') THEN q <= d;
qn <= not d;
END IF;
END PROCESS;
END comportamiento;
```

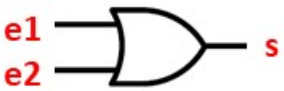



```
ENTITY and3 IS
 PORT(e1, e2, e3 : IN bit ; s: OUT bit);
END and3;
ARCHITECTURE comportamiento OF and3 IS
BEGIN
 s <= e1 AND e2 AND e3;
END comportamiento;
```

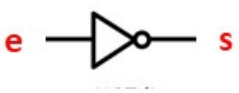

```
ENTITY and2 IS
 PORT(e1, e2 : IN bit; s : OUT bit);
END and2;
ARCHITECTURE comportamiento OF and2 IS
BEGIN
 s <= e1 AND e2;
END comportamiento;
```



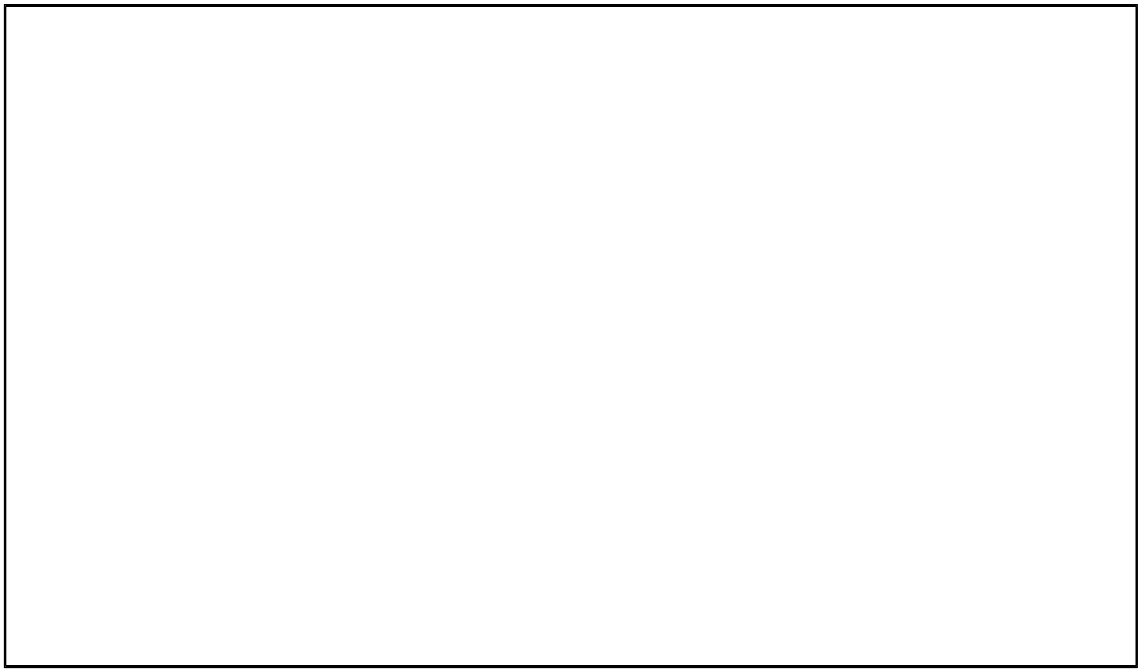

```
ENTITY or2 IS
 PORT(e1, e2 : IN bit; s : OUT bit);
END or2;
ARCHITECTURE comportamiento OF or2 IS
BEGIN
 s <= e1 OR e2;
END comportamiento;
```




```
ENTITY inv IS
 PORT(e : IN bit; s : OUT bit);
END inv;
ARCHITECTURE comportamiento OF inv IS
BEGIN
 s <= NOT e;
END comportamiento;
```



Esquema gráfico de interconexión del reconocedor



Código VHDL del reconocedor