CS 3853: Computer Architecture
Midterm -1
Spring 2014
February 25, 2014
Total Marks: 50
Time: 1 hour 15 min

Name:
Banner Id:
Alias:

1. [10 pt] Indicate **True** or **False** for the following statements:

   - A MIPS 5 stage pipeline does not have WAW hazards but it can have WAR hazards.
   - Every data dependence always leads to a hazard in a pipeline.
   - If 20% of a program cannot be parallelized, then the maximum speed up that can be achieved through parallelization is 5.
   - The higher the value of IPC, the better it is.
   - In a precise exception, no instructions after the exception causing instruction can complete before the exception is handled.
   - Performance of a machine is proportional to its execution time.
   - Usually arithmetic mean is not used to summarize performance of a benchmark suite.
   - Ideal CPI of a MIPS 5 stage pipelined processor is 1.
   - In a multi cycle FP pipeline, instructions does not complete out of order.
   - In a delayed branch, the delay slot instruction is not executed if the branch is taken.

2. [15 pt] CPU performance and Amdahl's law:

   (a) [6 pt] Suppose you can apply two enhancements - enh_1 and enh_2. enh_1 can be applied to 30% of the program whereas enh_2 can be applied to 20% of the program. Suppose the speed ups of the enhancements are 2.5 and 3.0 respectively.

      i. How much will be the overall speed up when only enh_1 is applied?

      ii. How much will be the overall speed up when only enh_2 is applied?

      iii. How much will be the overall speed up if you apply both enhancements together?

      iv. What is the maximum speed up of the program?

(b) [9 pt] Suppose we have made the following measurements:

- Frequency of FP operations = 25%
- Average CPI of FP operations = 4.0
- Average CPI of other instructions = 1.33

In order to improve performance, an architect proposes to decrease the average CPI of all FP operations to 2.5.

i. What is the CPI of the original design?

ii. What is the CPI of proposed scheme?

iii. What is the speed up of the proposed scheme?

3. [25 pt] For this question, let us assume a classic 5 stage MIPS pipeline where the branch is resolved in ID stage. Consider the following code fragment:

```
LD R1, 0(R4)
L1:ADD R3, R1, R2
ADD R3, R3, R3
SD R3, -4(R4)
SUB R4, R4, #8
BNEQZ R4, L1
```

(a) [1 pt] If the initial value of R4 is 48, then how many times the branch will be taken?

(b) [6 pt] List all the immediate dependences in code.

(c) [7 pt] Assume that the pipeline does not have any forwarding support, branches are handled by stalling, and the initial value of R4 is 16. Show the pipeline timing diagram for up to the first instruction of the second iteration of the loop.

Ins	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
LD R1, 0(R4)																					
L1:ADD R3, R1, R2																					
ADD R3, R3, R3																					
SD R3, -4(R4)																					
SUB R4, R4, #8																					
BNEQZ R4, L1																					
LD R1, 0(R4)																					

(d) [7 pt] Assume that the pipeline has full forwarding support, branches are handled using static predict untaken strategy, and the initial value of R4 is 16. Show the pipeline timing diagram for up to the first instruction of the second iteration of the loop

Ins	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
LD R1, 0(R4)																					
L1:ADD R3, R1, R2																					
ADD R3, R3, R3																					
SD R3, -4(R4)																					
SUB R4, R4, #8																					
BNEQZ R4, L1																					
LD R1, 0(R4)																					

(e) [4 pt] Let us assume that the probability of a load immediately followed by a dependent ALU instruction is 10%. Also assume that the probability of a load immediately followed by dependent branch is 3%. A load is never followed by an immediate store instruction. What is the load penalty?