CS 3853: Computer Architecture
Homework 4 Solution

Name:
Banner Id:
Alias:

1. [20 pt] Memory hierarchy:
   Let us assume a 2-way set associative 128 KB L1 cache with LRU replacement policy. The cache implements write back and no write allocate policy. Cache block size is 16 Byte. Page size is 64 KB. The system has a direct mapped TLB with16 entries. TLB also implements LRU policy. Virtual address is 24 bit and physical address is 20 bit long. The cache is virtually indexed and physically tagged.

   (a) [2 pt] How many entries are there in the page table?
   Ans. 2^8 entries.

   (b) [2 pt] How many physical pages are there?
   Ans. 2^4 entries.

   (c) [2 pt] How many bits are used for TLB index and tag?
   Ans. 4 bits for index and 4 bits for tag.

   (d) [2 pt] How many bits are used for cache index and tag?
   Ans. 12 bits for index and 4 bits for tag.

(e) [12 pt] Please fill up the following the table. All numbers are in hexadecimal.

Addr R/W	Binary Addr	TLB Tag	TLB Index	TLB Hit	Physical Addr	Cache Index	Cache Tag	Found Way
16103A W	00010110000100000111010	1	6	m	4103A	103	4	-
17113C R	00010111000100010111100	1	7	m	8113C	113	8	M(0)
26112B R	00100110000100010101011	2	6	m	7112B	112	7	M(0)
16103B R	00010110000100000111011	1	6	m	4103B	103	4	M(0)
16103C W	00010110000100000111100	1	6	h	4103C	103	4	H(0)
23113D R	00100011000100010111101	2	3	m	6113D	113	6	M(1)
26103A R	00100110000100000111010	2	6	m	7103A	103	7	M(1)
17113D R	00010111000100010111101	1	7	h	8113D	113	8	H(0)

Table 1: Memory access sequence.

Virtual Page	Physical Page
16	4
17	8
23	6
26	7

Table 2: Partial Page Table

TLB Index	TLB Tag	Physical Page	V
3			
6			
7			

Table 3: TLB

Except for TLB Hit and Found Way, each number is worth 0.25 point. TLB hit and Found way is worth 0.125 point each.