CS 3853: Computer Architecture
Homework 4
Due: April 28, 2017

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1. [20 pt] Memory hierarchy:

Let us assume a 2-way set associative 128 KB L1 cache with LRU replacement policy. The cache implements write back and no write allocate policy. Cache block size is 16 Byte. Page size is 64 KB. The system has a direct mapped TLB with16 entries. TLB also implements LRU policy. Virtual address is 24 bit and physical address is 20 bit long. The cache is virtually indexed and physically tagged.

(a) [2 pt] How many entries are there in the page table?

Page size : $64\,KB = 2^{16}$, virtual addres : 2^{24}

entries : $\frac{2^{24}}{2^{16}} = 2^8 = 256$

(b) [2 pt] How many physical pages are there?

physical addrs: 2^{20} =) $\frac{2^{20}}{2^{16}} = 2^4 = 16$

(c) [2 pt] How many bits are used for TLB index and tag?

- TLB index : $\log_2(16) = 4$ bits
- tag = 8 − 4 = 4 bits

(d) [2 pt] How many bits are used for cache index and tag?

offset = $\log_2(16) = 4$

catches = $\frac{2^{17}}{2 \times 2^4} = 2^{12}$

=) - tag = 20 - 12 - 4 = 4 bits

1 - index = 12 bits

(e) [12 pt] Please fill up the following the table. All numbers are in hexadecimal.

Addr R/W	Binary Addr	TLB Tag	TLB Index	TLB Hit	Physical Addr	Cache Index	Cache Tag	Found Way
16103A W	000101100001000000111010	1	6	miss	4103A	103	4	m
17113C R	000101110001000100111100	1	7	miss	8113C	113	8	m
26112B R	001001100001000100101011	2	6	miss	7112B	112	7	m
16103B R	000101100001000000111011	1	6	hit	4103B	103	4	H
16103C W	000101100001000000111100	1	6	hit	4103C	103	4	H
23113D R	001000110001000100111101	2	3	miss	6113D	113	6	m
26103A R	001001100001000000111010	2	6	miss	7103A	103	7	m
17113D R	000101110001000100111101	1	7	hit	8113D	113	8	H

Table 1: Memory access sequence

Virtual Page	Physical Page
16	4
17	8
23	6
26	7

Table 2: Partial Page Table

TLB Index	TLB Tag	Physical Page	V
3	2	6	1
6	2	7	1
7	1	8	1

Table 3: TLB