Recitation 6

CS 3853: Computer Architecture

Tomasulo's Algorithm

The pipeline functional units are described by the following table

FU Type	Cycles in Ex	# of Ex Units	# of Reservation Stations
Integer	1	1	4
FP Add/Sub	4	1	4
FP Mult/Div	10	2	4

Assume 1 inst of any type can commit/cycle
Assume 1 CDB

Single Issue & No Speculation

Instruction	Reservation Station	Exec FU	Issue	Exec begin-end	Mem Access	CDB write
LD F2, 0(R1)	int1	int	1	2	3	4
MUL.D F4, F2, F0						
LD F4, 4(R1)						
SD F4 8(R1)						
MUL.D F6, F4, F1						
ADD.D F6, F4, F2						
DSUBUI R1, R1, #8						
BEQZ R1, **L1**						
LD F2, 8(R1)						
LD F1, 0(R1)						
MUL.D F4, F2, F0						

Single Issue & No Speculation

Instruction	Reservation Station	Exec FU	Issue	Exec begin-end	Mem Access	CDB write
LD F2, 0(R1)	int1	int	1	2	3	4
MUL.D F4, F2, F0	mult1	md1	2	5-14		15
LD F4, 4(R1)	Int2	int	3	4	5	6
SD F4 8(R1)	Int3	int	4	5	7	
MUL.D F6, F4, F1	mult2	md2	5	7-16		17
ADD.D F6, F4, F2	add1	as1	6	7-10		11
DSUBUI R1, R1, #8	int1	int	7	8		9
BEQZ R1, **L1**	int2	int	8	10		
LD F2, 8(R1)	int3	int	9	11	12	13
LD F1, 0(R1)	int1	int	10	12	13	14
MUL.D F4, F2, F0	mult3	md1	11	15-24		25

Single Issue With Speculation

Instruction	Reservation Station	Exec FU	Issue	Exec begin-end	Mem Access	CDB write	Commit/ Mem Wrt
LD F2, 0(R1)	int1	int	1	2	3	4	5
MUL.D F4, F2, F0							
LD F4, 4(R1)							
SD F4 8(R1)							
MUL.D F6, F4, F1							
ADD.D F6, F4, F2							
DSUBUI R1, R1, #8							
BEQZ R1, **L1**							
LD F2, 8(R1)							
LD F1, 0(R1)							
MUL.D F4, F2, F0							

Single Issue With Speculation

Instruction	Reservation Station	Exec FU	Issue	Exec begin-end	Mem Access	CDB write	Commit/ Mem Wrt
LD F2, 0(R1)	int1	int	1	2	3	4	5
MUL.D F4, F2, F0	mult1	md1	2	5-14		15	16
LD F4, 4(R1)	Int2	int	3	4	5	6	17
SD F4 8(R1)	Int3	int	4	5	7		18
MUL.D F6, F4, F1	mult2	md2	5	7-16		17	19
ADD.D F6, F4, F2	add1	as1	6	7-10		11	20
DSUBUI R1, R1, #8	int1	int	7	8		9	21
BEQZ R1, **L1**	int2	int	8	10			22
LD F2, 8(R1)	int1	int	9	11	12	13	23
LD F1, 0(R1)	int3	int	10	12	13	14	24
MUL.D F4, F2, F0	mult3	md1	11	15-24		25	26

Tomasulo's Algorithm

The pipeline functional units are described by the following table

FU Type	Cycles in Ex	# of Ex Units	# of Reservation Stations
Integer	1	1	4
FP Add/Sub	4	1	4
FP Mult/Div	10	2	4

Assume 2 inst of any type can commit/cycle
Assume 2 CDB

Multiple Issue & No Speculation

Instruction	Reservation Station	Exec FU	Issue	Exec begin-end	Mem Access	CDB write
LD F2, 0(R1)	int1	int	1	2	3	4
MUL.D F4, F2, F0						
LD F4, 4(R1)						
SD F4 8(R1)						
MUL.D F6, F4, F1						
ADD.D F6, F4, F2						
DSUBUI R1, R1, #8						
BEQZ R1, **L1**						
LD F2, 8(R1)						
LD F1, 0(R1)						
MUL.D F4, F2, F0						

Multiple Issue & No Speculation

Instruction	Reservation Station	Exec FU	Issue	Exec begin-end	Mem Access	CDB write
LD F2, 0(R1)	int1	int	1	2	3	4
MUL.D F4, F2, F0	mult1	md1	1	5-14		15
LD F4, 4(R1)	int2	int	2	3	4	5
SD F4 8(R1)	int3	int	2	4	6	
MUL.D F6, F4, F1	mult2	md2	3	6-15		16
ADD.D F6, F4, F2	add1	as1	3	6-9		10
DSUBUI R1, R1, #8	int4	int	4	5		6
BEQZ R1, **L1**	int1	int	5	7		
LD F2, 8(R1)	int2	Int	6	8	9	10
LD F1, 0(R1)	int4	Int	6	9	10	11
MUL.D F4, F2, F0	mult3	md1	7	15-24		25

Multiple Issue With Speculation

Instruction	Reservation Station	Exec FU	Issue	Exec begin-end	Mem Access	CDB write	Commit/ Mem Wrt
LD F2, 0(R1)	int1	int	1	2	3	4	5
MUL.D F4, F2, F0							
LD F4, 4(R1)							
SD F4 8(R1)							
MUL.D F6, F4, F1							
ADD.D F6, F4, F2							
DSUBUI R1, R1, #8							
BEQZ R1, **L1**							
LD F2, 8(R1)							
LD F1, 0(R1)							
MUL.D F4, F2, F0							

Multiple Issue With Speculation

Instruction	Reservation Station	Exec FU	Issue	Exec begin-end	Mem Access	CDB write	Commit/ Mem Wrt
LD F2, 0(R1)	int1	int	1	2	3	4	5
MUL.D F4, F2, F0	mult1	md1	1	5-14		15	16
LD F4, 4(R1)	int2	int	2	3	4	5	16
SD F4 8(R1)	int3	int	2	4	6		17
MUL.D F6, F4, F1	mult2	md2	3	6-15		16	17
ADD.D F6, F4, F2	add1	as1	3	6-9		10	18
DSUBUI R1, R1, #8	int4	int	4	5		6	18
BEQZ R1, **L1**	int1	int	4	7			19
LD F2, 8(R1)	int2	int	5	8	9	10	19
LD F1, 0(R1)	int3	int	5	9	10	11	20
MUL.D F4, F2, F0	mult3	md1	6	15-24		25	26