CS3853: Computer Architecture
Midterm 1
Fall 2014
Total Marks: 36
Time: 50 min

Name:
Banner Id:
Alias:

1. [10 pt] Indicate **True** or **False** for the following statements:

   - If system A is n% faster that system B, then $ET_A/ET_B = n/100$.
   - If 20% of a program cannot be parallelized, then the maximum speed up that can be achieved through parallelization is 5.
   - The higher the value of CPI, the worse it is.
   - If a pipeline allows some earlier instructions before an exception causing instruction to commit before the exception is handled, then the pipeline does not support precise exception.
   - Throughput is not a measure of performance.
   - Structural hazard cannot be eliminated by duplicating various resources.
   - A delayed branch always executes instructions in the delay slots.
   - In the 5 stage MIPS pipeline, a load followed by a dependent ALU instruction causes 2 cycle stall.
   - Hazards are detected in the EX stage.
   - Pipeline interlock is in charge of hazard detection.

2. [8 pt] Amdahl's law:

   Suppose you can apply two enhancements - enh_1 and enh_2. enh_1 can be applied to 40% of the program of which 60% can be further improved by enh_2. The speed ups of enh_1 and enh_2 are 3 and 2 respectively.

   (a) [2 pt] What is the overall speed up if you use only enh_1?

   (b) [2 pt] What is the overall speed up if you use both enhancements together?

3. [18 pt] Pipeline & CPI:

Let us consider a classic 5 stage MIPS pipeline where the **branch is resolved in ID stage**. Consider the following code fragment:

```
L1: LD R1, 0(R10)
LD R2, 4(R1)
ADD R2, R2, R3
ADD R3, R1, R2
BEQZ R3, L1
SD R3, 0(R10)
```

(a) [6 pt] Assume that the pipeline has no forwarding support and branches are handled using static *freeze* strategy. Show the pipeline timing diagram of the same code.

Ins	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
L1: LD R1, 0(R10)																					
LD R2, 4(R1)																					
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ADD R3, R1, R2																					
BEQZ R3, L1																					
SD R3, 0(R2)																					

(b) [6 pt] Assume that the pipeline has full forwarding support and branches are handled using static *predict not taken* strategy. Show the pipeline timing diagram of the same code.

Ins	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
L1: LD R1, 0(R10)																					
LD R2, 4(R1)																					
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ADD R3, R1, R2																					
BEQZ R3, L1																					
SD R3, 0(R2)																					

(c) [6 pt] Assume our 5 stage MIPS pipeline with full forwarding. Lets assume that branch condition is evaluated in ID stage and target is calculated in EX stage. Assume that 10% loads have a dependence with the immediately following ALU instruction and 5% loads have a dependence with the immediately following branch instruction. Assume there are no other load dependencies.

i. What is the average number of stalls for a load instruction?

ii. What is the CPI of a load instruction?