



Lab 01

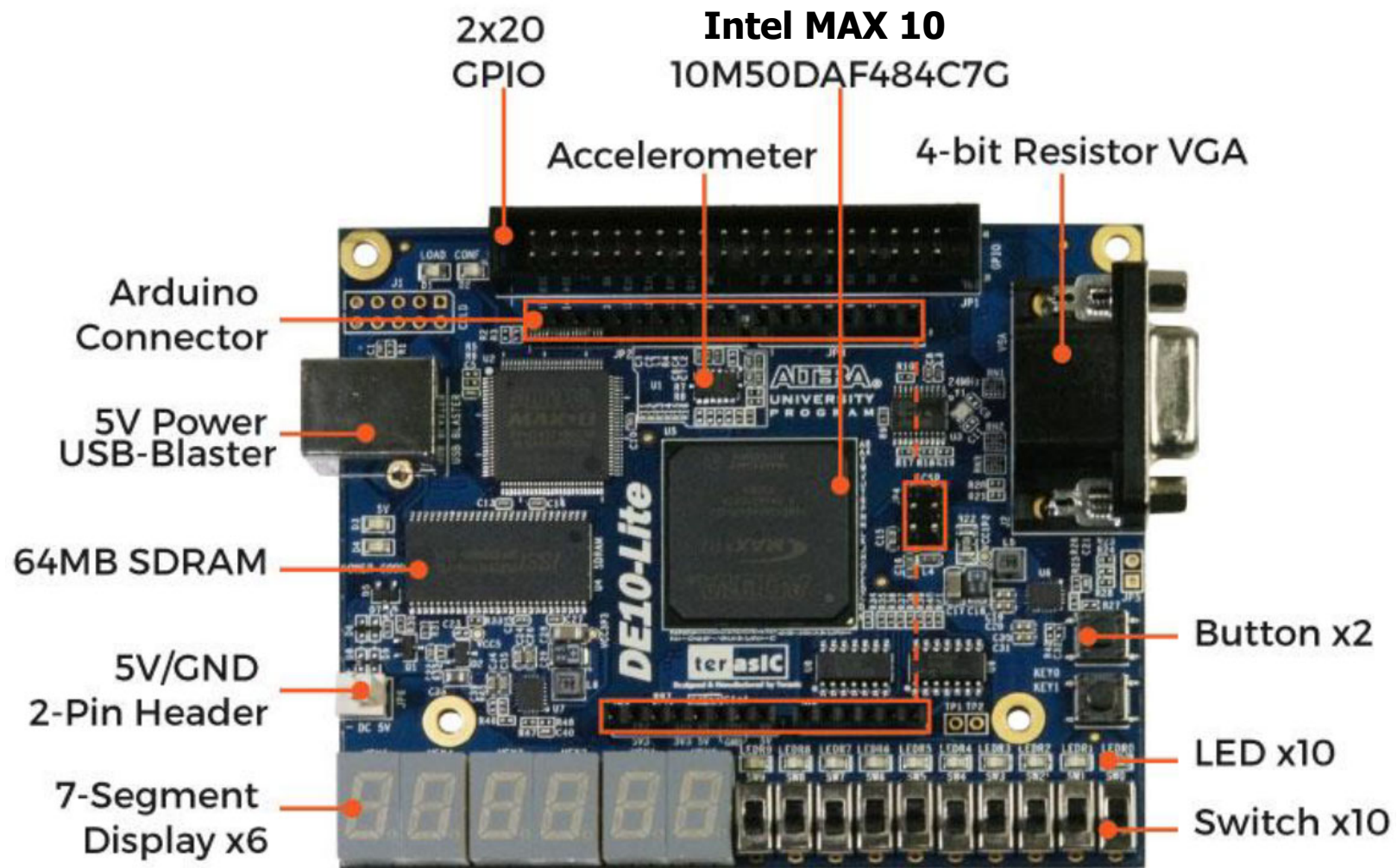
Introduction

Ren-Der Chen (陳仁德)
Department of Computer Science and
Information Engineering
National Changhua University of Education
E-mail: rdchen@cc.ncue.edu.tw
Spring, 2024

Course Contents

- Hardware Description Language (HDL)
 - Verilog
- Design platform
 - DE10-Lite Development Board
 - JQH-EDU-006-V1數位邏輯教學置具
- Design tool
 - Intel Quartus Prime (20.1 Light Edition)

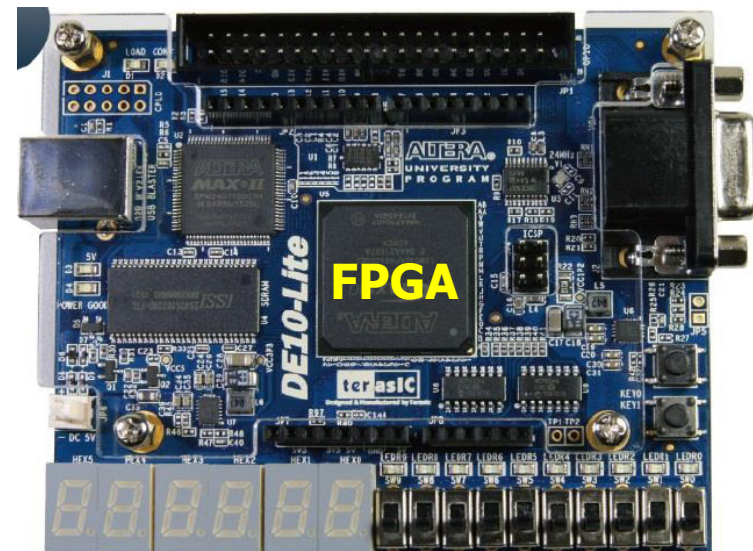
DE10-Lite Development Board



Hardware on the Board (1/3)

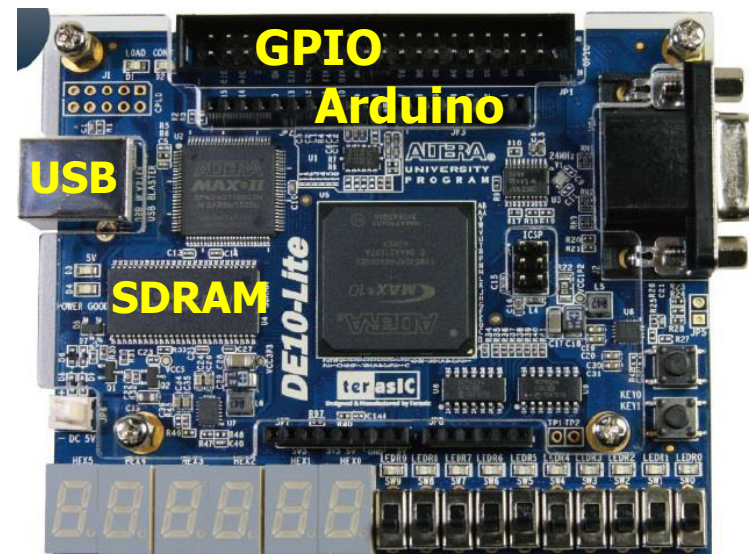
■ FPGA Device

- MAX 10 10M50DAF484C7G Device
- Integrated dual ADCs, each ADC supports 1 dedicated analog input and 8 dual function pins
- 50K programmable logic elements
- 1,638 Kbits M9K Memory
- 5,888 Kbits user flash memory
- 144 18×18 Multiplier
- 4 PLLs



Hardware on the Board (2/3)

- Programming and Configuration
 - On-Board USB Blaster (Normal type B USB connector)
- Memory Device
 - 64MB SDRAM, x16 bits data bus
- Connectors
 - 2x20 GPIO Header
 - Arduino Uno R3 Connector, including six ADC channels.



Hardware on the Board (3/3)

■ Display

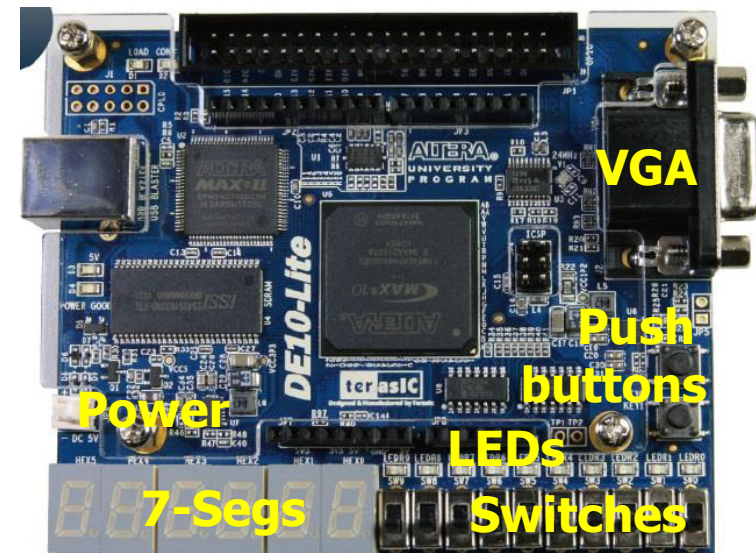
- 4-bit resistor-network DAC for VGA (With 15-pin high-density D-sub connector)

■ Switches, Buttons and LEDs

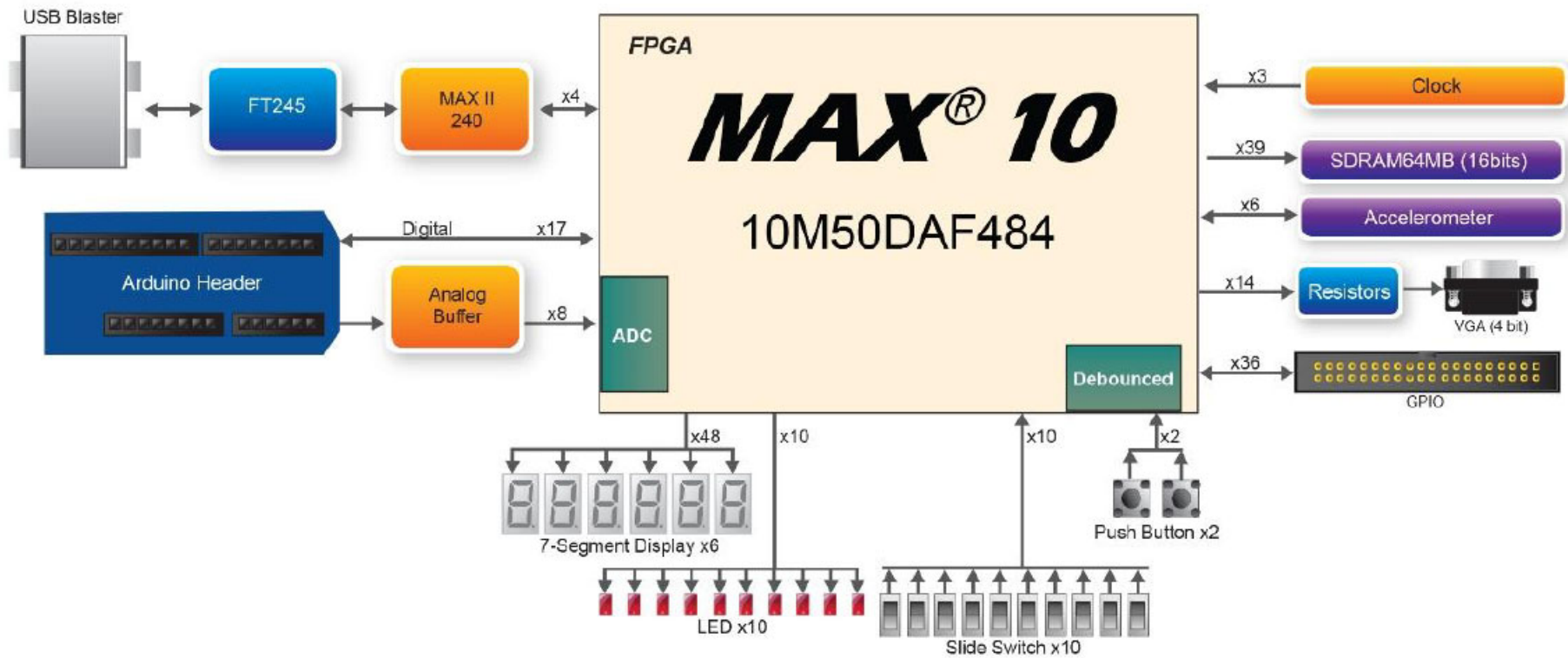
- 10 LEDs
- 10 Slide Switches
- 2 Push Buttons with Debounced.
- Six 7-Segments

■ Power

- 5V DC input from USB or external power connector.



Board Block Diagram



Intel MAX 10 Device Ordering Information

Member Code

02 : 2K logic elements
04 : 4K logic elements
08 : 8K logic elements
16 : 16K logic elements
25 : 25K logic elements
40 : 40K logic elements
50 : 50K logic elements

Package Type

V : Wafer-Level Chip Scale (WLCSP)
E : Plastic Enhanced Quad Flat Pack (EQFP)
M : Micro FineLine BGA (MBGA)
U : Ultra FineLine BGA (UBGA)
F : FineLine BGA (FBGA)

Operating Temperature

C : Commercial ($T_J = 0^\circ\text{C}$ to 85°C)
I : Industrial ($T_J = -40^\circ\text{C}$ to 100°C)
A : Automotive ($T_J = -40^\circ\text{C}$ to 125°C)

Family Signature · **10M-50-DA-F-484-C-7-G**

10M : Intel® MAX® 10

Feature Options

SC : Single supply - compact features
SA : Single supply - analog and flash features with RSU option
DC : Dual supply - compact features
DF : Dual supply - flash features with RSU option
DA : Dual supply - analog and flash features with RSU option

FPGA Fabric Speed Grade

6 (fastest)
7
8

Optional Suffix

Indicates specific device options or shipment method

G : RoHS6
ES : Engineering sample
P : Leaded package

Package Code

WLCSP Package Type

36 : 36 pins, 3 mm x 3 mm
81 : 81 pins, 4 mm x 4 mm

EQFP Package Type

144 : 144 pins, 22 mm x 22 mm

MBGA Package Type

153 : 153 pins, 8 mm x 8 mm

UBGA Package Type

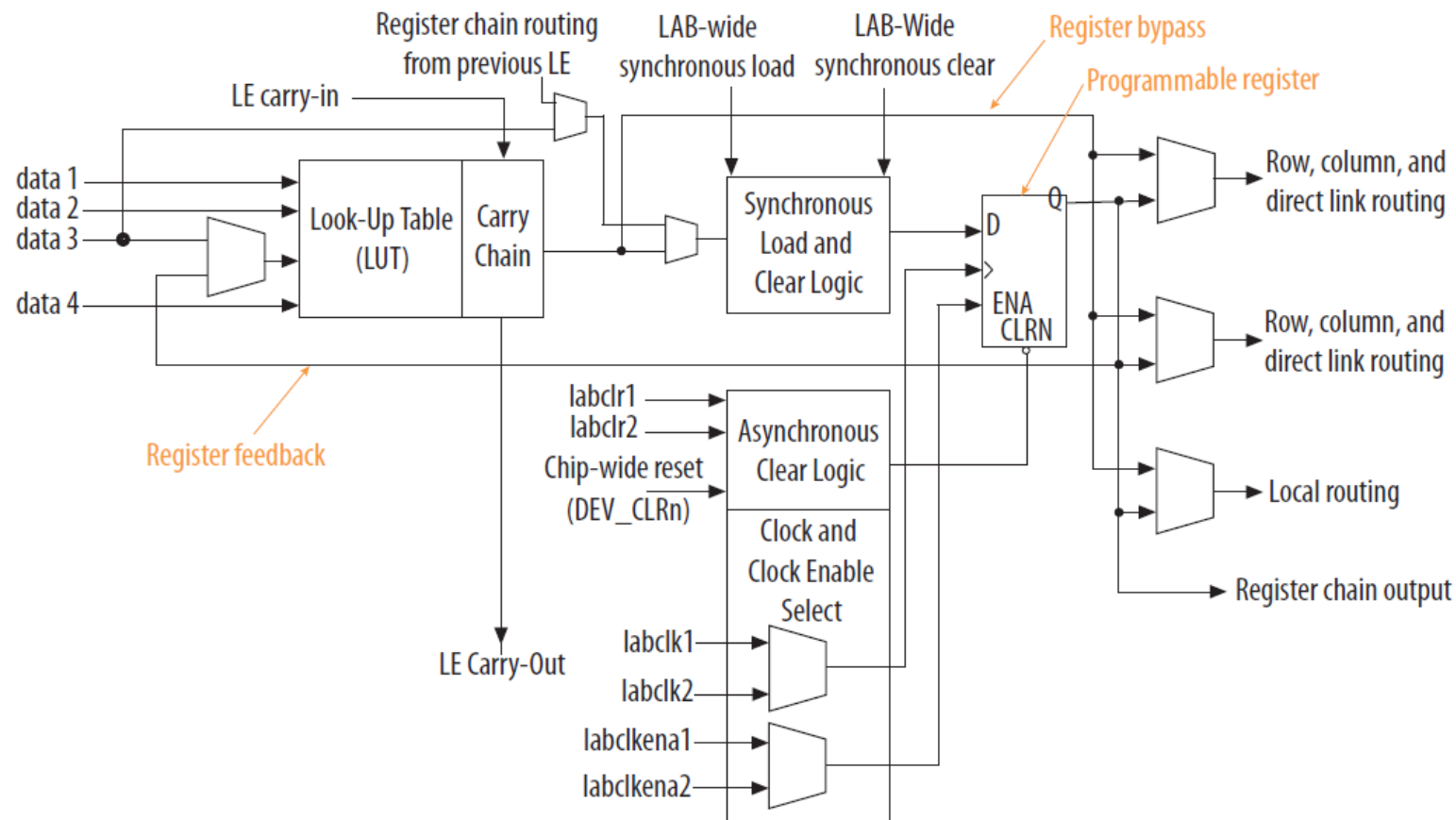
169 : 169 pins, 11 mm x 11 mm
324 : 324 pins, 15 mm x 15 mm

FBGA Package Type

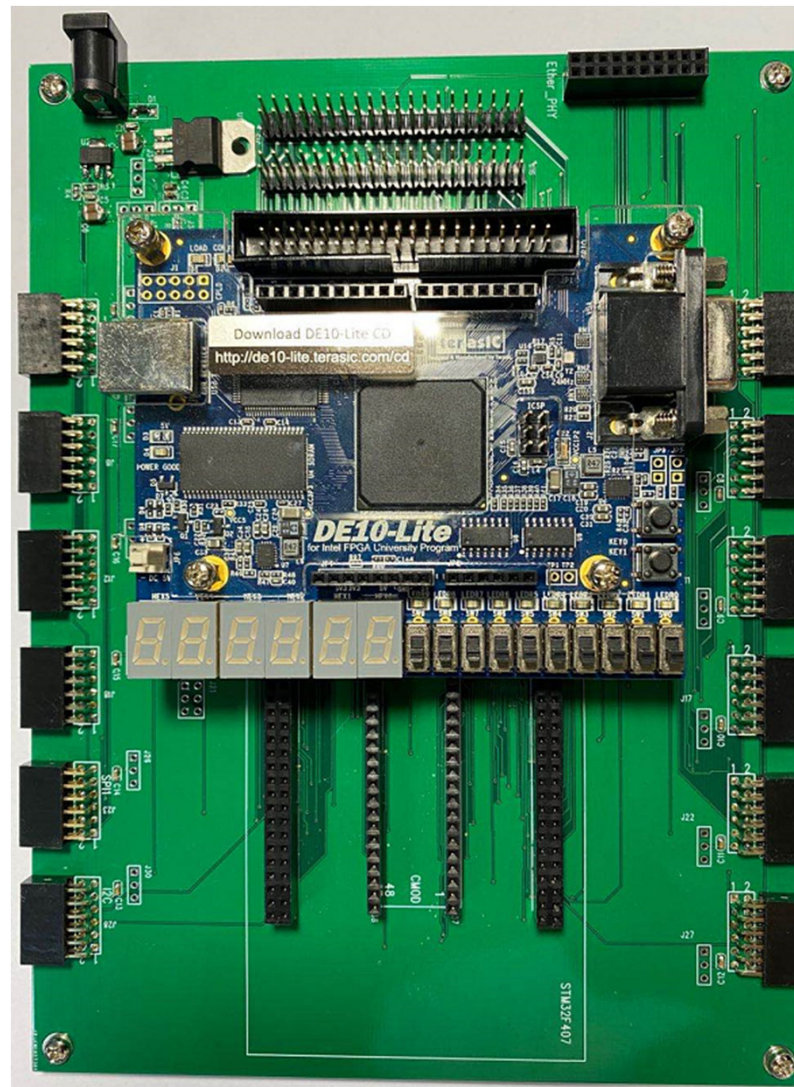
256 : 256 pins, 17 mm x 17 mm
484 : 484 pins, 23 mm x 23 mm
672 : 672 pins, 27 mm x 27 mm

Logic Elements (LEs)

- An LE is the smallest unit of logic in the Intel MAX 10 device architecture.



JQH-EDU-006-V1數位邏輯教學置具



實驗組件 (1/2)

MAX DE10 Lite 主系統板



系統開發搭接訊號轉接板



LCD 顯示轉接板



七段顯示器/8X8 DOTMATRIX 轉接板



LED 顯示數位位元控制板/Bits Switch



LED 顯示數位位元控制板/Push Button



鍵盤



CCD 顯示器轉接板



ADDA 訊號調節控制設定板



實驗組件 (2/2)

40pin 排線



USB 傳輸線



七段顯示器 4 個 8



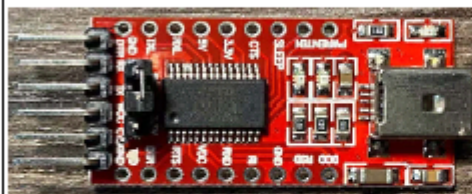
8X8 點陣列 LED



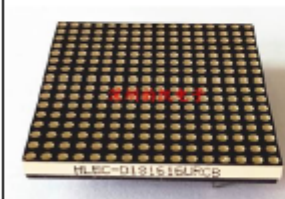
蜂鳴器



FTDI232



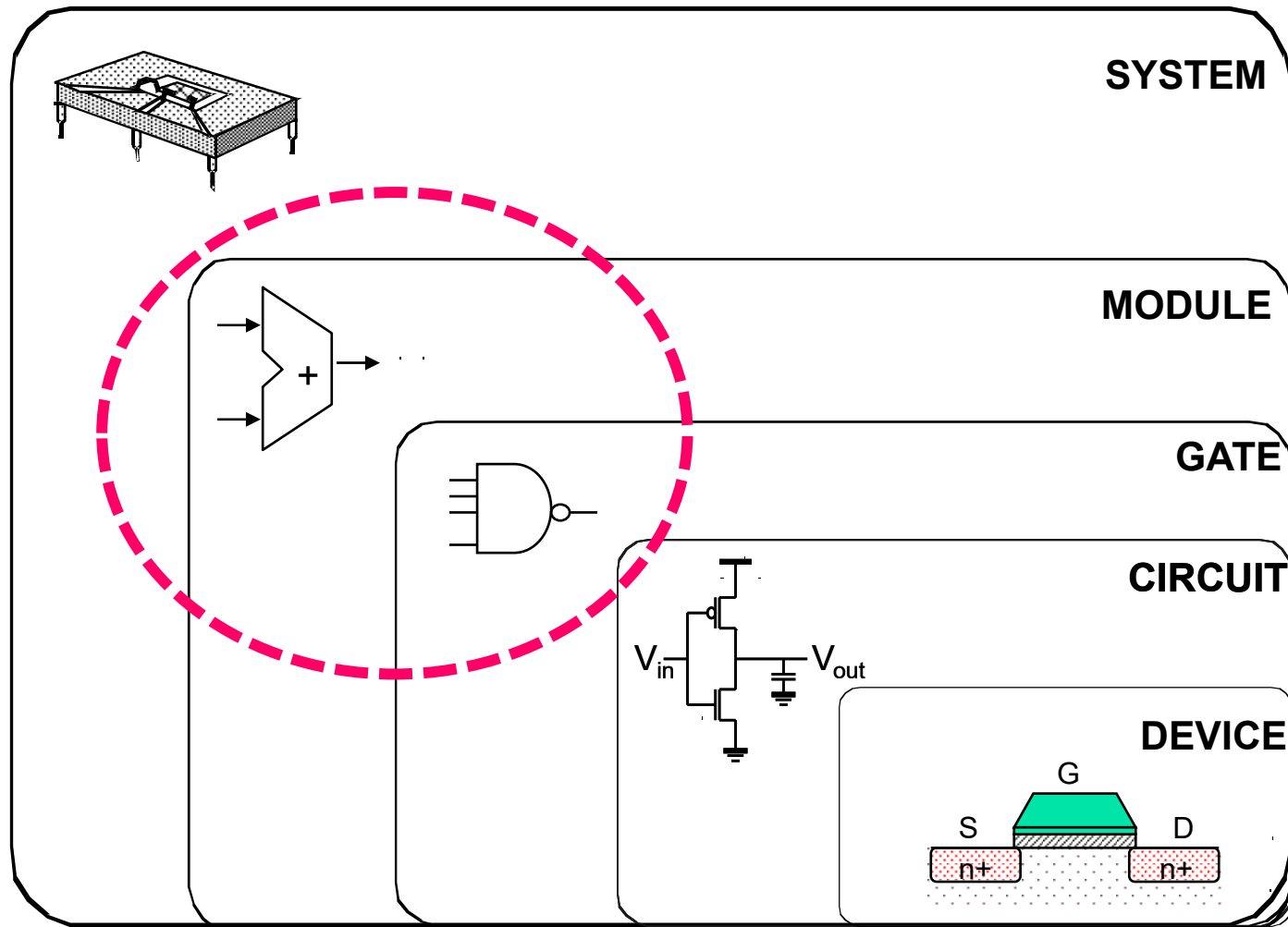
16X16 點陣列 LED



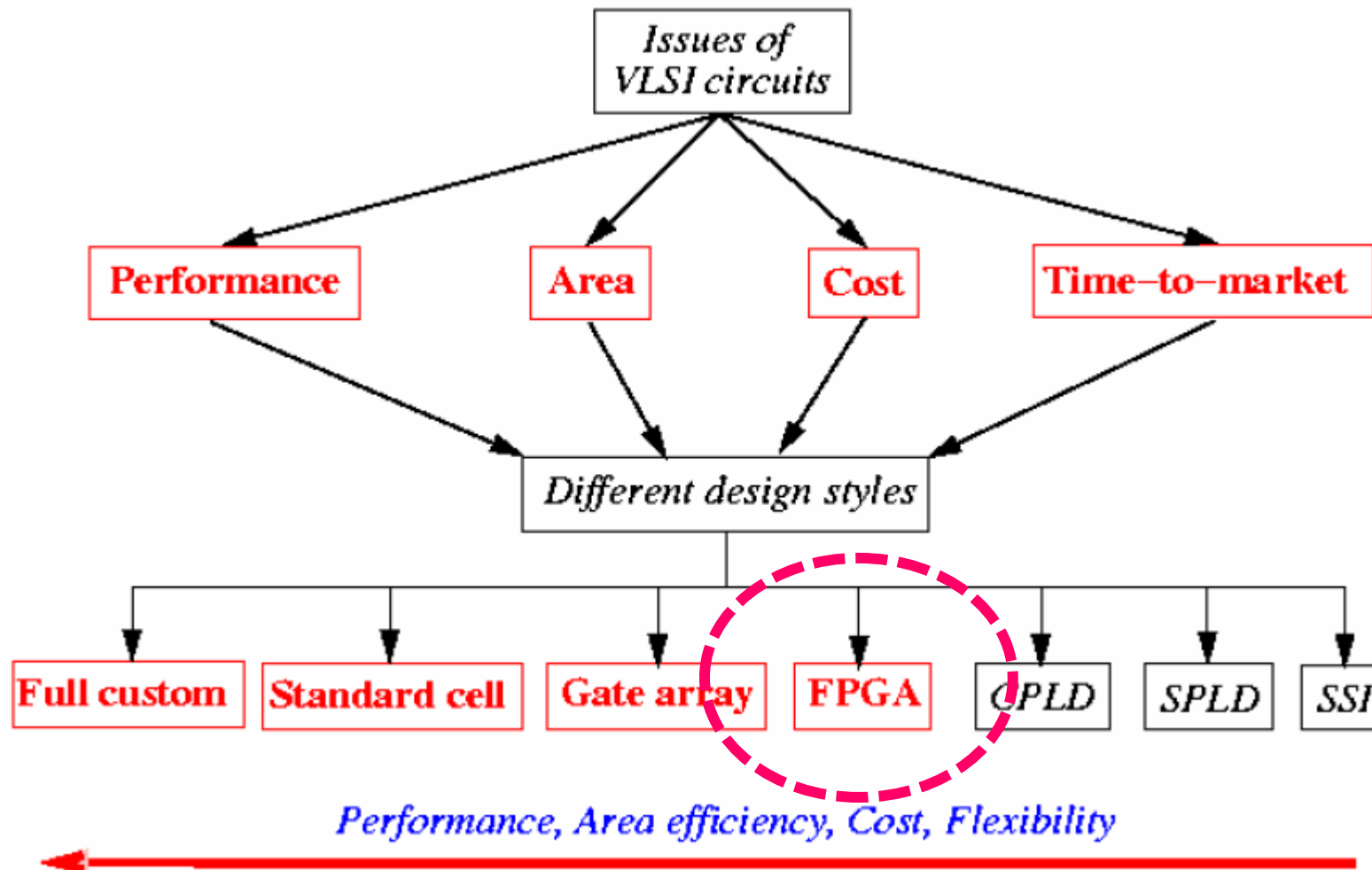
16X16 點陣列 LED 驅動控制板



IC Design Abstraction Levels



IC Design Considerations



Verilog Design - Structural Description of a Half Adder

```
module add_half_struct (a, b, sum, c_out);
```

```
    input          a, b;
```

```
    output         sum, c_out;
```

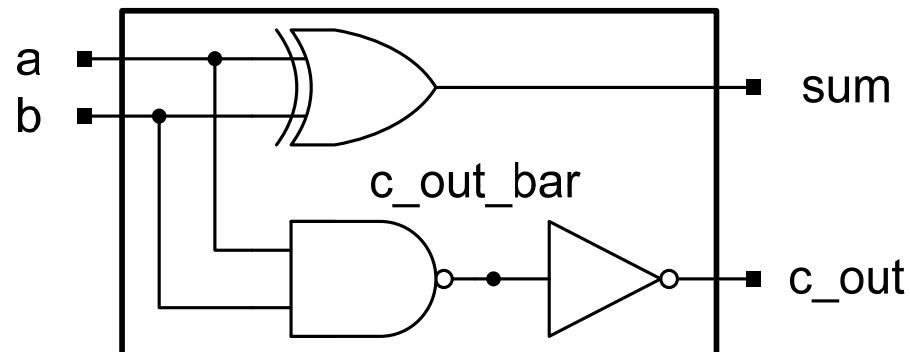
```
    wire          c_out_bar;
```

```
    xor            G1 (sum, a, b);
```

```
    nand           G2 (c_out_bar, a, b);
```

```
    not            G3 (c_out, c_out_bar);
```

```
endmodule
```



Verilog Design - Algorithmic Description of a 4-Input AND Gate

```
module and4_alg (x_in, y_out);
```

```
    input    [3:0] x_in;
```

```
    output    y_out;
```

```
    reg       y_out;
```

```
    integer    k;
```

```
    always @ (x_in) // x_in[3] or x_in[2] or x_in[1] or x_in[0]
```

```
    begin: and_loop
```

```
        y_out = 1;
```

```
        for (k=0; k <= 3; k = k+1)
```

```
            if (x_in[k] == 0)
```

```
                begin
```

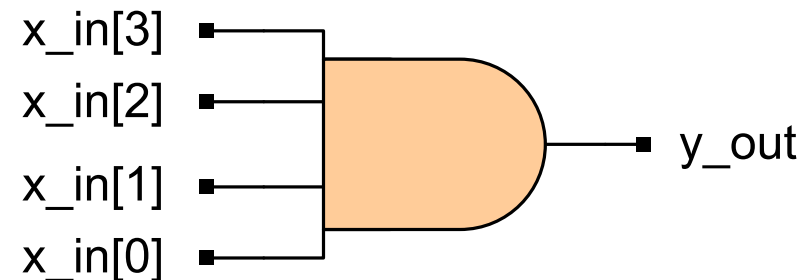
```
                    y_out = 0;
```

```
                    disable and_loop;
```

```
                end
```

```
    end
```

```
endmodule
```



Verilog Design - Algorithmic Description of a Comparator

```
module compare_alg (A, B, A_lt_B, A_gt_B, A_eq_B);  
  input    [1:0] A, B;  
  output    A_lt_B, A_gt_B, A_eq_B;  
  reg       A_lt_B, A_gt_B, A_eq_B;
```

```
  always @ (A or B)
```

```
  begin
```

```
    A_lt_B = 0; A_gt_B = 0; A_eq_B = 0;
```

```
    if (A == B)
```

```
      A_eq_B = 1;
```

```
    else if (A > B)
```

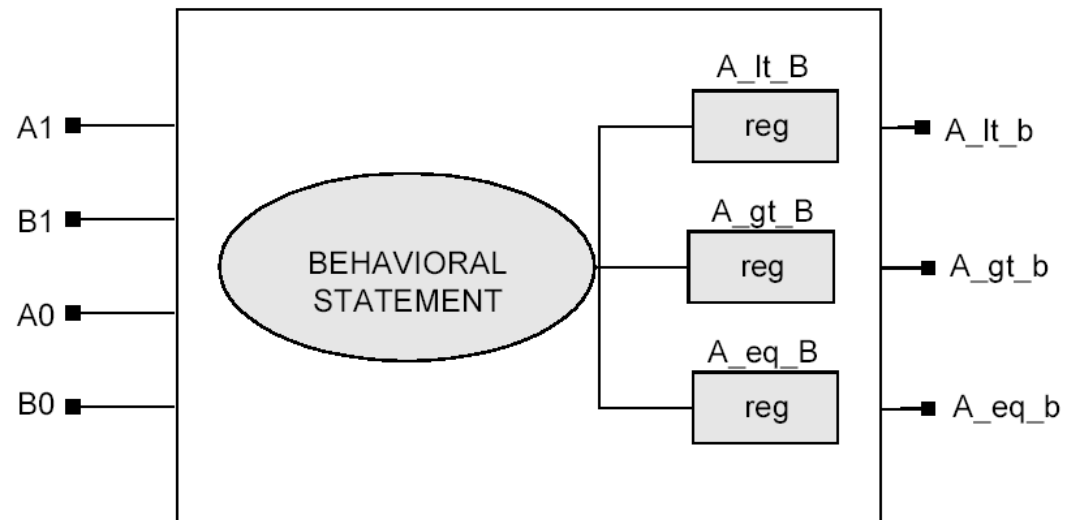
```
      A_gt_B = 1;
```

```
    else
```

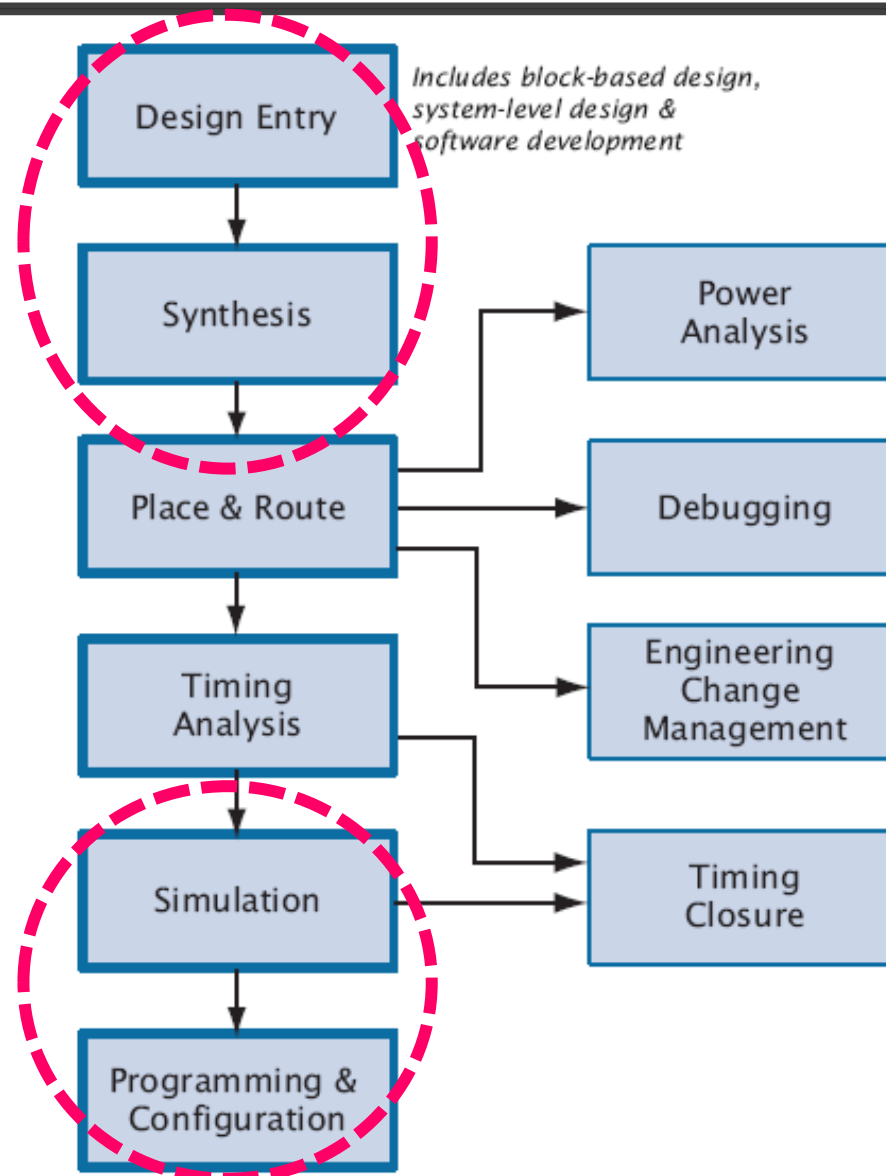
```
      A_lt_B = 1;
```

```
  end
```

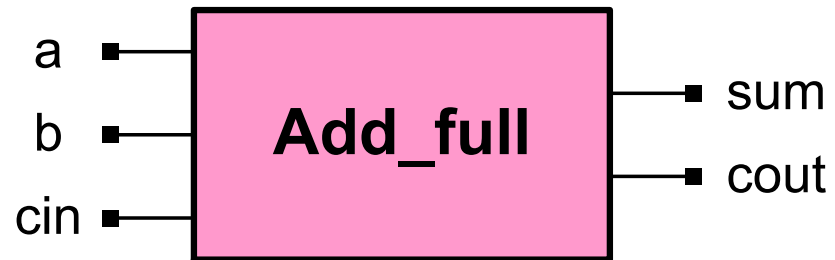
```
endmodule
```



FPGA Design Flow



Design Example: Full Adder



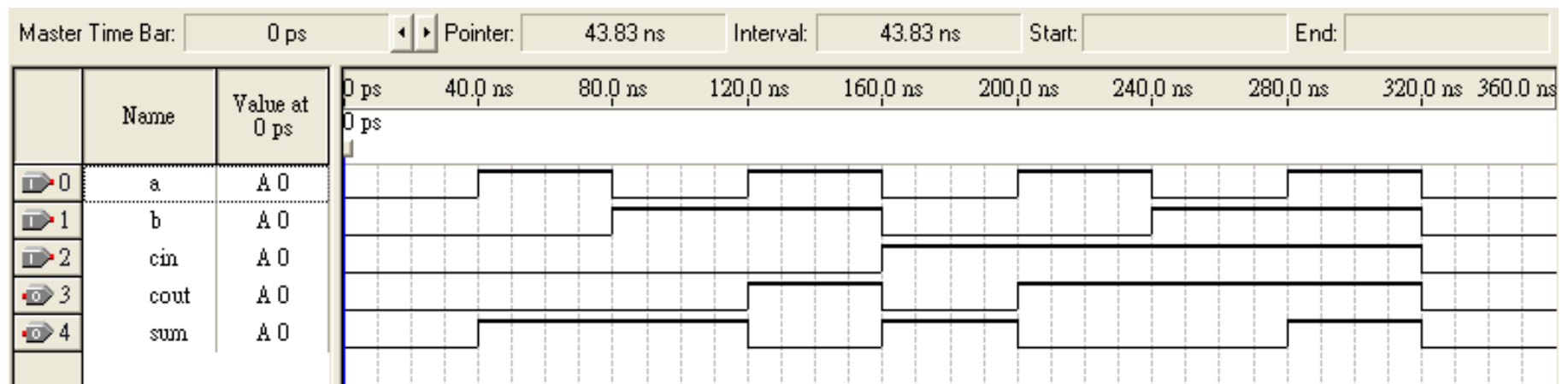
ab\cin	0	1
00	0	1
01	1	0
11	0	1
10	1	0

$$\text{sum} = (a \oplus b) \oplus \text{cin}$$

ab\cin	0	1
00	0	0
01	0	1
11	1	1
10	0	1

$$\text{cout} = a \cdot b + (a \oplus b) \cdot \text{cin}$$

Functional Simulation Result



Pin Assignments

Inputs



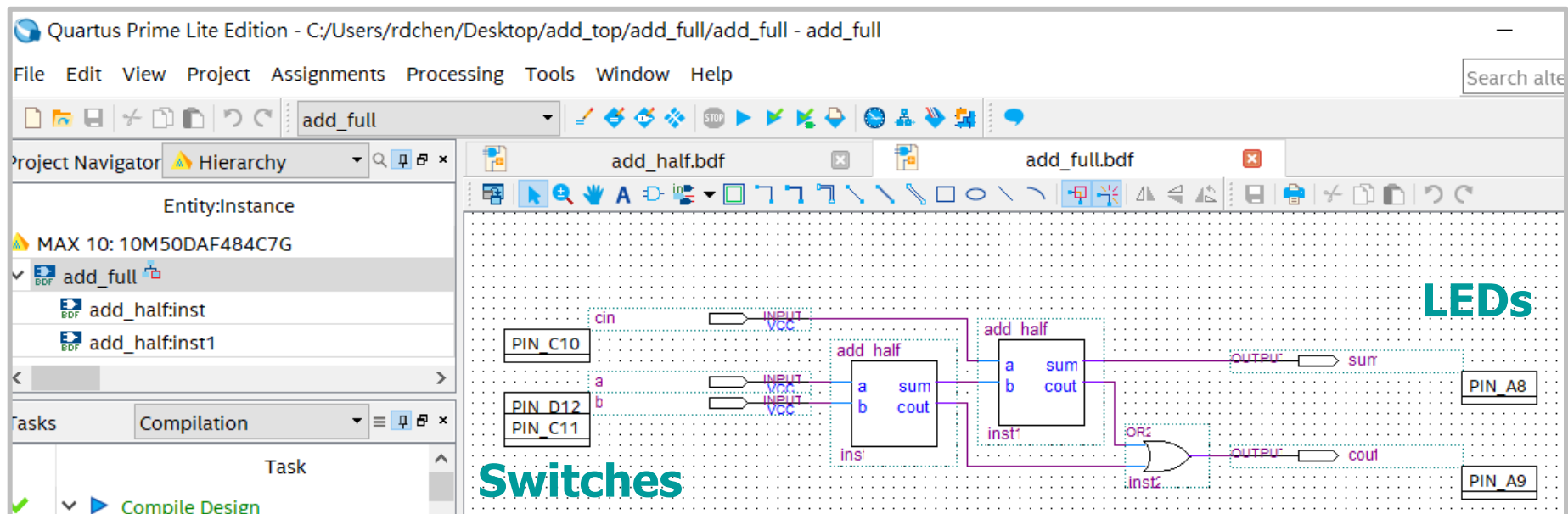
Outputs



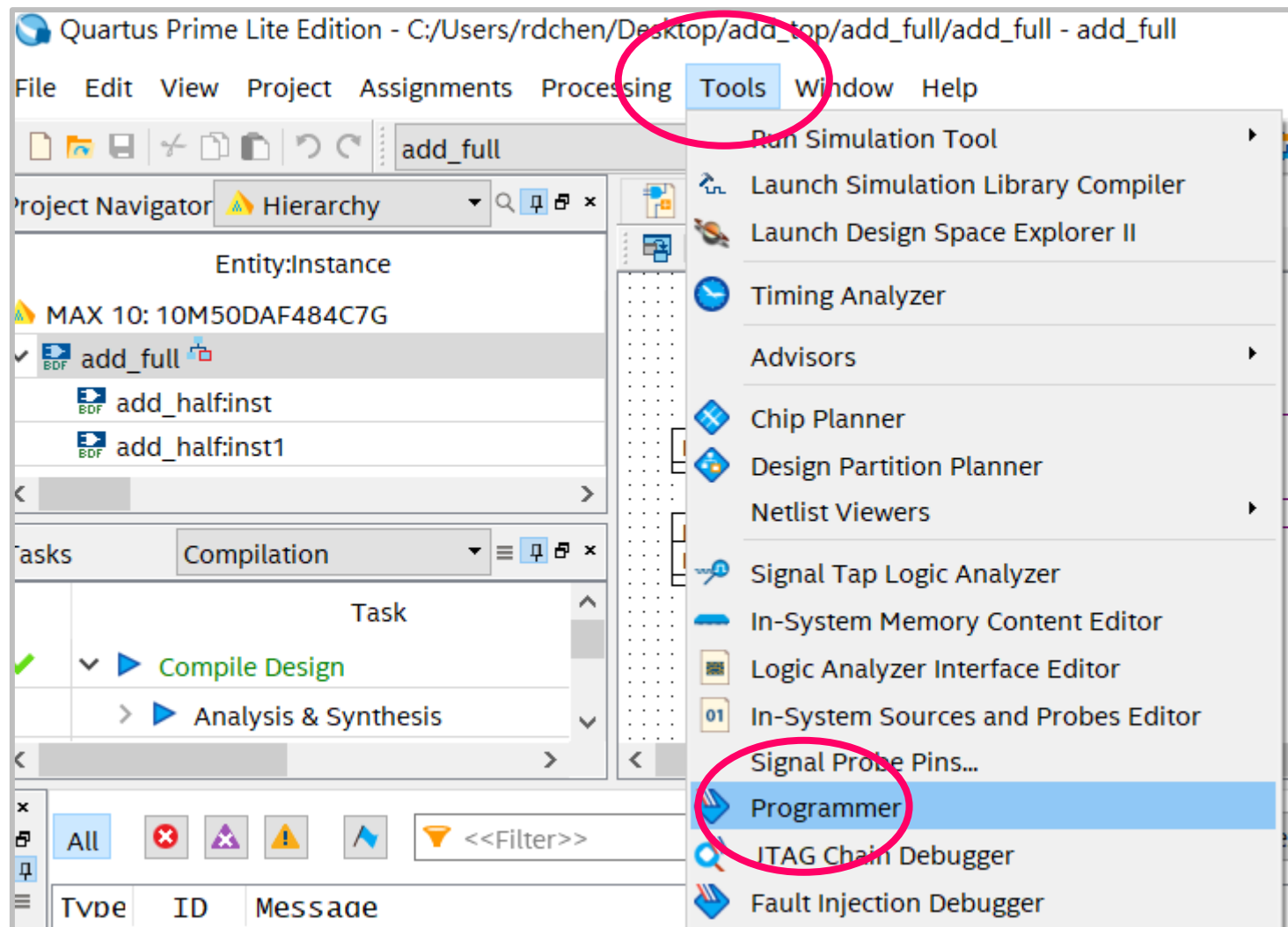
$$\{\text{cout, sum}\} = a + b + \text{cin}$$

Design Step 1

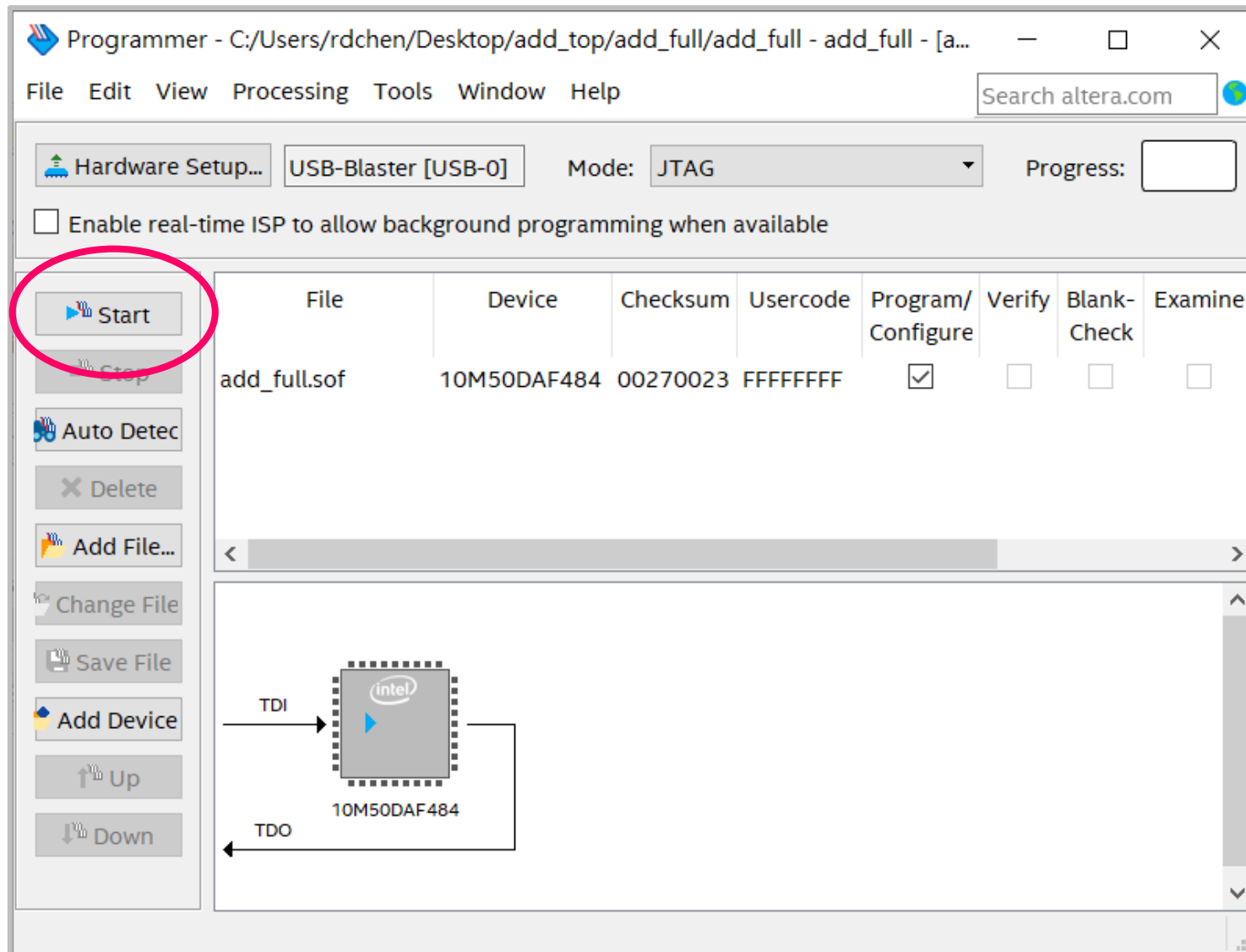
- Copy [add_top.zip](#) to hard disk and unzip it.
- Run [add_full.qpf](#) in [add_top\add_full](#)



Design Step 2



Design Step 3



Verify Your Design

- sw2/sw1/sw0 : dn/dn/dn (0/0/0) => L1/L0: off/off (0/0)
- sw2/sw1/sw0 : dn/dn/up (0/0/1) => L1/L0: off/on (0/1)
- sw2/sw1/sw0 : dn/up/dn (0/1/0) => L1/L0: off/on (0/1)
- sw2/sw1/sw0 : **dn/up/up (0/1/1)** => L1/L0: **on/off (1/0)**
- sw2/sw1/sw0 : up/dn/dn (1/0/0) => L1/L0: off/on (0/1)
- sw2/sw1/sw0 : up/dn/up (1/0/1) => L1/L0: on/off (1/0)
- sw2/sw1/sw0 : up/up/dn (1/1/0) => L1/L0: on/off (1/0)
- sw2/sw1/sw0 : **up/up/up (1/1/1)** => L1/L0: **on/on (1/1)**



成績評量

■ 評分

- 期中考: 30%
- 期末考: 30%
- 課堂參與&書面報告: 40%

- 本課程期中、期末考試，完成時間亦為評分項目之一。全體同學依比序給分。**1. 答題分數越高，比序越前面；2. 答題分數相同，較快完成者比序在前面。**