JISHNU JANARDANAN

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EDUCATION

B.S. in Computer Engineering | Illinois Institute of Technology | Chicago, IL | Graduated: Dec 2025

Coursework: Data Structures & Algorithms, Machine Learning, Object-Oriented Programming, Computer Organization and design, Probability & Statistics, Operating Systems, Systems Programming, Circuit Analysis, Digital Systems, Signals and Systems, Engineering Electronics

PUBLICATIONS

ThinkFast: A Versatile Trivia System for Education, Collaboration, and Communication

Submitted to 2026 IEEE International Conference on Electro/Information Technology (EIT 2026) | Paper ID: 121

WORK EXPERIENCE

Backend Developer Intern (Remote) | FoodCLUB | United Kingdom (Remote) | Jan 2024 – May 2024

- Developed Node.js backend services on AWS EC2, maintaining 99% uptime for user authentication and data retrieval APIs
- Optimized REST API performance by implementing Redis caching, reducing response latency by 30% across core user-facing endpoints
- Debugged and resolved backend issues through systematic code reviews, improving overall API stability and reducing production incidents
- Wrote technical documentation for REST API endpoints, standardizing request/response formats and error handling for frontend integration

SKILLS

- **Programming Languages:** Python, JavaScript, TypeScript, Java, C, C++, SQL, Bash, VHDL, Verilog, HTML/CSS
- **Frameworks & Libraries:** React, Node.js, OpenMP, Kafka, RabbitMQ, GraphQL
- **Databases(SQL & NoSQL)**: PostgreSQL, MySQL, DynamoDB, Redis, Firebase
- **EDA & VLSI Tools:** Synopsys Design Compiler, Cadence SOC Encounter, ModelSim, VLSI CAD Flows (RTL to GDSII)
- **Cloud Computing & Infrastructure:** AWS(Lambda, EC2, API gateway, S3, RDS, CloudFront), Docker, Git (version control), CI/CD, Linux/Ubuntu
- **Concepts:** System Design, Microservices, Distributed Systems, TCP/IP, RESTAPIs, Object-Oriented Programming, Data Structures and Algorithms, Unit Testing, Multi-threaded Programming, Agile, Load Balancing, Caching Strategies, Database Sharding & Replication, CAP Theorem, Message Queues, Fault Tolerance, Rate limiting

TECHNICAL PROJECTS

SneakersForLess - Sneaker Price Comparison Website | React, AWS Lambda, DynamoDB, Firebase |Personal Project | Nov 2025 | sneakersforless.org

- Built the React frontend with Firebase Authentication for OAuth login, deployed on S3 and CloudFront with 99.9% availability
- Set up a serverless backend with Lambda, API Gateway, and DynamoDB that auto-scales and responds in under 100ms
- Implemented CI/CD pipeline using GitHub Actions, reducing deployment time by 80% with automated testing and builds

Old Is Gold - Senior Fitness Platform | React, AWS Lambda, DynamoDB, CloudFront |Personal Project | Jan 2026 oldisgold. fit

- Built a full-stack fitness app for seniors with personalized workouts, nutrition tracking (50+ foods), and progress analytics
- Engineered a serverless backend using Lambda +API Gateway with auto-scaling architecture and consistent sub-200ms response times
- Deployed globally via CloudFront CDN across 200+ edge locations for high availability and low-latency access
- Configured CI/CD with GitHub Actions, cutting deployment time from 15 minutes to 30 seconds with zero-downtime releases

Think Fast! – Embedded Trivia Game | Python, Raspberry Pi, Arduino, Serial | Team Project (4 members) | Illinois Institute of Technology | Spring 2025

- Developed a hardware-integrated trivia game using Python and Raspberry Pi, implementing physical button inputs and real-time game state management
- Designed context-aware input handling system with dynamic button mapping that switches functionality based on game state (menu navigation vs. answer selection)
- Integrated Arduino microcontroller with Raspberry Pi via UART Serial communication to trigger LED feedback with sub-100ms response times
- Optimized input reliability by implementing software debouncing algorithms, eliminating false triggers and synchronizing audio playback with hardware events

Chicago Transit Authority (CTA) Database System | Python, SQL, MySQL, PostgreSQL | Illinois Institute of Technology | Summer 2024

- Architected a relational database with 6-8 entities, enforcing referential integrity constraints and business rules to ensure data consistency across transit operations
- Configured indexes, views, stored procedures, and triggers to optimize query performance and maintain data reliability under concurrent access
- Authored complex SQL queries using advanced window functions and OLAP analytics to support scalable reporting across diverse business scenarios
- Delivered a Python CRUD application with an intuitive UI, enabling reliable data operations with complex query support

Neural Network Inference Engine | C++, MNIST | Illinois Institute of Technology | Fall 2024

- Refactored 300 lines of C++ using OpenMP parallelization to eliminate performance bottlenecks in the inference engine's core computational layers
- Switched to NCHW/NHWC tensor layouts, which improved cache hit rate by 8% and saved 7ms off each inference
- Executed MLP and CNN models end-to-end with pre-trained weights, achieving 97.5% classification accuracy on MNIST

Matrix and Tensor Operations for EasyNN | C++, Python | Illinois Institute of Technology | Fall 2024

- Programmed a matrix and tensor operations in C++ for the EasyNN framework, including scalar/tensor input handling, matrix multiplication, and consistent numerical accuracy
- Validated C++ implementation using automated grading scripts, ensuring reliability and compliance with 10 functional requirements

32-bit Pipelines CPU with Enhanced ALU Architecture | VHDL, Verilog, Synopsys DC, Cadence SOC Encounter | Illinois Institute of Technology | Fall 2024

- Engineered a 32-bit custom RISC processor based on MIPS ISA with VHDL, supporting R-, I-, and J-format instructions with reliable instruction execution
- Constructed a modular 32-bit ALU from 1-bit cells with custom instructions (NAND, ORI), extending ISA functionality while maintaining consistent data flow across the data path
- Orchestrated pipeline synchronization for concurrent instruction execution; synthesized using Synopsys Design Compiler and compared adder architectures (Carry Ripple, Lookahead, Skip, Select), optimizing delay, area, and power
- Validated system reliability through RTL-to-GDSII VLSI CAD flow—RTL, post-synthesis, and post-layout simulations using ModelSim and Verilog with custom testbenches with physical design in Cadence SOC Encounter

INVOLVEMENT

IIT Motorsports (FSAE) | Jan 2024 – May 2024

- Researched hardware architecture for a quad inverter system powering a Formula SAE electric race car
- Conducted technical analysis for power switch selection using decision matrices and documented findings in the team design report