EE1 Project 2020 – Circuit Simulator File Format

Your circuit simulator should read an input file that defines the circuit and the simulation. The format of the input file is compatible with SPICE, but you only need to support a subset of the features of SPICE, which are described in this document.

Components

The netlist is described by lines defining the type, designator (name), nodes and value of each component

Designator letter	Component	Node order	Value
V	Voltage source	+, -	Volts or function
I	Current source	In, out	Amps or function
R	Resistor	N/A	Ohms
C	Capacitor	N/A	Farads
L	Inductor	N/A	Henries
D	Diode	Anode, Cathode	Model name
Q	Transistor	Collector, Base, Emitter	Model name

The format of each line is:

```
<designator> <node0> <node1> [<node 2] <value>
```

Designator

The designator field contains a letter and a number. The letter specifies the type of component (see table above) and the number is added to make a unique identifier for each component

Node list

A list of two or three node names occurs after the designator. Node names have the format `N123`. The component is connected to these nodes, in the order given in the table above. The reference (ground) node is named `0`

Value

The value is the component value in the units given in the table above. Numbers can be followed by a multiplier:

Multiplier	Value
p	$\times 10^{-12}$
n	$\times 10^{-9}$
u	$\times 10^{-6}$
m	$\times 10^{-3}$
k	$\times 10^{3}$
Meg	$\times 10^{6}$
G	$\times 10^{9}$

Voltage and current sources can have a DC value, or a function. The only function required is a sinusoid written in the form:

```
SINE(<dc offset> <amplitude> <frequency>)
```

DC offset and amplitude have units of Volts or Amps. Frequency has units of Hertz.

Diodes and transistors are given a model name instead of a value. If you support them, the following models should be defined internally in your software:

Model name	Type
D	Silicon diode
NPN	NPN BJT
PNP	PNP BJT

Simulation settings

The transient simulation is described with a line of the form:

```
.tran 0 <stop time> 0 <timestep>
```

Stop time is the duration of the simulation. Timestep is the resolution of the simulation. `0` fields are included to maintain compatibility with SPICE and do not need to be interpreted.

End of file

The file ends with the line:

```
.end
```

Comments

The input file may contain comments on lines beginning with *

These lines should be ignored.

Extensions to the specification

You can extend the file format if necessary to support any additional features you have added. Maintain compatibility with SPICE if possible.

Example

```
* A test circuit to demonstrate SPICE syntax
V1 N003 0 SINE(2 1 1000)
R1 N001 N003 1k
C1 N001 0 1µ
I1 0 N004 0.1
D1 N004 N002 D
L1 N002 N001 1m
R2 N002 N001 1Meg
Q1 N003 N001 0 NPN
.tran 0 10ms 0 1us
.end
```

You can generate your own examples by drawing a circuit in the LTspice software and choosing the option View → SPICE Netlist. LTspice includes some additional lines which aren't required for your simulator. You may wish to configure your simulator to ignore these lines so you can produce test circuits directly from LTspice.