Parasitic Inductance Modeling and Reduction for a Wire Bonded Half Bridge SiC MOSFET Multichip Power Module

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***Abstract* — The parasitic inductance in the current commutation loop (CCL) could cause current and voltage oscillations during switching transient, increase switching loss, EMI and voltage stress on power semiconductor devices. These undesirable features intensify with the use of Wide Bandgap (WBG) devices due to increased switching speed and lower on-resistance. In this paper, the parasitic inductance of the current commutation loop is modeled with Partial Element Equivalent Circuit (PEEC) method for SiC multichip module. Different from other studies, the mutual inductance between paralleled branches are thoroughly analyzed and included in the model. As shown in Finite Element Analysis (FEA) simulation and experiment measurement, the mutual inductance has significant influence on the accuracy of the model. A wire bonded package layout is then proposed for SiC multichip half bridge modules that could reduce parasitic inductance without increasing fabrication difficulty. The effectiveness of the developed structure is verified with 3D FEA simulation and experiment.**

Keywords—Package design, Silicon carbide (SiC), Multichip power module layout, Electromagnetic interference, Finite Element Analysis, 3D modeling

I. INTRODUCTION

With the development of power electronics, the continuing demand of higher efficiency and higher power density design is pushing the performance of power semiconductors to the limit of Si material. At the same time, Wide Bandgap semiconductor materials including SiC and GaN, have presented multiple advantages over Si materials. For the first time, it is possible to reduce conduction loss and switching loss at the same time. However, with the increasing of switching speed operating frequency, the impact of parasitic elements of module package becomes higher. For instance, the direct bond copper (DBC) and wire bonded package structure is the most widely used for multichip power module because of manufacturing maturity, low cost and good thermal performance. But the use of bond wires and 2D layout result in large parasitic inductance in the current commutation loop (CCL), as shown in Fig.1.

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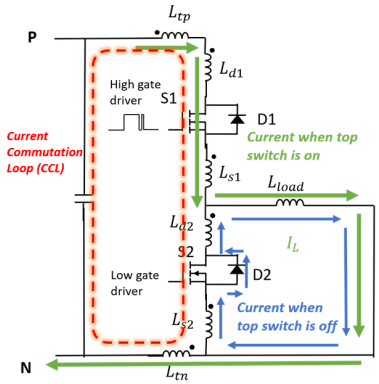


Fig.1 Illustration of the current commutation loop of a half bridge under double pulse tester set up

The double pulse tester circuit in Fig.1 is widely used for evaluating device switching performance. During the switching transition of the top switch, high di/dt will occur between the top switch S1 and bottom diode D2 (bottom switch S2 is kept off during double pulse testing). The total parasitic inductance in the current commutation loop could cause high overshoot voltage on S1 during turn off transient, as shown in (1).

$$V_{S1} = V_{DC} + L_{CCL} \cdot di/dt \quad (1)$$

Where

$$L_{CCL} = L_{tp} + L_{d1} + L_{s1} + L_{d2} + L_{s2} + L_{tn} \quad (2)$$

V_{S1} is the drain to source voltage of high switch S1. L_{CCL} is the sum of all the parasitic inductance in the current commutation loop. In the meantime, the quality factor of the resonant circuit formed in the current commutation loop is:

$$Q_{CCL} = \frac{1}{R_{total}} \sqrt{\frac{L_{CCL}}{C_{total}}} \quad (3)$$

Where R_{total} is the total resistance of current commutation loop, usually determined by the transistor on-resistance. C_{total} is the total capacitance in the CCL, which is the total series capacitance of device junction capacitor. Large parasitic inductance could cause high voltage overshoot on power semiconductor devices. Large quality factor could increase ringing duration, causing high switching loss. The high frequency oscillations can also cause detrimental electromagnetic interference (EMI) issues [1] [2]. Both R_{total} and C_{total} are determined once power devices are selected, but parasitic inductance in the CCL can be reduced by package design.

The multichip structure is widely adapted when utilizing SiC MOSFETs, whose high current withholding capability is limited [3] [4]. In such structure, the transistors are paralleled to increase current handling abilities. Consequently, the parasitic inductance inside a multichip power module is more complicated due to its paralleled layout structure. Thus, to fully utilize the advantages of WBG power devices, it is crucial to address the oscillation issues caused by parasitic inductance in multichip power modules.

The parasitic inductance in power modules is modeled in many papers. In [7], the total parasitic inductance is modeled as current commutation loop (CCL) area. Based on that, switching cell concept are adopted to reduce the current commutation loop area. The loop area model was also used in [9], a multiloop design method is developed for multilayer PCB and applied to several examples. The loop area model is very straightforward and could provide guidance for layout design. However, the mutual inductance between paralleled branches on the same conductor are not included. A detailed parasitic inductance model was developed in [19] for the planar bus bar of an IGBT H bridge. The relationship between current paths and parasitic inductance was firstly illustrated. The parasitic inductance was extracted in [10] using FEA software, however, it was not clear whether the mutual inductance is included. The result in [10] showed the simulated turn off voltage overshoot in [10] is about 14% smaller than their measurement. Up to the time this paper is written, the mutual inductance between paralleled branch inside the multichip power module has not been thoroughly discussed.

Many methods have been developed to reduce the parasitic inductance during package layout design process. For most methods developed for bond wires on DBC structure, the parasitic inductance reduction is realized by reducing CCL loop area. Some general design considerations were summed up in [7]. Other than general design considerations, design methodologies are also proposed in many researches. The use of switching cell concept proposed in [7] has large impact on power module design. As adopted in [8]. Some designs applied hybrid structure. Bond wires and planar hybrid structure was proposed in [20], PCB and DBC hybrid structures were proposed in [17] and [21]. The mutual inductance considered in [17] is between drive loop and CCL instead of paralleled branches. It is discovered in [18] that interleaving half bridge legs can reduce parasitic inductance, but the reason is not fully explained. Furthermore, the resulting structure is difficult to be connected to bus bars because the positive and negative terminals are separated. The mutual inductance between loops was discussed in [9], but the analysis is for conductor loops in PCB design which is not suitable for high power module applications.

Other than trying to reduce parasitic inductance in bond wire package, many different packaging technologies have been developed to realize planar 3D structure. As illustrated in [6] [10] [12] - [16], planar 3D structures can reduce parasitic inductance due to the elimination of bond wires. However, the planar 3D structure greatly increases the fabrication difficulty and has reliability issues. As a result, bond wires on DBC structure is still the most suitable package technology for SiC multichip power module.

Different from the above-mentioned researches, the mutual inductance among paralleled branches are first thoroughly discussed in this paper. An accurate parasitic inductance model is developed that could accurately predict voltage overshoot and oscillation during switching transient. Then, a wire bonded package layout based on the developed model is proposed for SiC multichip power module that could reduce parasitic inductance without increasing fabrication difficulty. The paper will be organized as follows: the parasitic inductance model for multichip power module is developed in Chapter II, the proposed layout structure will be presented in Chapter III, Measurement results will be shown in Chapter IV, Chapter V concludes this paper.

II. Develop Parasitic Inductance Model for Multichip Power Modules

A commercial half bridge multichip power module layout shown in Fig.2 (a) is analyzed in this paper as a base line. The positive (P), negative (N) and output (OUT) terminal bars are hidden in Fig.2 (b) so the layout can be clearly shown. The schematic can be found in Fig.2 (c). This SiC MOSFETs half bridge multichip power module has the power rating of 1200 V 300 A. Six SiC MOSFETs and six antiparallel SiC Schottky diodes are paralleled as the top switches of the half bridge, same construction for low switches. The gate drives are connected via high gate (HG), low gate (LG), high source (HS) and low source (LS) pins.

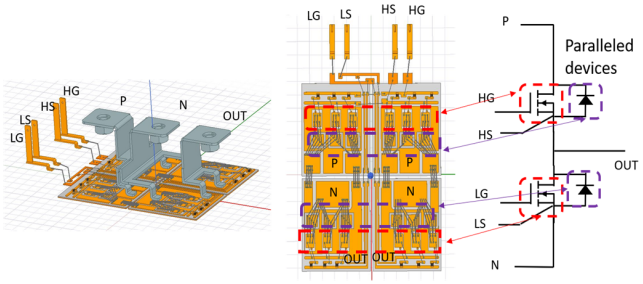


Fig.2 Commercial SiC multichip power module (CAS300M12BM2) layout. (a) overview of SiC power module with case hidden, (b) Module layout with terminals hidden and (c) Schematic of the half bridge power module

It can be observed that there are in total six paralleled paths in this power module, each of them contains one MOSFET and one diode as top switch and one MOSFET and one diode for bottom switch. In this paper, the paralleled paths are referred as branches.

If power semiconductors are considered as open circuit, the CCL loop of each paralleled half bridge consists of three conduction paths. As shown in Fig. 3 (a). The first conduction path (red arrow) includes positive terminal (P) and DBC copper plane that connects to the drain of top switches and cathodes of diodes. Second conduction path (black arrow) includes bond wires that connect the source pads of top switches, diodes anodes to the copper plane that leads to low switch drains and low diodes cathodes. Finally, the third conduction path (green arrow) includes bond wires connect low switch source pads and

low diodes anodes to negative terminal (N). It is worth noting that voltage overshoot and oscillation is due to the parasitic inductance of CCL, where there is high $\frac{di}{dt}$, so the inductance of the output conduction path has little impact. As a result, the output terminal is not analyzed in this paper.

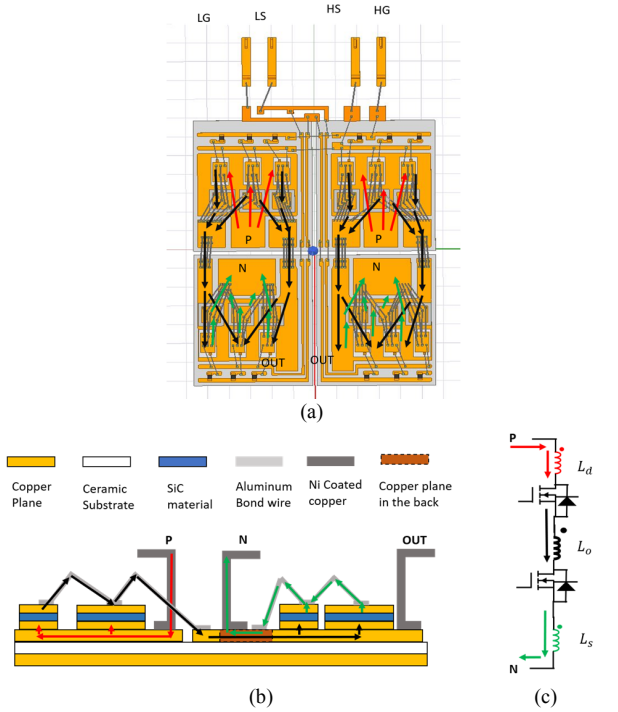


Fig.3 Illustration of the three conduction paths of the current commutation loop from (a) top view, (b) side view and (c) the parasitic inductance related to each conduction path in the schematic of half bridge topology

In Fig.3 (a) the conduction paths are shown in top view, in Fig.3 (b), the side view of the module is shown, for clarity, gate drive loops and gate resistors are hidden. Different materials are labeled with different colors. Because the copper plane that connected to negative terminal (N) occupies the same space with the copper plane that connects to output terminal when see from the side. To distinguish, difference colors are used.

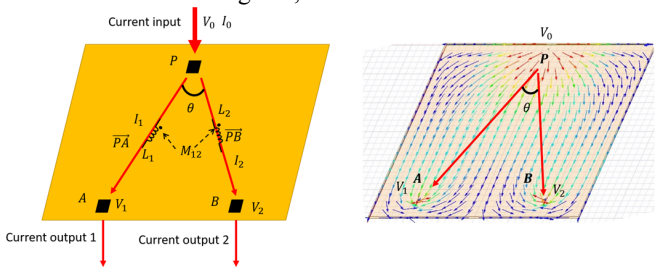


Fig.4 Current paths on a copper plane with one input and two outputs. (a) Current paths illustration, and (b) simulated current vector

To accurately model the parasitic inductance of the three conduction paths, the method of partial element equivalent circuit (PEEC) is used. In PEEC method, the total inductance of the CCL is the sum of the self partial inductance of each conductor and the mutual inductance between each pair. As can be seen in Fig.3 (a), the current paths for each paralleled branch are different in location. To discuss the mutual inductance between paralleled branches, a simple model is built as shown in Fig.4.

As can been seen in Fig.4 (a). Point P, A, B are three points on the copper plane, with voltage potential V_0, V_1 and V_2 respectively, Current flows in the conductor from point P and flows out the conductor from A and B. During normal operation of a multichip power module, such scenario is very common. The electric field and current density in the conductor can be calculated as:

$$\vec{E} = -\nabla\varphi \tag{4}$$

$$\vec{J} = \sigma\vec{E} = -\sigma\nabla\varphi \tag{5}$$

Where φ is the electric potential. σ is the conductivity of the conductor, in this case, copper. It can be seen from (5) that the current density will be concentrated on the path where the voltage potential decreases the fastest, which means the current will flows through the path with minimum impedance. The current density vectors are simulated in Ansys Maxwell software and shown in Fig. 4 (b). When $V_1 = V_2$, the potential difference between PA and PB are the same, which is true for multichip power module, then $I_1 = I_2 = \frac{I_0}{2}$. The angle between the two current paths is θ, as shown in Fig. 4 (a) and (b).

The magnetic field energy generated by current I_1 is:

$$W_1 = \iiint \overrightarrow{B_1} \cdot \overrightarrow{H_1}\, dV = \iiint \mu_0 \overrightarrow{H_1}^2\, dV \tag{6}$$

Where μ_0 is the permeability of the air, because for the case of power modules, with the absence of magnetic cores of inductors, most of the magnetic flux flows through air.

The mutual inductance between current path $\overrightarrow{PA}$ and $\overrightarrow{PB}$ can be calculated as:

$$M_{12} = \frac{\iiint \overrightarrow{B_1}\cdot\overrightarrow{H_2}\, dV}{I_1 I_2} = \frac{\iiint \mu_0 \cdot \overrightarrow{H_1}\cdot\overrightarrow{H_2}\, dV}{I_1 I_2} \tag{7}$$

Where B_1 is the magnetic flux density vector generated by I_1, H_1 and H_2 are the magnetic field generated by I_1 and I_2 respectively.

The magnetic flux vector is perpendicular with the current direction vector. As a result, the position angle between the magnetic flux vectors generated by current I_1 and I_2 is also θ. (7) can be rewritten as:

$$M_{12} = \frac{\iiint \mu_0 H_1 H_2 cos\theta\, dV}{I_1 I_2} \tag{8}$$

In multichip power module, the paralleled devices share the same conductors that connect to their drains and sources. The positions of paralleled devices are very close to each other in traditional design, such as the one in Fig. 2. The position angles between them is very small, leading to large mutual inductance.

Since the self and mutual inductance is obtained, the parasitic inductance model of multichip power module can be developed. In the model, the self-inductance and mutual inductance between all the conductors should be included. To clarify the definition, the self-inductance inductance and mutual inductance between arbitrary two paralleled branches are shown in Fig. 5.

The self-inductance of the three conduction paths in branch i are denoted as L_{di}, L_{oi}, and L_{si}, respectively. They represent the partial inductance of the three conduction paths shown in Fig.3. The mutual inductance between each two of the partial

inductances is shown in Fig.5.

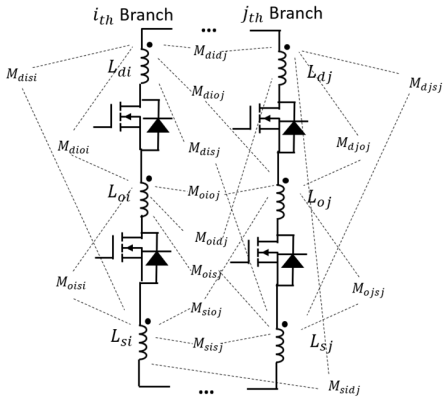


Fig.5 Self and mutual inductance of paralleled branch i and j.

The total parasitic inductance in a multichip power module can be described by the following matrix:

$$\boldsymbol{L_{total}} = \begin{bmatrix} \boldsymbol{L_{b1}} & \boldsymbol{M_{b12}} & \cdots & \boldsymbol{M_{b1i}} & \boldsymbol{M_{b1j}} \\ \boldsymbol{M_{b12}} & \boldsymbol{L_{b2}} & \cdots & \boldsymbol{M_{b2i}} & \boldsymbol{M_{b2j}} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \boldsymbol{M_{b1i}} & \boldsymbol{M_{b2i}} & \cdots & \boldsymbol{L_{bi}} & \boldsymbol{M_{bij}} \\ \boldsymbol{M_{b1j}} & \boldsymbol{M_{b2j}} & \cdots & \boldsymbol{M_{bij}} & \boldsymbol{L_{bj}} \end{bmatrix} \tag{9}$$

Where

$$\boldsymbol{L_{bi}} = \begin{bmatrix} L_{di} & M_{dioi} & M_{disi} \\ 0 & L_{oi} & M_{sioi} \\ 0 & 0 & L_{si} \end{bmatrix} \tag{10}$$

$$\boldsymbol{M_{bij}} = \begin{bmatrix} M_{didj} & M_{dioj} & M_{disj} \\ M_{oidj} & M_{oioj} & M_{oisj} \\ M_{sicj} & M_{sioj} & M_{sisj} \end{bmatrix} \tag{11}$$

$\boldsymbol{L_{total}}$ represents the total loop inductance of a multichip power module with j paralleled branches. $\boldsymbol{L_{bi}}$ represents the total loop inductance of branch i, it consists of the self-inductance of each conduction paths and the mutual inductance between each two of the three conduction paths of branch i. $\boldsymbol{M_{bij}}$ represents the total mutual inductance between branch i and branch j.

With the developed model, the voltage between the drains and sources of high switches during turn off transient can be expressed as:

$$\begin{bmatrix} \boldsymbol{V_1} \\ \boldsymbol{V_2} \\ \vdots \\ \boldsymbol{V_i} \\ \boldsymbol{V_j} \end{bmatrix} = V_{DC} + \boldsymbol{L_{total}} \cdot d \begin{bmatrix} \boldsymbol{I_{b1}} \\ \boldsymbol{I_{b2}} \\ \vdots \\ \boldsymbol{I_{bi}} \\ \boldsymbol{I_{bj}} \end{bmatrix} / dt \tag{12}$$

Where

$$\boldsymbol{I_{bi}} = \begin{bmatrix} i_{bi} \\ \vdots \\ i_{bi} \end{bmatrix} \tag{13}$$

$\boldsymbol{I_{bi}}$ represents the current flow through i^{th} branch, it is a single column j rows matrix. V_i represents the drain to source voltage of the high switch of branch i. V_{DC} is the DC bus voltage added between positive and negative terminal.

It can be observed from (9) to (13), the overshoot voltage during switching off transient is not only determined by the CCL inductance of the individual branch, but also largely depend on the mutual inductance between paralleled branches.

Particularly, with the traditional model where only the loop inductance between positive terminal and negative terminal are considered, the total inductance of the individual branch cannot be obtained, the parasitic inductance would be underestimated.

The self and mutual inductance of each conduction path is extracted with Ansys Q3D software. To illustrate the influence of mutual inductance, the inductance matrix of the first two branches from the left in Fig. 7 are shown as (14) – (16) as example.

$$\boldsymbol{L_{b1}} = \begin{bmatrix} 12.20 & -1.22 & -6.12 \\ 0 & 9.49 & -4.16 \\ 0 & 0 & 19.32 \end{bmatrix} \text{nH} \tag{14}$$

$$\boldsymbol{L_{b2}} = \begin{bmatrix} 11.95 & -1.01 & -6.06 \\ 0 & 8.94 & -4.19 \\ 0 & 0 & 18.83 \end{bmatrix} \text{nH} \tag{15}$$

$$\boldsymbol{M_{b12}} = \begin{bmatrix} 11.91 & -0.93 & -6.05 \\ -0.93 & 7.66 & -4.14 \\ -6.05 & -4.14 & 17.61 \end{bmatrix} \text{nH} \tag{16}$$

(14) and (15) are the total loop inductance of branch 1 and branch 2, respectively, as defined in (10). (16) is the mutual inductance between branch 1 and branch 2. As can be seen, due to small position angle, the mutual inductance between the two paralleled branches are large. Consequently, the total loop inductance of the power module will be large, which determines the overshoot voltage between the drains and sources of the devices, according to (12).

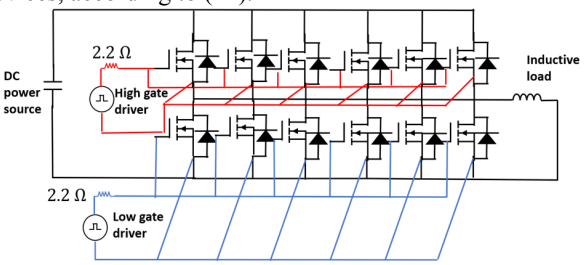


Fig.6 Circuit simulation schematic (without parasitic inductance)

To verify the developed model, the inductance matrix is imported into Ansys Simplorer. The switching waveforms are obtained in a double pulse tester set up as shown in Fig.6. In the circuit simulation, SiC MOSFETs and SiC Schottky Diodes are characterized using Ansys Simplorer's device characterization tool. Both static and dynamic characteristics from the data sheets are fitted in. The circuit simulation schematic without parasitic inductance can be found in Fig.6. The gate resistor used for both turn on and turn off is 2.2 Ω. The final simulation schematic with extracted parasitic elements of both power loop and drive loop included are shown in Fig. 7. The experiment set up is described in detail in Chapter IV. The circuit set up in circuit simulation is exactly the same with experiment. The voltage between the P terminal and OUT terminal are measured and simulated. The results are shown in Fig.8.

As can be seen in Fig.8 (a) and (b). The simulated switching waveforms match experiment very well, in both frequency and magnitude. This verified the accuracy of the developed model.

To better show the importance of mutual inductance, another simulation is conducted where only the self-inductance of each branch is extracted. Under the same testing condition, the result is shown in Fig 8. (c). The turn off overshoot voltage in Fig. 8 (c) is about 25 V, while the turn off overshoot voltage in Fig.8 (b) is about 35 V. It can be seen that, neglecting mutual

inductance between paralleled branches will have large influence on model accuracy. More importantly, it could lead to an underestimation of voltage overshooting on device, which could cause dangerous situations such as device failure.

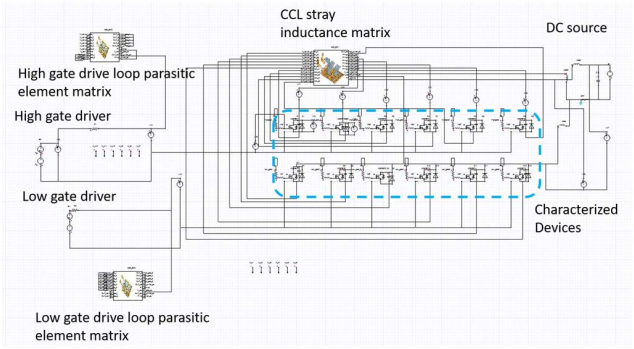


Fig.7 Circuit simulation schematic (with parasitic inductance included)

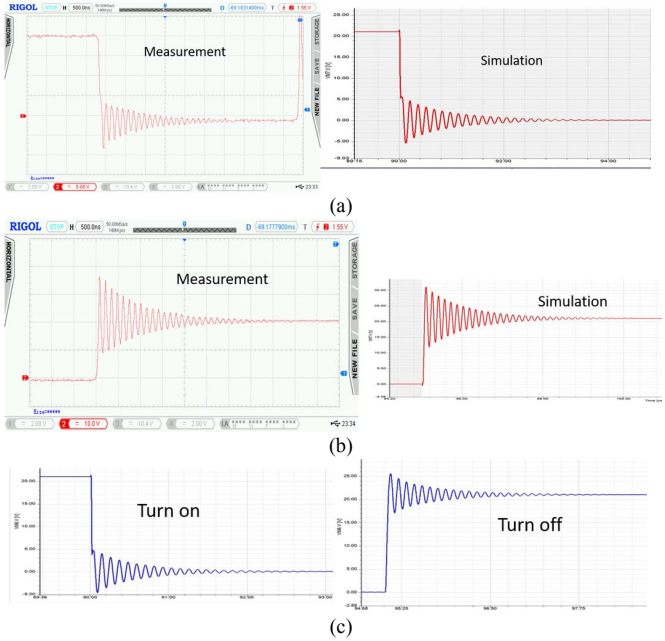


Fig.8 Switching waveform comparison (a) Turn on transient (b) Turn off transient (c) Turn on and turn off transient waveforms of model with mutual inductance neglected.

III. Improved Layout Structure for Half Bridge Multichip SiC MOSFET Power Modules

Based on the developed model in Chapter II, the total parasitic inductance of the power module is largely influenced by the mutual inductance between the branch and other paralleled branches. In this Chapter, the concept of mutual inductance cancellation is presented, a novel layout structure is proposed based on the concept.

It can be observed from (10) to (11), the mutual inductance of two branches includes two kinds of contributors: the mutual inductance between the three conduction paths of the individual branch, as shown in (10), and the mutual inductance between the two branches, as shown in (11). To reduce the total parasitic inductance of a branch, the two kinds of mutual inductance should both be negative to cancel the self-inductance. To realize it, two methods are used to achieve mutual inductance cancellation. 1. The negative mutual inductance between the three conduction paths of the same branch should be increased as much as possible. 2. The position angle of conduction paths on the same conductor should be 180° to achieve large negative mutual inductance or small positive mutual inductance between paralleled branches.

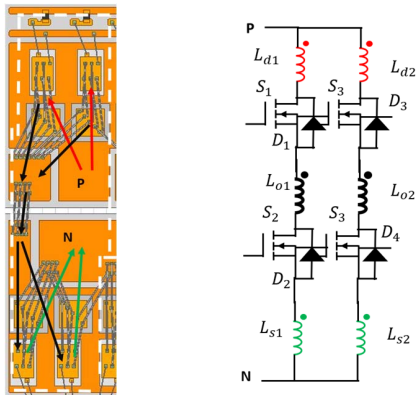


Fig.9 Illustration of self and mutual inductance between two paralleled branches for original layout (a) conduction paths and (b) associated parasitic inductances.

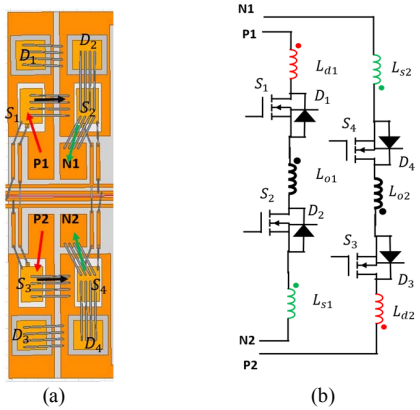


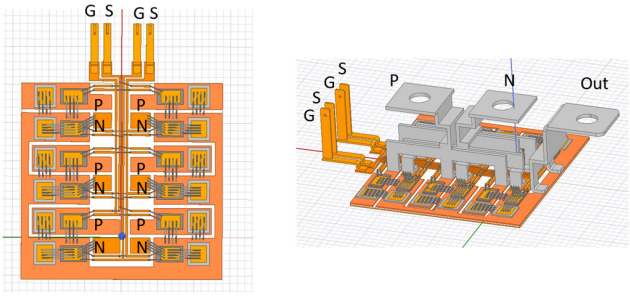
Fig.10 Illustration of self and mutual inductance between two paralleled branches for proposed layout with mutual inductance cancellation concept (a) conduction paths and (b) associated parasitic inductances

In Fig. 9 (a) and Fig. 10 (a), two paralleled branches of original layout and proposed layout are shown. The three conduction paths and their associated parasitic inductance are shown in Fig. 9 (b) and Fig. 10 (b). In the original layout, as shown in Fig.9, the mutual inductance between conduction paths of the same branch is negative because the position angle is larger than 90°, however, the mutual inductance between L_{d1} and L_{s1} is small due to the large distance between them. On the other hand, the mutual inductances between conduction paths on the same conductor, such as L_{d1} and L_{d2}, are positive and large due to the very small position angle. In the layout with mutual inductance cancellation concept, the two paralleled branches are separated and positioned with 180° position angle. As a result, both mutual inductance between L_{d1} and L_{d2}, and the mutual inductance between L_{d1} and L_{s1}, are negative. Thus, the total parasitic inductance of each branch is reduced.

A half bridge multichip power module with the same power

rating as the original module is designed, as can be seen in Fig. 11. The separated positive and negative terminals are connected with bus bar in the middle of the module.

The distance between paralleled devices, and the distance between paralleled branches are determined by heat dissipation angle [5] and power clearance distance IEC 60664-1. The minimum distance between dies can be achieved by choosing the larger distance of the two, to make sure there will be no heat overlaps or power breakdown. Driving signal are connected by kelvin connection, so the drive loops and power loops are well decoupled. The terminal bars that connect the module to the DC source and AC output are soldered on DBC copper, as shown in Fig. 11. The positions of these terminals are the same with original module in Fig. 2 (a). In this way, the connection between power module and application circuit does not require any special design.



(a) (b)

Fig.11 Proposed layout for multichip power module. (a) Proposed layout design with terminals hidden and (b) Proposed module design with terminals

The parasitic inductance of first two branches from the top in Fig. 11 are shown as (17) – (19) as example in comparison to (14) – (16).

$$\boldsymbol{L_{b1\_p}} = \begin{bmatrix} 13.35 & -0.04 & -7.87 \\ 0 & 1.61 & -0.21 \\ 0 & 0 & 14.07 \end{bmatrix} \text{nH} \quad (17)$$

$$\boldsymbol{L_{b2\_p}} = \begin{bmatrix} 9.53 & -0.05 & -5.74 \\ 0 & 1.64 & -0.17 \\ 0 & 0 & 10.63 \end{bmatrix} \text{nH} \quad (18)$$

$$\boldsymbol{M_{b12\_p}} = \begin{bmatrix} 6.7 & -0.23 & -4.84 \\ -0.23 & 0.008 & -4.14 \\ -4.84 & -4.14 & 5.49 \end{bmatrix} \text{nH} \quad (19)$$

As can be seen, the mutual inductance between paralleled branches are reduced. They are still positive because the two paralleled branches still have to share the same conductor that connect to the terminals. The coupling coefficient of mutual inductance between the two paralleled branches is shown in Fig. 12. It can be observed that the proposed layout has much lower mutual inductance. As a result, it can be expected that the turn off voltage overshoot and oscillation during transition in the proposed module will be significantly reduced.

Both modules are simulated in double pulse tester circuit, the voltage between the drain and source of the MOSFET in the first branch (from the left) is shown in Fig.13 as an example. By comparing the obtained drain to source voltage, the total parasitic inductance in CCL of two package layout can be compared. As can be seen in Fig.12 and Fig. 13 due to the reduced parasitic inductance, the over shoot and oscillation are both significantly reduced in the proposed module.

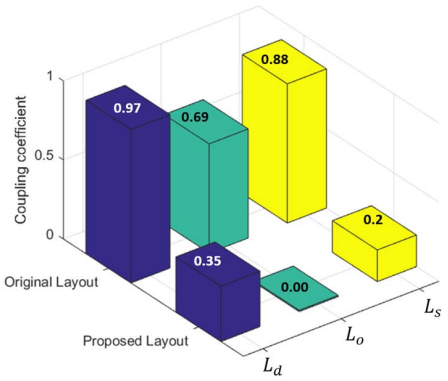


Fig.12 Comparison of coupling coefficient between the two paralleled branches for original and proposed layout

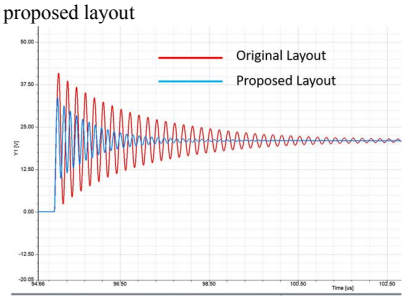


Fig.13 Simulated drain to source voltage of top switch of the first branch during turn off transition of original and proposed layout

IV. Experimental Verification

To verify the previous analysis and the effectiveness of mutual inductance cancellation concept, a half bridge multichip power module with the proposed layout is fabricated and tested in double pulse tester set up.

TABLE I
Comparison between Bare die on PCB and Wire bonded DBC process

	Substrate Material	Trace material	Wire Bonding Technology
Bare die on PCB process	FR4	Bare copper	Conductive Epoxy (EPOTEK H20E)
Wire bonded DBC process	Al_2O_3 ceramic	Bare copper	Ultrasonic welding

The prototype of the proposed module was fabricated with bare die on PCB process. The comparison between the two process is shown in Table I. The patterns and thickness of PCB traces are exactly the same with DBC copper traces. With same layout, the parasitic inductance between the two process are the same. As a result, bare die on PCB process provides a good alternative to evaluate the parasitic inductance of power module without the high cost of DBC process when the heat dissipation requirement is not strict.

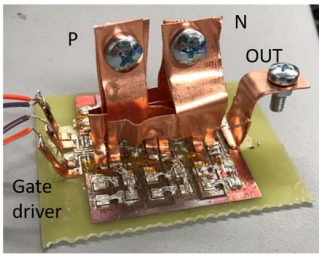


Fig.14 Prototype of the proposed half bridge multichip power module

The switches of the proposed half bridge multichip power module consist of 12 SiC MOSFETs (CPM2-1200-0025B) and 12 SiC Schottky diodes (CPW51200Z050B), same with the original module. The fabricated prototype of the proposed module is shown in Fig.14. It should be pointing out that the proposed layout structure could be built with the exact same procedure with wire bonded DBC process, which means the proposed structure will not increase any fabrication difficulty.

The double pulse tester set up is widely used in power module switching performance evaluation [7]. The experiment set up is shown in Fig. 15. The DC power supply is connected to the power module DC bus bar, a 1000 μF decoupling capacitor is added between the positive and negative terminals of the power module so that the cables that connected to DC power supply won't influence the result. An inductor with 33 μH inductance is served as load inductor. Because the fabricated prototype has no insulating silica gel, the two modules are tested under 20 V/18 A and 50 V/30 A condition for safety consideration.

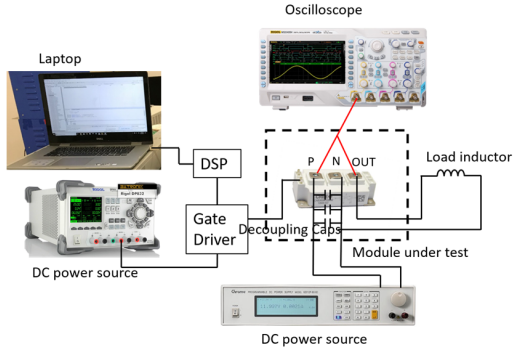
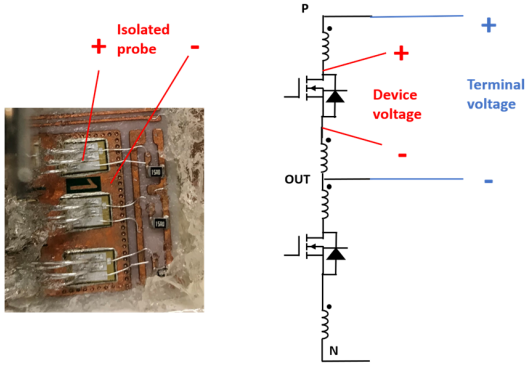


Fig.15 Double pulse test setup

To obtain accurate voltage between the drain and source of the device, the modules are opened, isolated probes are added directly between the drain and source of each device, as shown in Fig.16 (a).

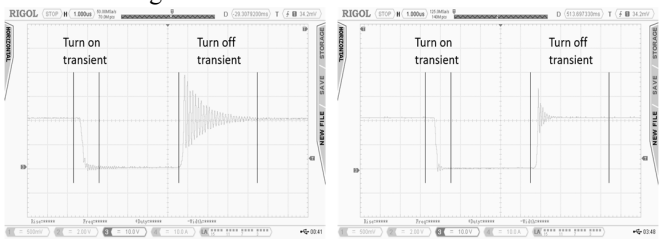


(a) (b)

Fig.16 Voltage measurement illustration. (a) Illustration of Probe position on the device and (b) Difference between terminal voltage and device voltage

The switching waveforms of proposed and original module are shown in Fig. 17. During turn on transition, the oscillation of the device is caused by diode reverse recovery, the measured device drain to source voltage is very small because the device has been turned on. During turn off transition, the voltage overshoot and oscillation due to parasitic inductance is more obvious. To better observe the peak voltage and oscillation, the enlarged turn off transient waveforms of the device drain to source voltage are shown in Fig. 18.

For the 20 V/ 18 A test, the original module has a peak voltage of 39 V. The ringing duration is 3 μs. In comparison, the peak voltage of the proposed module is 27 V and the ringing duration is just 1 μs. The ringing duration time is measured from when the voltage reaches rated value to the time when the oscillation magnitude is less than 10% of the rated value.



(a) (b)

Fig.17 Turn on and turn off voltage waveforms of original module and proposed module under 20 V/18 A test condition (a) original module and (b) proposed module

For the 50 V/ 30 A test, the original module has a peak voltage of 140 V is observed. The ringing duration is 3 μs. In comparison, the peak voltage of the proposed module is 80 V. Additionally, due to reduced quality factor, the ringing duration is reduced to 0.8 μs. It can be observed that the overshoot voltage is higher for high power tests. In the meantime, the benefit of low parasitic inductance is more obvious.

The voltage overshoot in both cases is smaller with the proposed module. The ringing duration rime is also reduced. Furthermore, the high frequency EMI caused by the voltage oscillation can also be significantly reduced in the proposed module. Due to the limitation of in-lab fabricating and packaging process, the prototype does not have sufficient voltage insulation for high voltage tests, but it is sufficient to validate the parasitic inductance reduction.

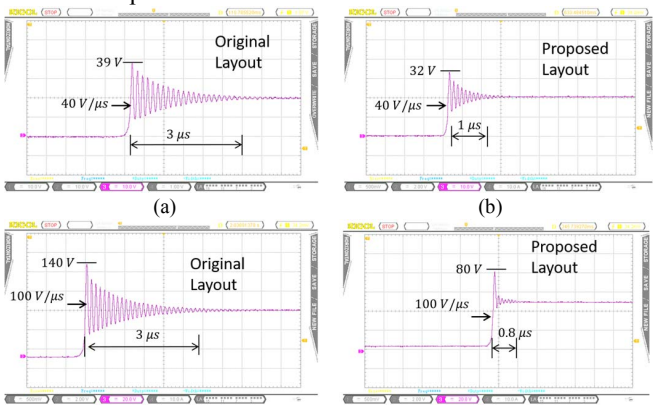


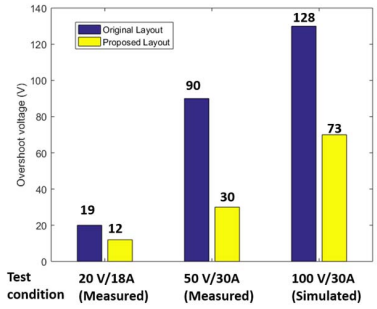
Fig.18 Voltage waveforms during turn off transient of original and proposed layout under 20 V and 50 V tests. (a) Turn off voltage of original layout under 20 V/ 18 A test, (a) Turn off voltage of proposed layout under 20 V/ 18 A test, (a) Turn off voltage of original layout under 50 V/ 30 A test, (a) Turn off voltage of proposed layout under 20 V/ 30 A test.

The switching energy of a device can be calculated by (20). Where $v_{ds}(t)$ is the drain to source voltage of the transistor, $i_d(t)$ is the current flows through the transistor. t_{tr} is the

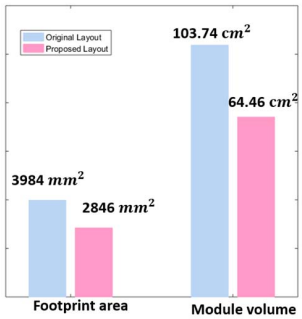
transient time when the product of $v_{ds}(t)$ and $i_{ds}(t)$ is not zero.

$$E_{sw} = \int_{t_{tr}} v_{ds}(t) \cdot i_d(t) dt \quad (20)$$

It can be seen that the transient time t_{tr}, which is ringing duration time in Fig.18 plays a crucial role in switching loss. With lower quality factor due to reduced parasitic inductance, the proposed module can achieve much smaller switching loss. Parameters including peak voltage, foot print and volume are compared and shown in Fig. 19.



(a)



(b)

Fig.19 Parameter comparison between proposed power module and original power module: (a) peak overshoot voltage comparison under different test conditions and (b) foot print area and module volume comparison

V. Conclusion

In this paper, the parasitic inductance model is developed for SiC multichip power module with wire bonded package. In the developed model, the mutual inductance between paralleled branches are recognized and included. From the analysis and simulation, the often-neglected mutual inductance between paralleled branches have significant impact on total parasitic inductance of the module. Based on the developed model, a different layout structure is proposed for half bridge multichip power module package that could effectively reduce the total parasitic inductance. The proposed layout could achieve lower switching loss, lower turn off voltage overshoot and lower EMI without increase any manufacturing difficulty. The analysis and effectiveness of the proposed module are verified in both simulation and experiment.

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