# ECE 2031 Group 1 Proposal

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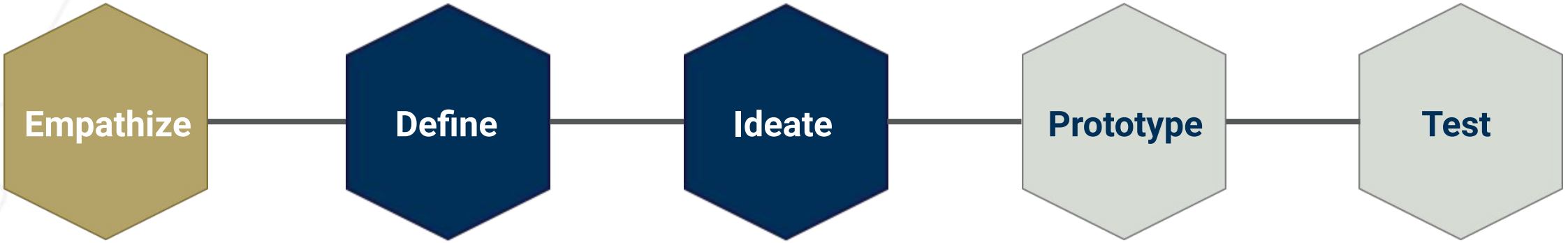
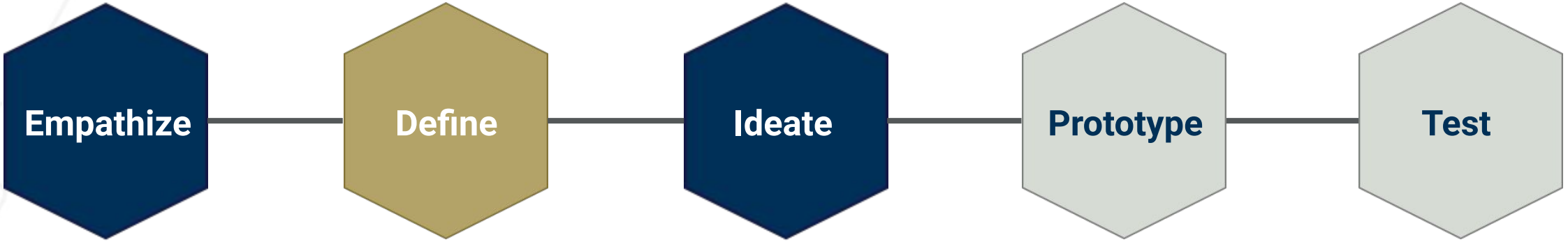
# Introduction

# Introduction - Design Thinking Approach




- **Understand the Challenge:** SCOMP's limited internal memory restricts its potential, especially for data-heavy projects.
- **User Needs:** SCOMP users require an easy-to-use peripheral to store and retrieve data.

# Introduction - Design Thinking Approach




- **Problem Statement:** How might we design an external memory peripheral that expands SCOMP's memory capacity while maintaining ease of use?
- **Key Requirements:**
  - Integrate with SCOMP without processor modifications.
  - Provide a straightforward interface for developers.
  - Use reserved I/O addresses 0x70-0x7F for accessibility.

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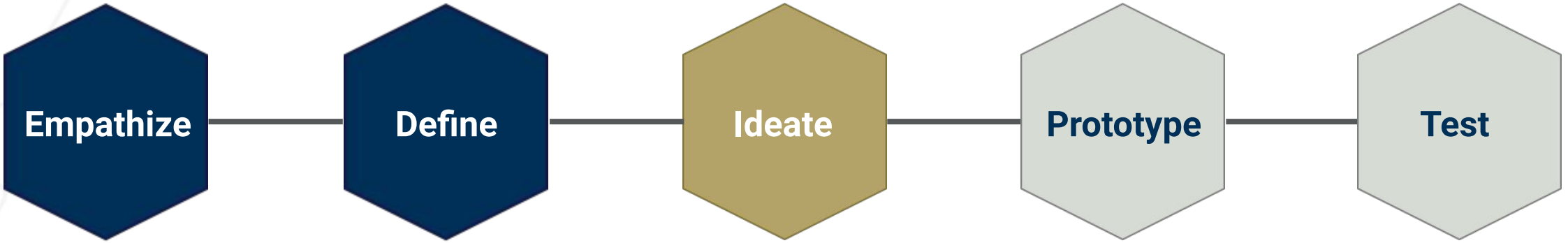
# Introduction - Design Thinking Approach




- **Brainstorm Features:** Considered ideas like address auto-increment, configurable data lengths, and write-protection for added functionality.
- **Narrowing Down:** Decided on a set of features that best balance user needs and project feasibility, focusing first on core functionality.

# Technical Approach

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# Technical Approach

- Utilize Altera's altsyncram megafunction to implement the core memory functionality.
- Create an External Memory Peripheral with seamless I/O interaction through SCOMP's existing I/O instructions.
- Integrate an Address Register that specifies the memory address for subsequent data access operations (read/write).

| ADDRESS | REGISTER NAME | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x70 | Adress Register | address_register[15:0] | | | | | | | | | | | | | | | |

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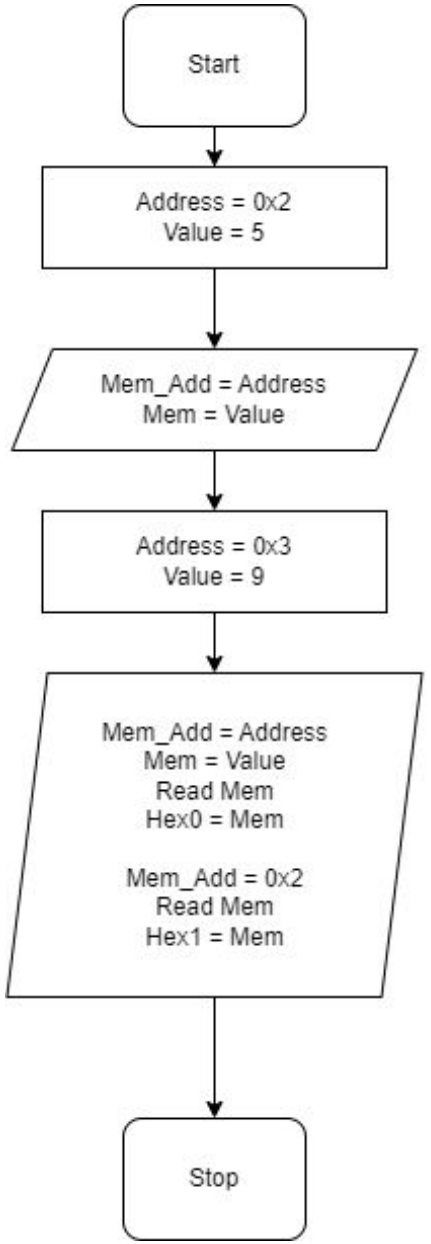
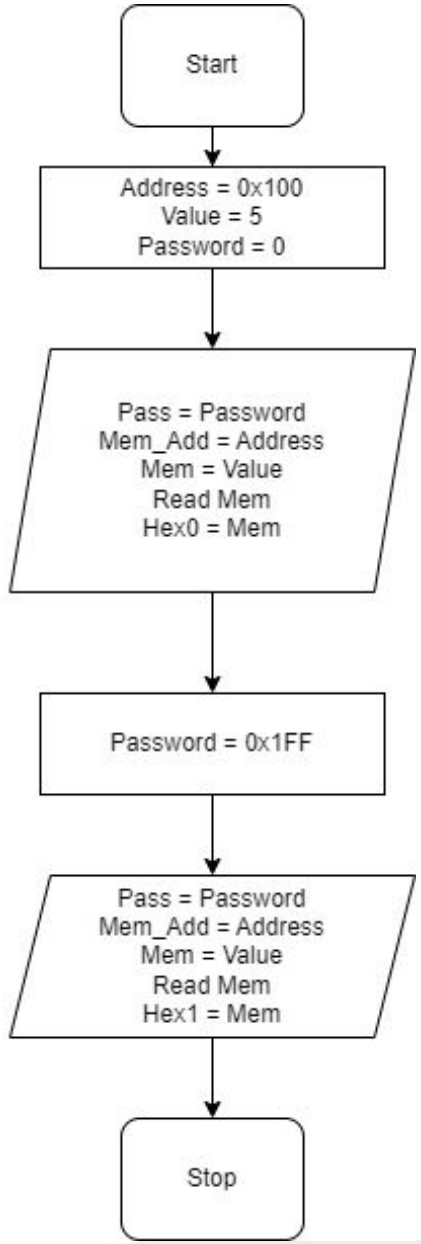
# Features

- Write Protection
  - Implement write protection for a predefined range of lower memory addresses to prevent accidental overwrites.
- Stack Memory
  - Designate a memory section to handle stack operations, supporting last-in, first-out (LIFO) data structure functionality.
- Queue Memory
  - Designate a memory section to handle queue operations, supporting first-in, first-out (FIFO) data structure functionality.
- Access Control with Password
  - Integrate an access control mechanism for a range of memory, requiring a password for memory read or write access.

# Experiments

- Leftmost flowchart tests multiple addresses storing different values
  - Expected value of Hex0 is 9, Hex1 is 5
- Rightmost flowchart tests password write protection at high address values
  - Expected value of Hex0 is 0, Hex1 is 5
- Our peripheral met the expected values of both tests

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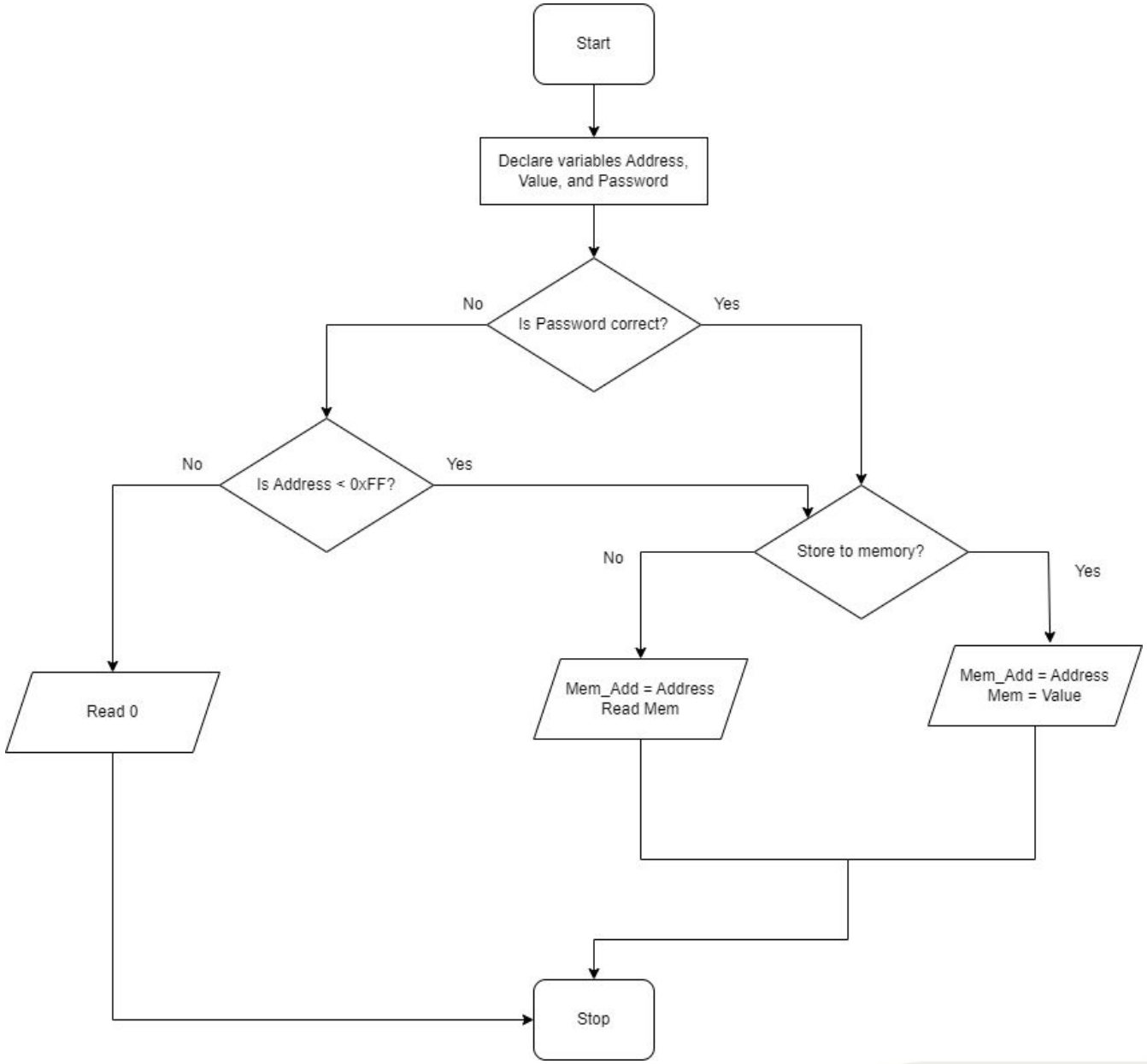
# Demo Idea

- Concept of a demonstration code that lets the user input values into addresses with password protection
  - Having the demo loop and display values on the 7-segment of the DE10 board is an additional goal
  - Incorporating showing stack and queue type of memory is also a goal



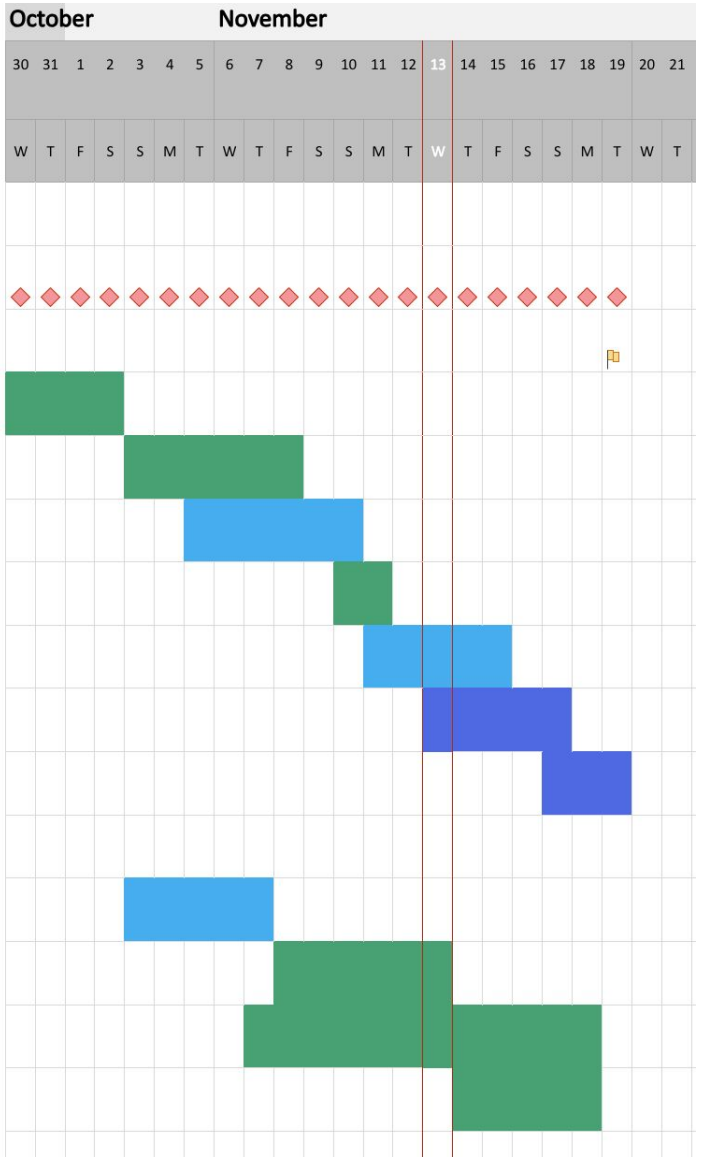
# Management Plan

# Chart

Project start date: 10/30/2024

Scrolling increment: 5

| Milestone description | Category | Assigned to | Progress | Start | Days |
|---|---|---|---|---|---|
| **Project development** | | | | | |
| Complete Project Implementation | Goal | Ali, Tayseer, Josh, Naeim | 80% | 10/30/2024 | 21 |
| Turn in Full Project | Milestone | | | 11/19/2024 | 1 |
| Project Planning | On Track | Ali, Tayseer, Josh, Naeim | 100% | 10/30/2024 | 4 |
| Basic Peripheral Functionality | On Track | Tayseer, Josh | 100% | 11/3/2024 | 6 |
| Basic Peripheral Testing | Low Risk | Ali, Naeim | 95% | 11/5/2024 | 6 |
| Additional Functionality Planning | On Track | Ali, Tayseer, Josh, Naeim | 100% | 11/10/2024 | 2 |
| Additional Functionality Implementation | Low Risk | Naeim, Tayseer | 65% | 11/11/2024 | 5 |
| Additional Functionality Testing | Med Risk | Ali, Josh | 35% | 11/13/2024 | 5 |
| Finalizing Project | Med Risk | Ali, Tayseer, Josh, Naeim | 15% | 11/17/2024 | 3 |
| **Documentation** | | | | | |
| Technical Checkpoint | Low Risk | Ali, Tayseer, Naeim | 100% | 11/3/2024 | 5 |
| Proposal Presentation | On Track | Ali, Josh, Naeim | 100% | 11/8/2024 | 6 |
| Final Demo | On Track | Ali, Josh, Tayseer | 70% | 11/7/2024 | 12 |
| Demo Presentation | On Track | Tayseer, Naeim, Josh | 15% | 11/14/2024 | 5 |




- Comprehensive Gantt Chart of what our timeline for the project is
  - Displays our progress for each part thus far, how many days we would estimate the work to be done, as well as how risky our current implementation of the task is to be prone to issues or generally not presenter-ready
- Low-Risk areas
  - Technical Checkpoint
  - Peripheral testing
  - Functionality implementation
- Med-Risk areas
  - Additional Functionality Testing
  - Finalizing project

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# Division of Labor

- Divided work amongst our team members during project planning and at the end of each small milestone
  - Small milestones consist of after finalizing our peripheral functionality/testing, and this presentation for example
- Check-ups are normally on Monday, Tuesday, and Wednesday
  - We all meet up in person on these three days to make sure that we are on track and because working in person is a lot more productive for us
  - If any issues arise, we can always have each other to help
- All other days we work individually
  - We would work on things like testing our peripheral individually so that when we do meet up, we have multiple ideas on approaching a topic

# Conclusion

- Our project expands SCOMP's memory with a secure and user-friendly external peripheral.
- Core features include password-protected access, read/write protection, and support for different types of memory structures.
- If the different memory structures cannot be implemented, we will pivot to using auto address increment to maintain usability.
- This peripheral has potential applications in embedded systems and secure data management.

# Q & A

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