HW2

States:   
11 = FIRST  
01 = SECOND  
10 = THIRD

Async rst high causes state to reset to FIRST.

A screenshot of a computer

Description automatically generated with medium confidence

Output odd is high if state is FIRST or THIRD.   
Output even is high if state is SECOND.  
Output terminal is high if in THIRD state is about to go to FIRST.

If pause is high when clk is high, current state will be held.

If restart is high when clk is high, the next state will always be FIRST. This also takes priority over the pause input.

If restart and pause inputs are low, states will go in sequence: FIRST, SECOND, THIRD, and back to FIRST.

A picture containing text, diagram, plan, drawing

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1. System Verilog

`default\_nettype none

module fsm (

  output logic [4:0] state,

  output logic odd,

  output logic even,

  output logic terminal,

  output logic [2:0] Out1,

  output logic [2:0] Out2,

  input pause,

  input restart,

  input clk,

  input rst,

  input goto\_third

);

  localparam [2:0] FIRST  = 3'b001\_00;

  localparam [2:0] SECOND = 3'b010\_01;

  localparam [2:0] THIRD  = 3'b011\_00;

  localparam [2:0] Fourth = 3'b100\_01;

  localparam [2:0] Fifth  = 3'b101\_10;

  always\_ff @(posedge clk or posedge rst) // sequential

    begin

      if (rst) state <= FIRST;

      else

      begin

        case (state)

          FIRST:    if (restart | pause) state <= FIRST;

                    else state <= SECOND;

          SECOND:   if (restart) state <= FIRST;

                    else if (pause) state <= SECOND;

                    else state <= THIRD;

          THIRD:    if (restart) state <= FIRST;

                    else if (pause) state <= Fourth;

                    else state <= Fourth;

          Fourth:   if (restart) state <= FIRST;

                    else if (pause) state <= Fourth;

                    else state <= Fifth;

          Fifth:    if (goto\_third) state <= THIRD;

                    else if (restart) state <= FIRST;

                    else if (pause) state <= Fifth;

                    else state <= FIRST;

          default:  state <= FIRST;

        endcase

      end

    end

  assign even = state[0];

  assign odd = ~state[0];

  assign terminal = state[1];

  always\_comb

    case (state)

      FIRST:    {Out1, Out2} = {3'd3, 3'd2};

      SECOND:   {Out1, Out2} = {3'd5, 3'd4};

      THIRD:    {Out1, Out2} = {3'd2, 3'd7};

      Fourth:   {Out1, Out2} = {3'd6, 3'd3};

      Fifth:    {Out1, Out2} = {3'd5, 3'd2};

      default:  {Out1, Out2} = {3'd3, 3'd2};

    endcase

endmodule

`default\_nettype wire

1. A picture containing text, diagram, sketch, drawing

   Description automatically generated