# Asynchronous Audio Sample Rate Converter

IIEEC - Presentation

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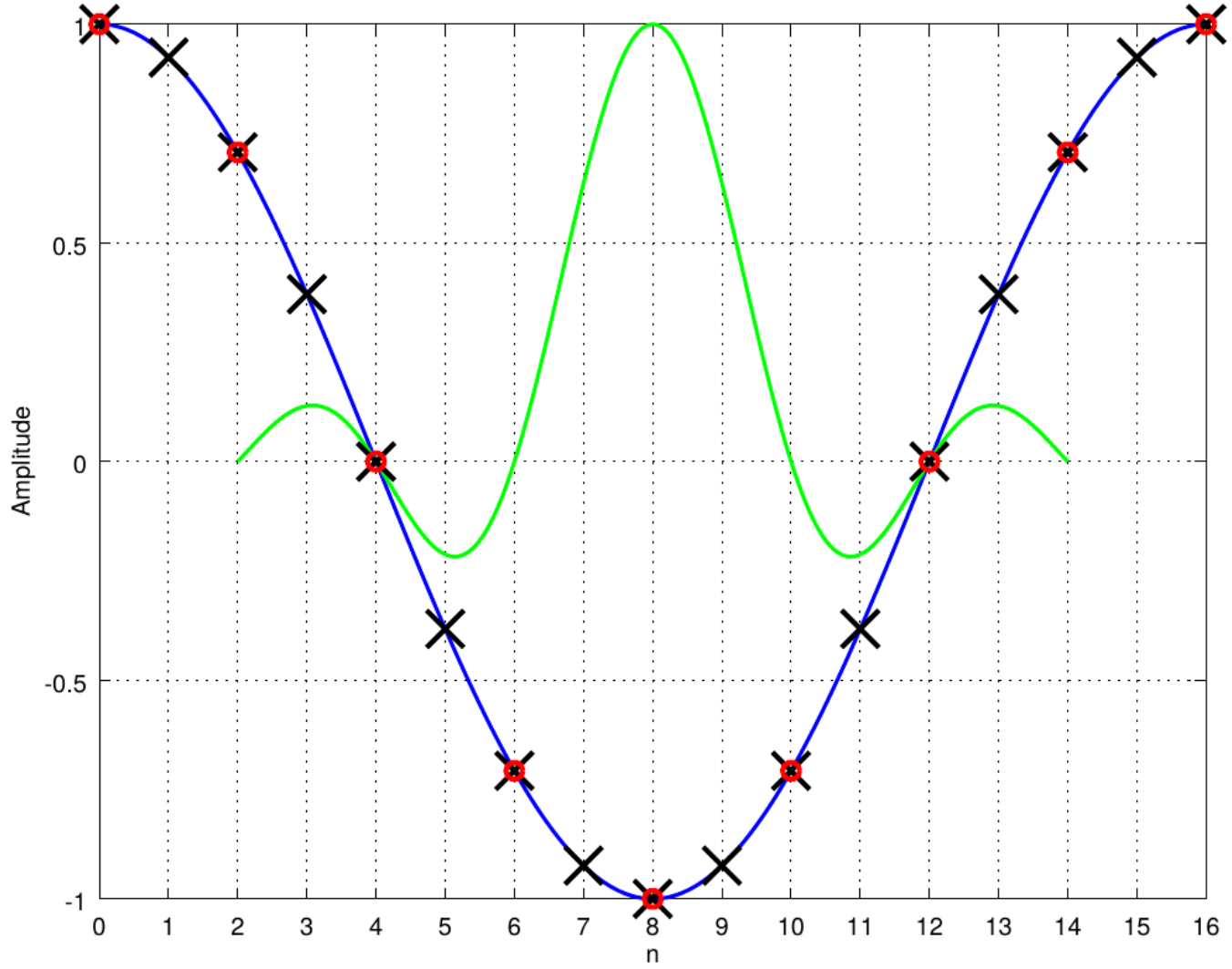
# What Is A Sample Rate Converter?



# Sample Rate Converter Applications

- Film and television
  - Most movies are shot at 24 frames per second
  - Most televisions run at 50 (PAL) or 60 (NTSC) frames per second

- Audio
  - Conversion from Compact Disc (44.1 kHz) to Digital Audio Tape (48 kHz)
  - Mixing consoles
  - Audio workstations
  - Audio broadcast equipment

# Some Sample Rate Converters

**AD1896 (IC)**

- 2 channel input
- 7.75:1 to 1:8 conversion ratio
- Worst THD+N: -117 dB

**SRC4194 (IC)**

- 4 channel input
- 16:1 to 1:16 conversion ratio
- Worst THD+N: -137 dB

**CWda52 (IP)**

- 8 channel input
- 7:1 to 1:7 conversion ratio
- Worst THD+N: -118 dB

# Motivation

- Few IP implementations, with limited specifications.
- No cheaper access to sample rate converters.
- Growth of the market leads to the need of better IP cores.

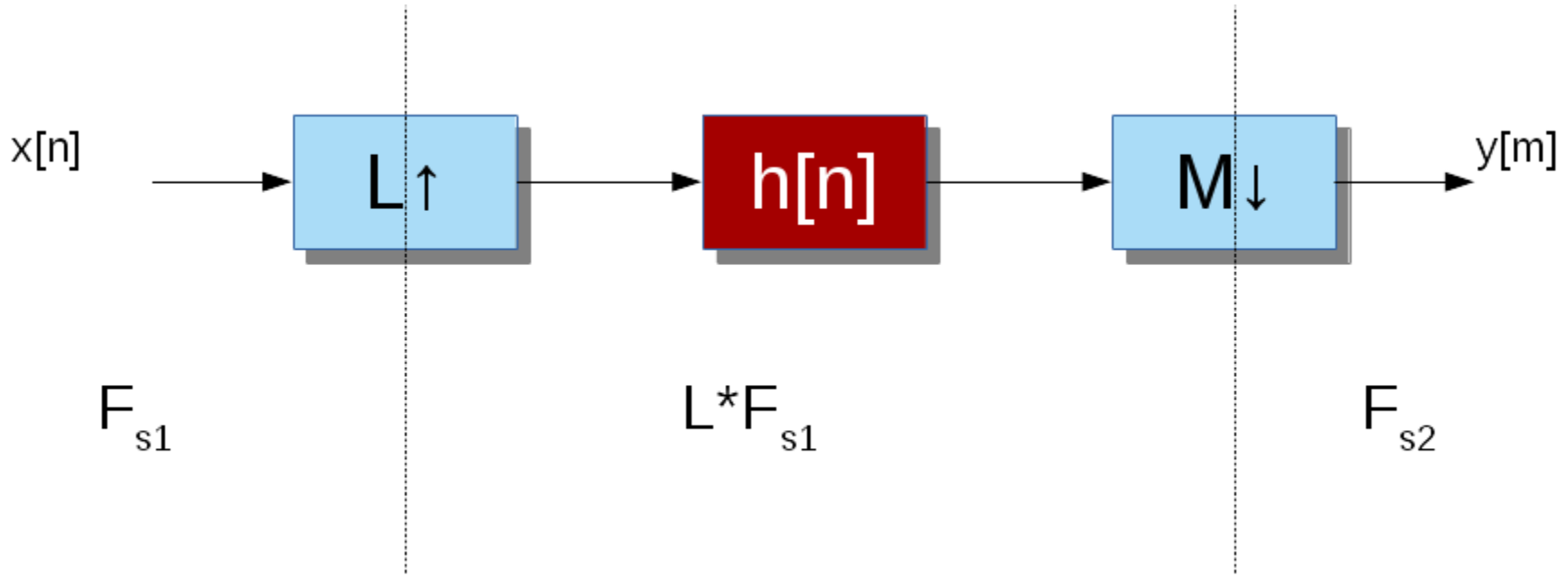
# Objectives

- Design an asynchronous sample rate converter IP core, using Verilog.
- Specifications should be competitive to IC counterparts.
- Core should be implemented in a system-on-chip.

# Proposed Specifications

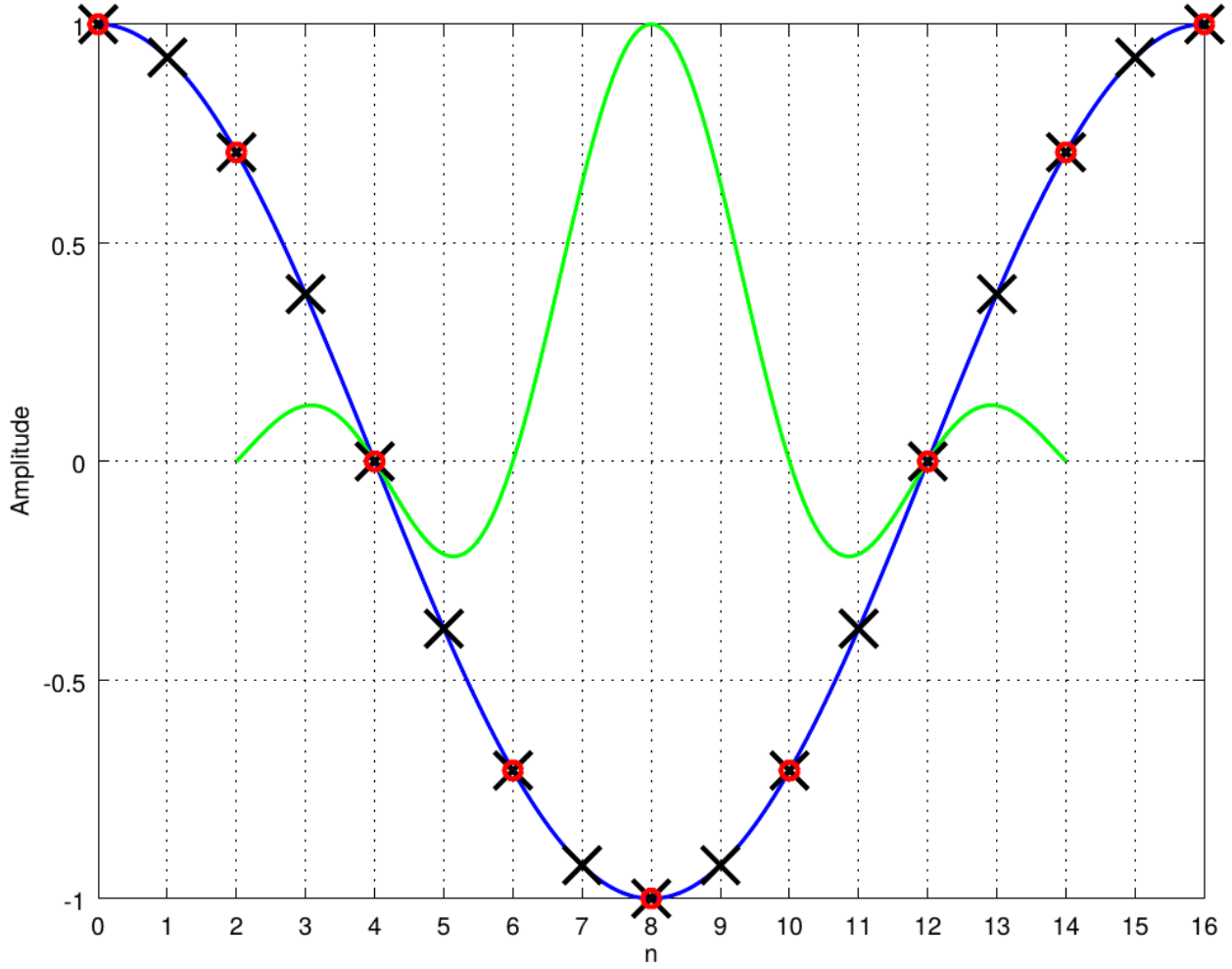
- Up to 24 bit samples
- Support to signals sampled from 8 kHz to 192 kHz
- 24:1 to 1:24 conversion ratio
- Worst THD+N: -130 dB
- Multi-channel support

# Sample Rate Converter Structure

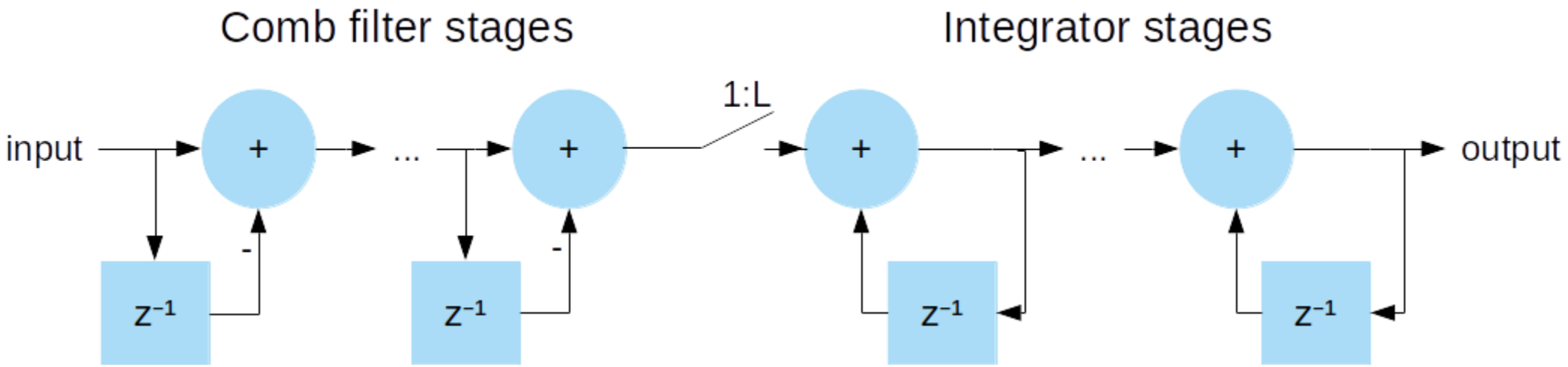


# Low Pass Filter – Digital Case

- $\left|H_d\left(e^{j\Omega}\right)\right| = \begin{cases} 1, |\Omega| < \Omega_c \\ 0, otherwise \end{cases}$
- $\Omega_c = \min\left(\frac{\pi}{2L}, \frac{\pi}{2M}\right)[rad]$
- $h_d[n] = \frac{\Omega_c}{\pi} sinc\left[\frac{\Omega_c}{\pi}(n - \tau_d)\right]$
- Normalization:
  - $\Omega = \frac{2\pi f}{L\, f_{s1}}\ [rad]$

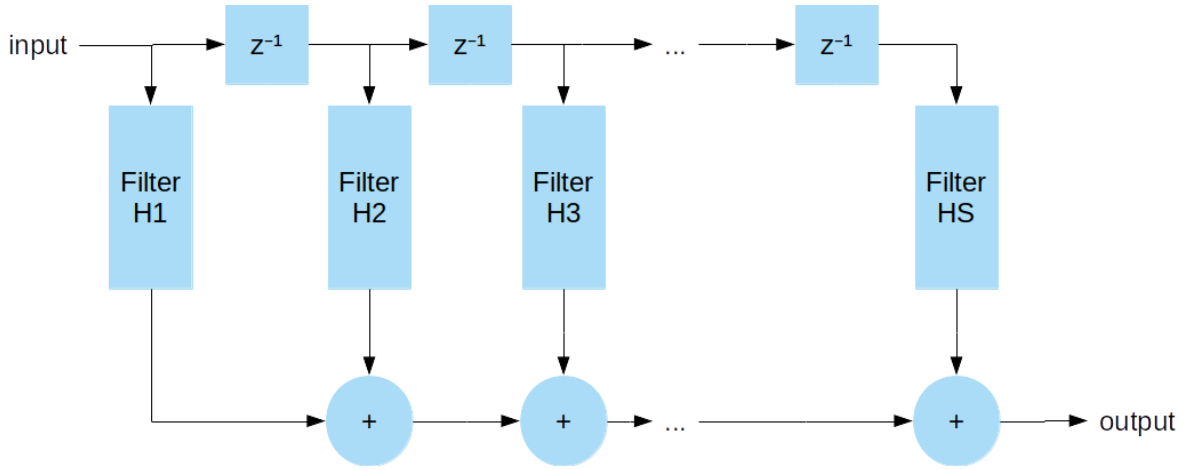


# Cascaded Integrator Comb Filters



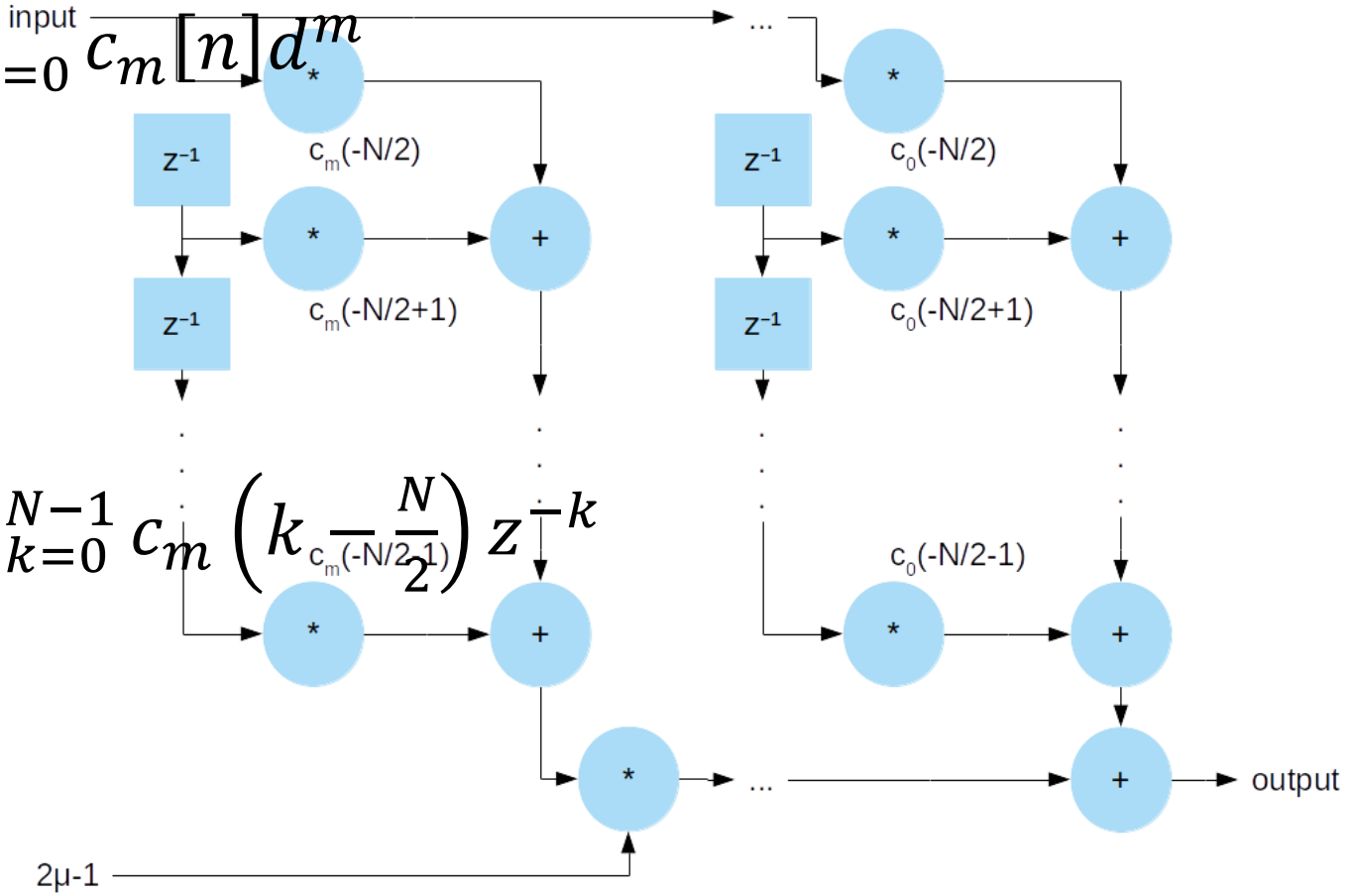
# Approximation By Piecewise Quadratic Function

- $h(t) = \begin{cases} a_{1,1}t^2 + b_{1,1}t + c_{1,1}, & 0 \le |t| \le \frac{1}{N} \\ \dots \\ a_{1,n}t^2 + b_{1,n}t + c_{1,n}, & \frac{n-1}{N} \le |t| \le 1 \\ \dots \\ a_{s,n}t^2 + b_{s,n}t + c_{s,n}, & s-1+\frac{n-1}{N} \le |t| \le s-1+\frac{n}{N} \\ \dots \\ a_{S,n}t^2 + b_{S,n}t + c_{S,n}, & S-1+\frac{n-1}{N} \le |t| \le S \end{cases}$

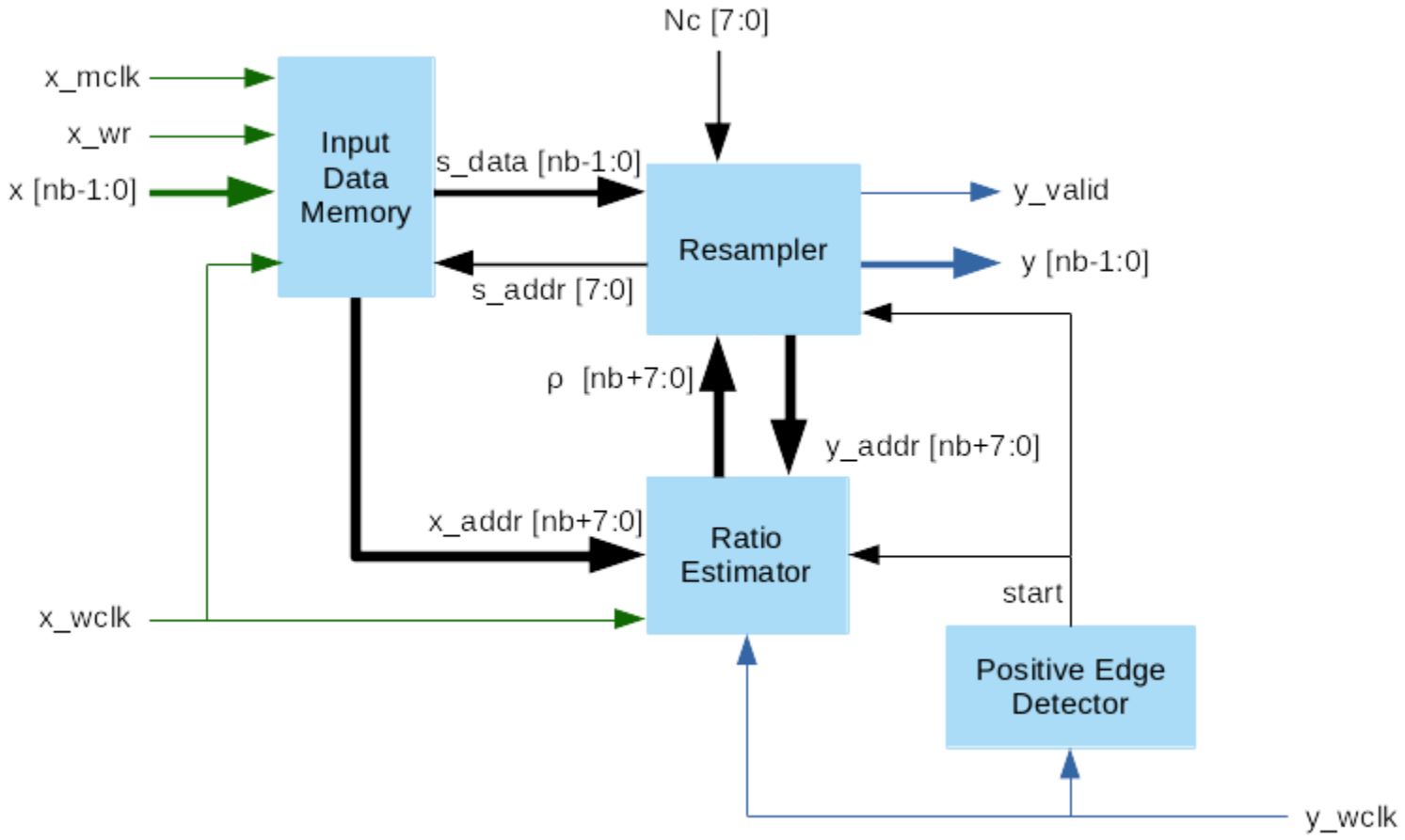


# Farrow Structure

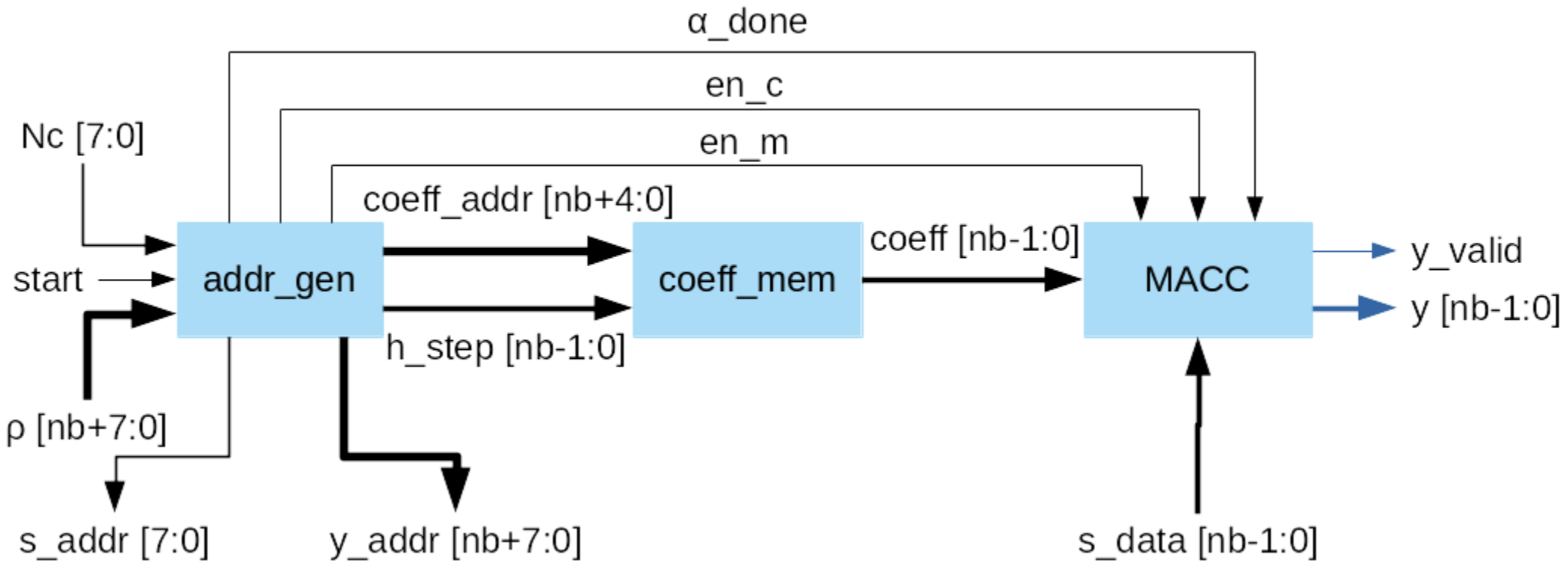
- $h[n] = \sum_{m=0}^{q} c_m[n] d^m$
- $\mu = \frac{k}{M}$
- $C_m(z) = \sum_{k=0}^{N-1} c_m\left(k - \frac{N}{2}\right) z^{-k}$



# Proposed Design – Top Module



# Proposed Design – Resampler



# Simulation

- Coefficients and input signal generated using Octave
- Simulated using NCSim

- Output analyzed using Octave:
  - Total harmonic distortion plus noise ratio measured
  - Fast Fourier Transform used
  - Small tolerance around the test frequency is considered signal, rest is considered distortion and noise

# Simulation – Preliminary Results

| Conversion Ratio | THD+N |
|---|---|
| 44.1 kHz : 48 kHz | -131,94 dB |
| 48 kHz : 44.1 kHz | -53,45 dB |
| 48 kHz : 96 kHz | -140,44 dB |
| 44.1 kHz : 192 kHz | -131.82 dB |
| 96 kHz : 48 kHz | - 143.31 dB |
| 192 kHz : 32 kHz | -46.21 dB |

- Expected worst THD+N: -130 dB

# Implementation

- Interfaces attached to core: AXI-Lite, I2S/Parallel
- Implementation in System-on-Chip (using picoRV32)
- Ethernet or UART for PC to FPGA data transfers.

# Future Work

| Task | Schedule |
|---|---|
| Improve sample rate converter prototype | 17/02 – 15/03 |
| Implement ratio estimator | 16/03 – 12/04 |
| Insert pipelines and control units | 13/04 – 19/04 |
| Optimize resources usage | 20/04 – 03/05 |
| Design and implement interfaces | 04/05 – 10/05 |
| Test and debug core in FPGA | 11/05 – 31/05 |
| Write thesis report | 1/06 – 19/07 |

# Conclusions

- A prototype was already done but does not fulfill specifications.
- Optimization and bug fixing is essential to obtain high precision and low area consumption.
- There are alternate structures to the resampler. Farrow structure is the most common.