Compiler Technology for CGRAs

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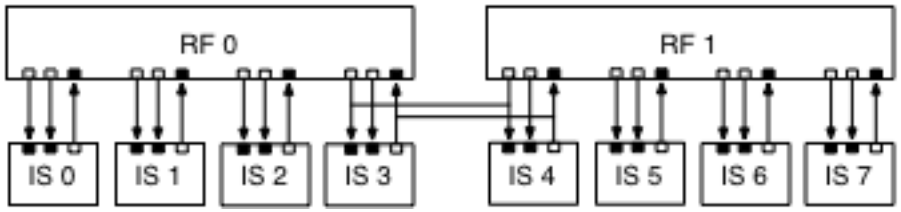
Ghent University

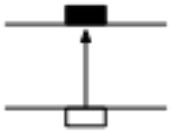
Overview

- What makes compilation for CGRAs different?
- What CGRA code generation techniques exist?
- What is not automated?

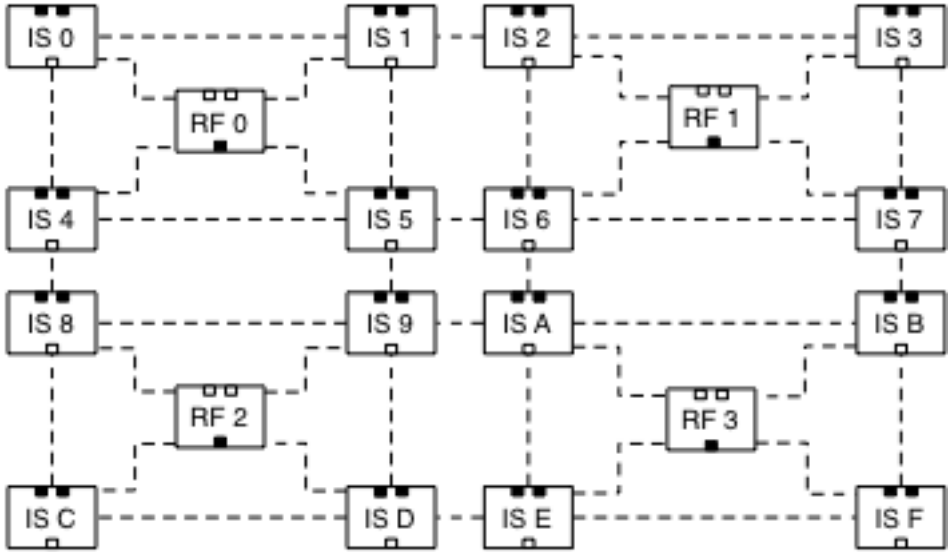
CGRA vs VLIW

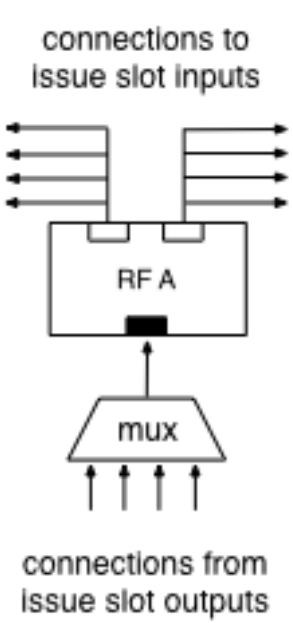
VLIW

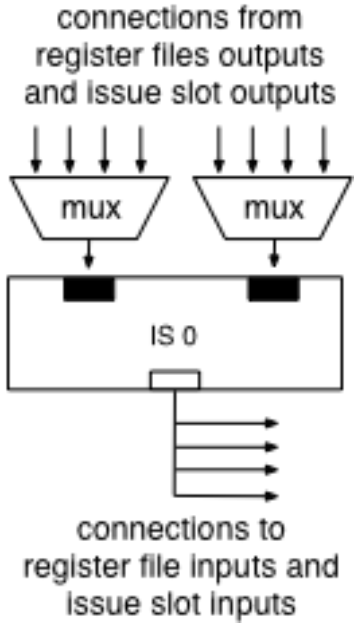




CGRA







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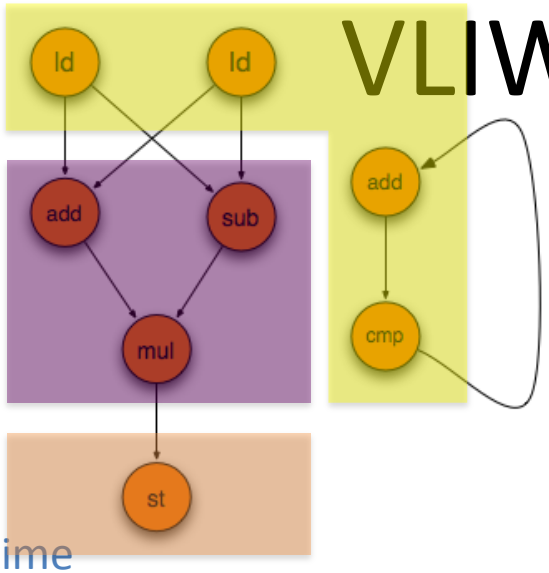
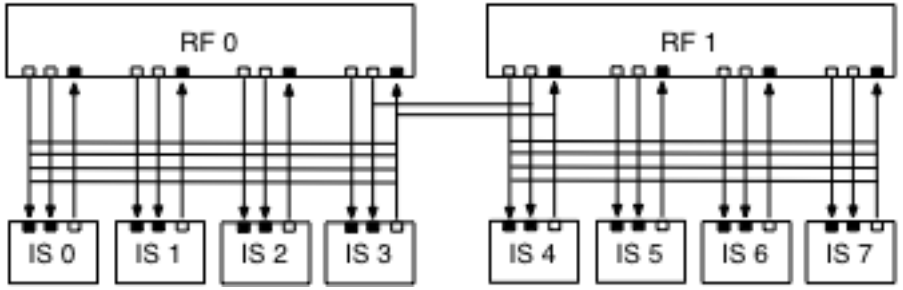
VLIW code scheduling





time

cycle 0

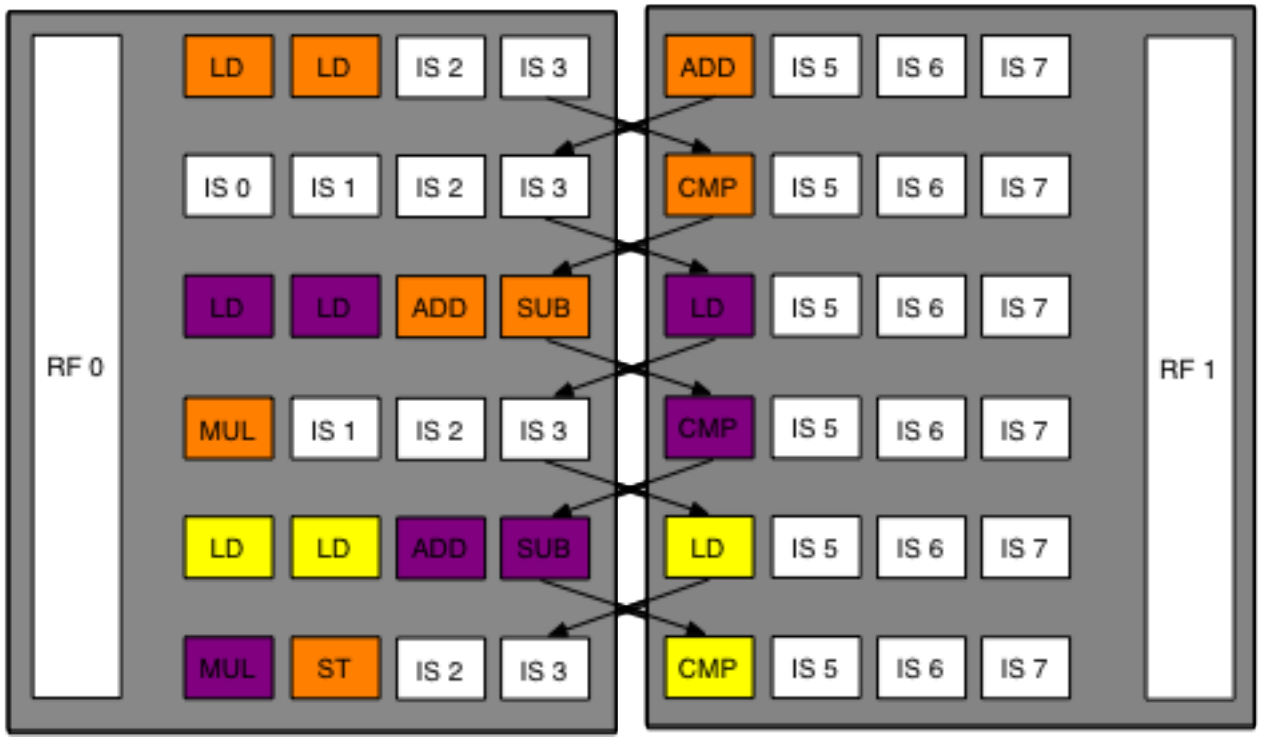
cycle 1

cycle 2

cycle 3

cycle 4

cycle 5



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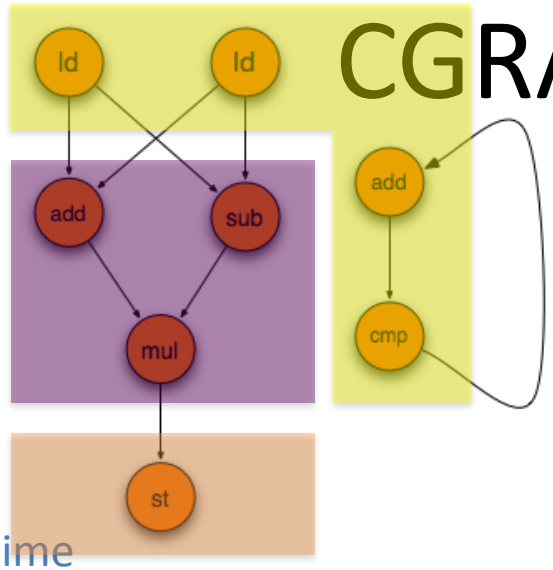
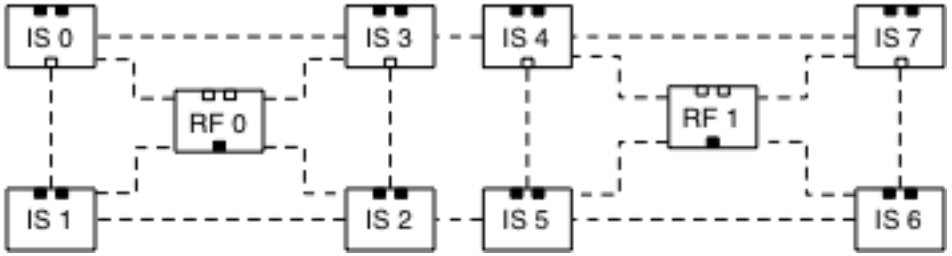
CGRA code scheduling





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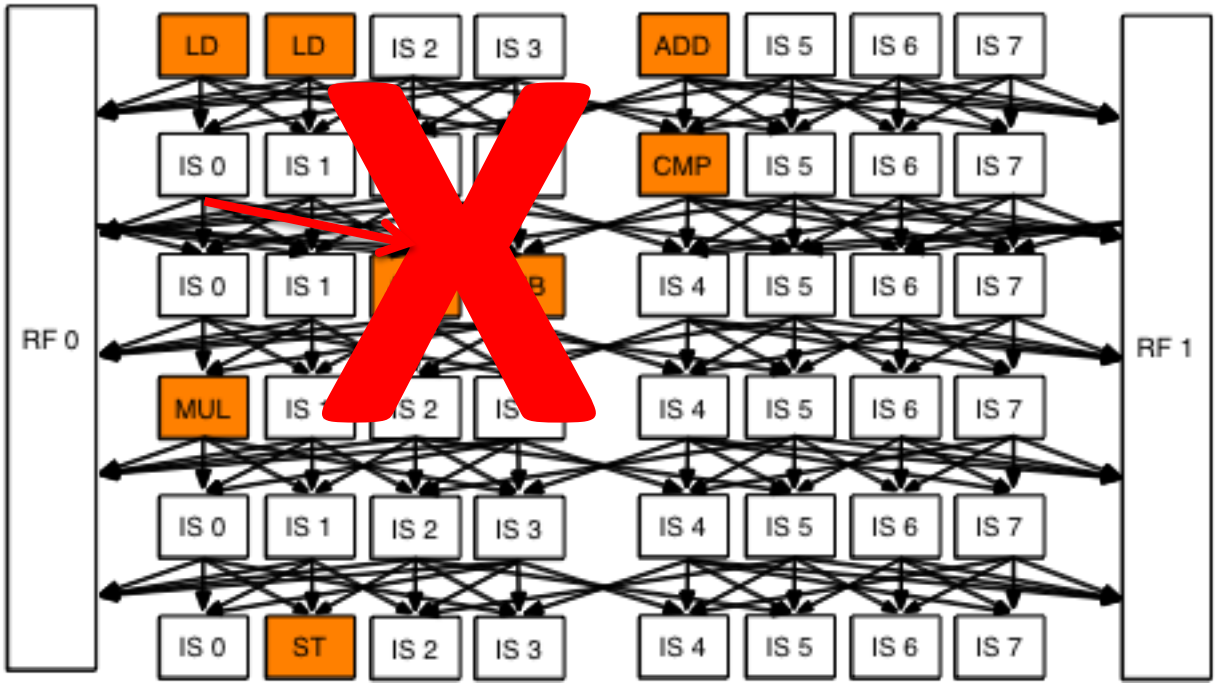

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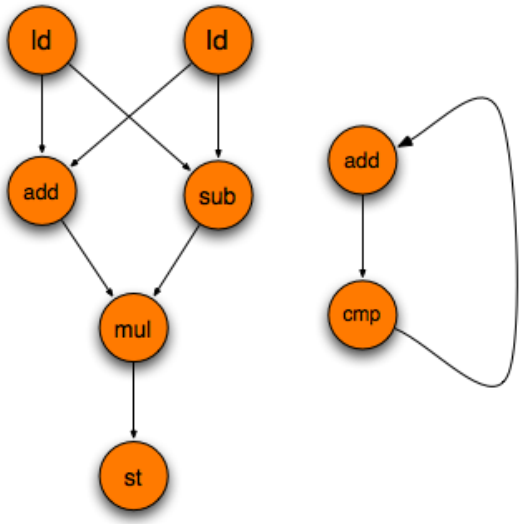
CGRA scheduling = graph mapping

data dependence graph

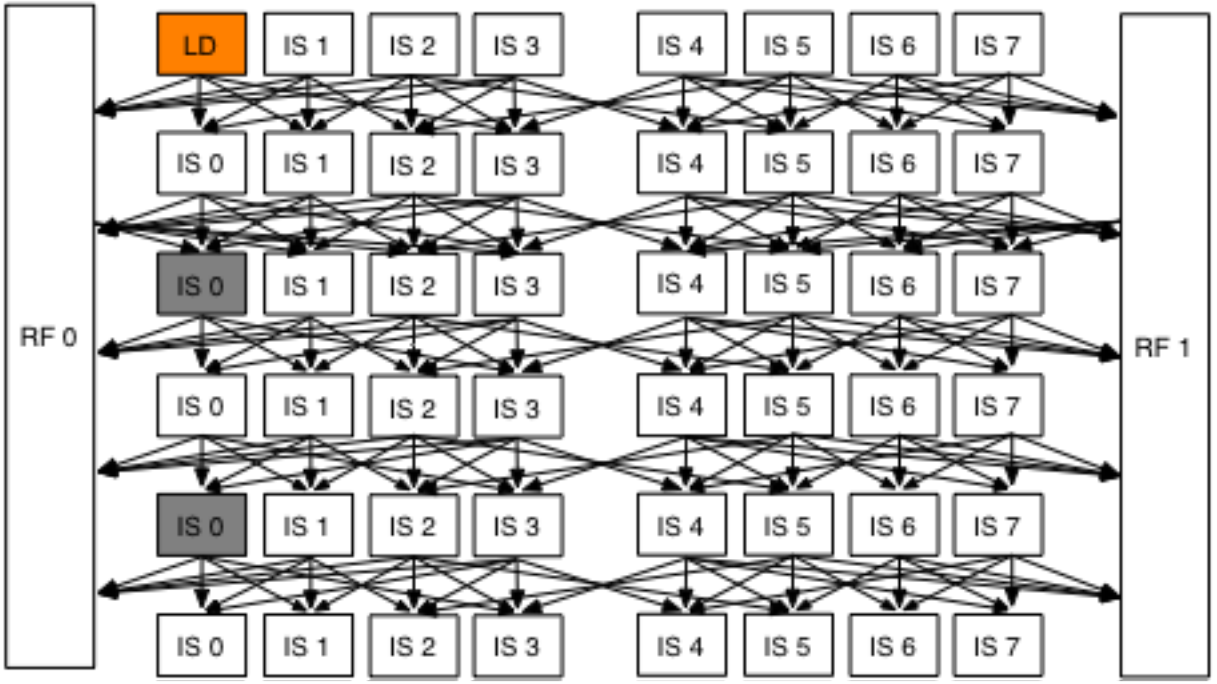
models code



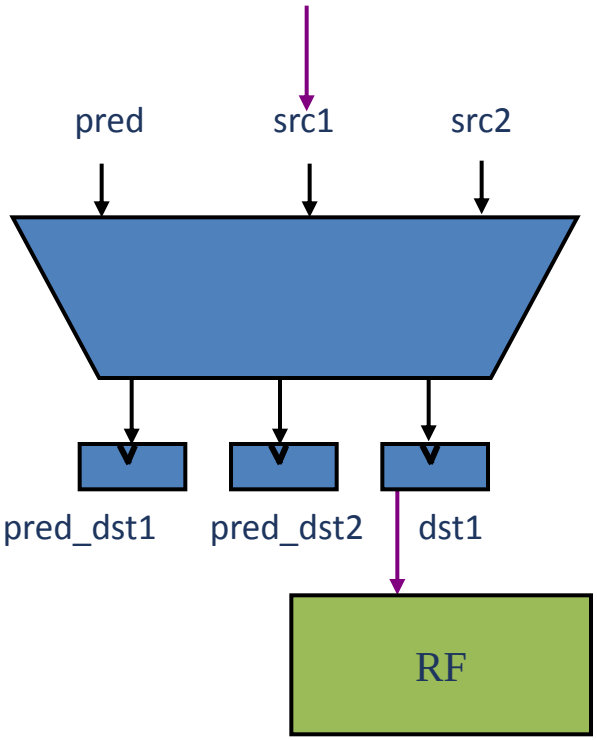
modulo routing resource graph

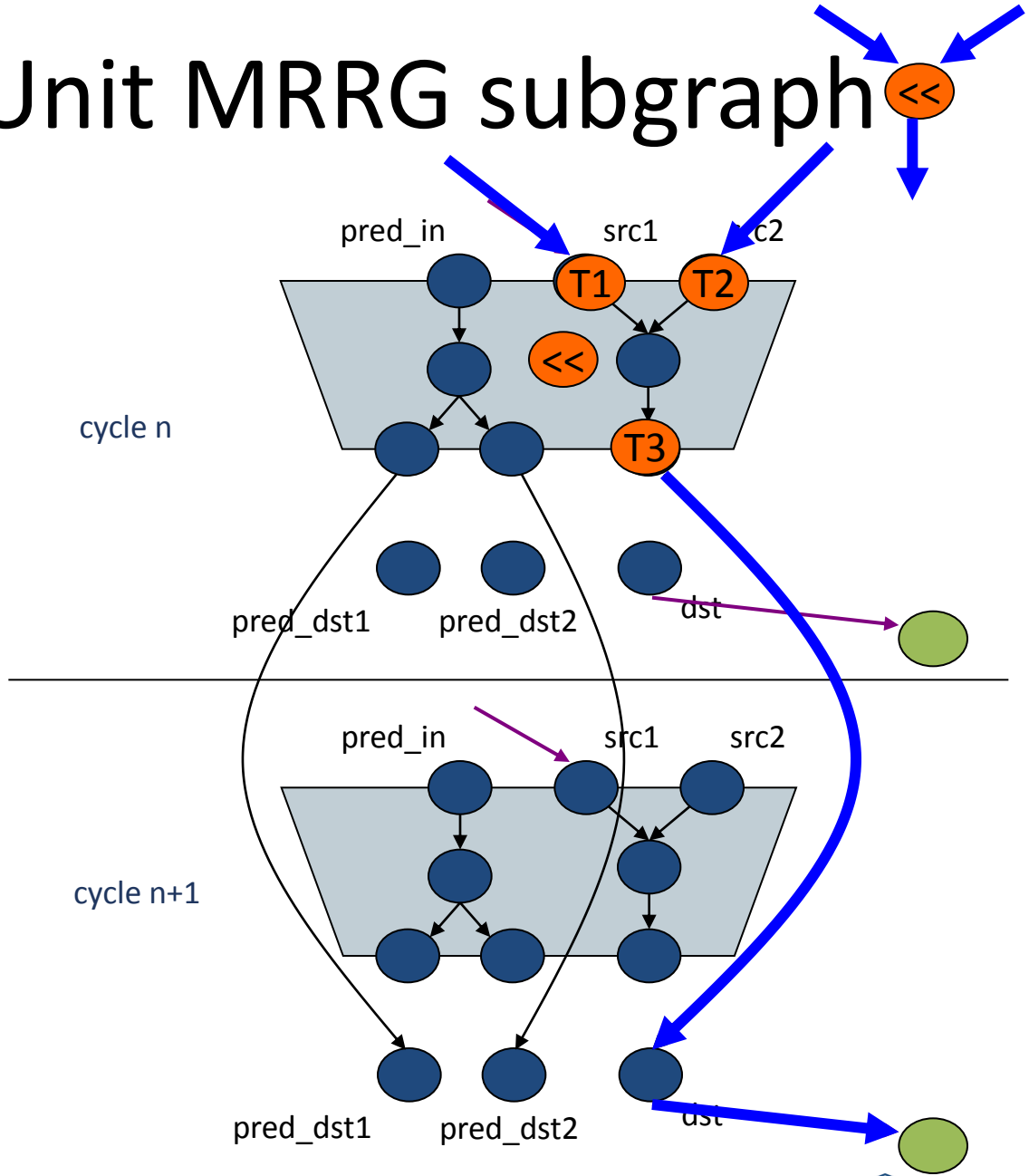
models the whole architecture

at some initiation interval



Functional Unit MRRG subgraph





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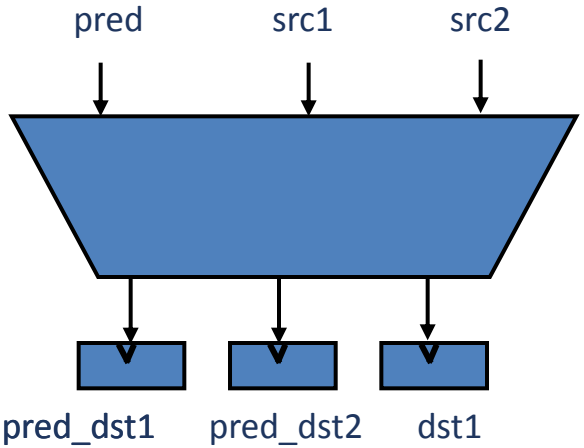

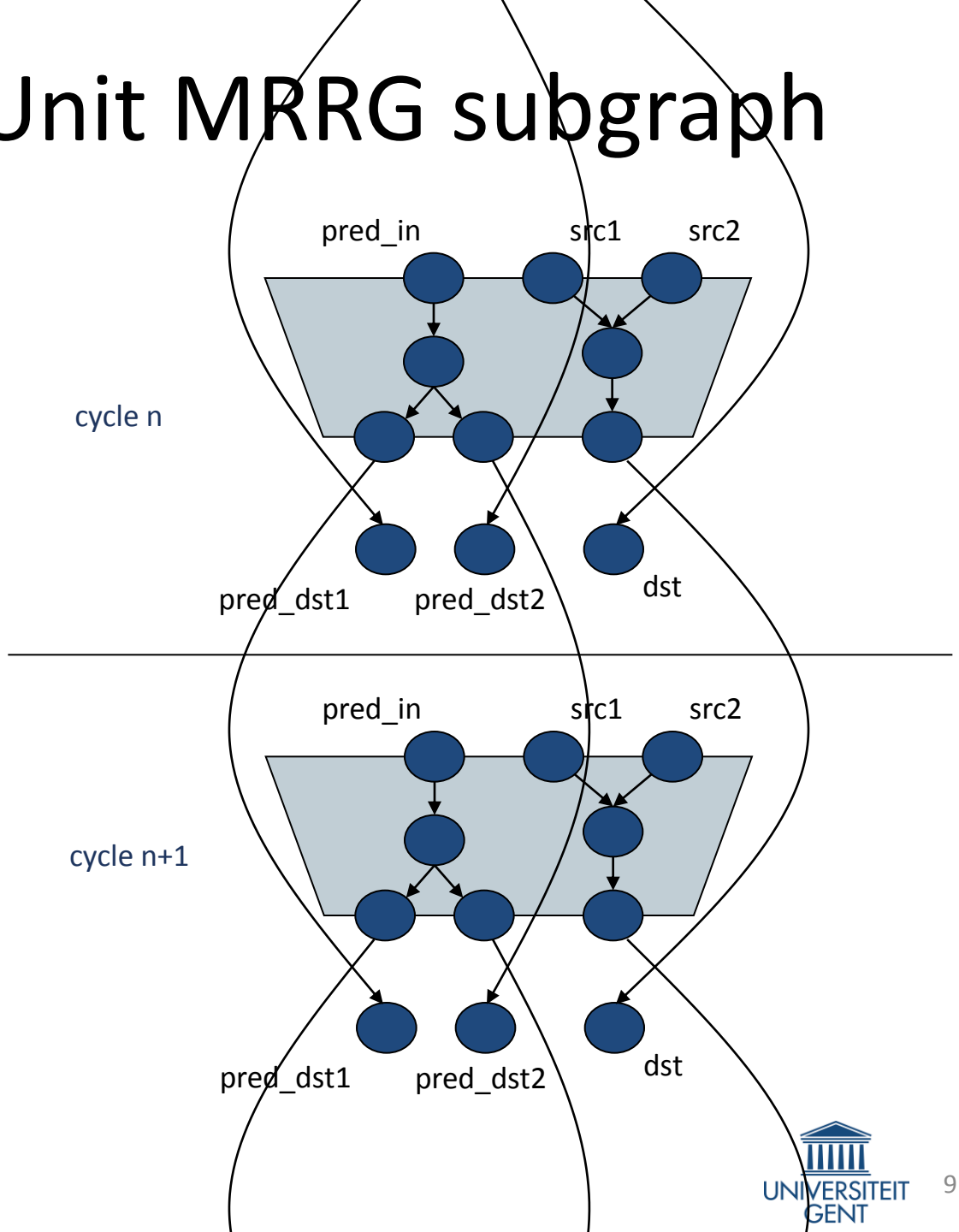

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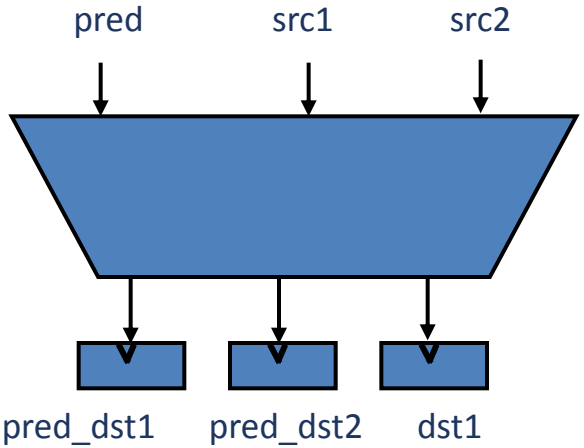
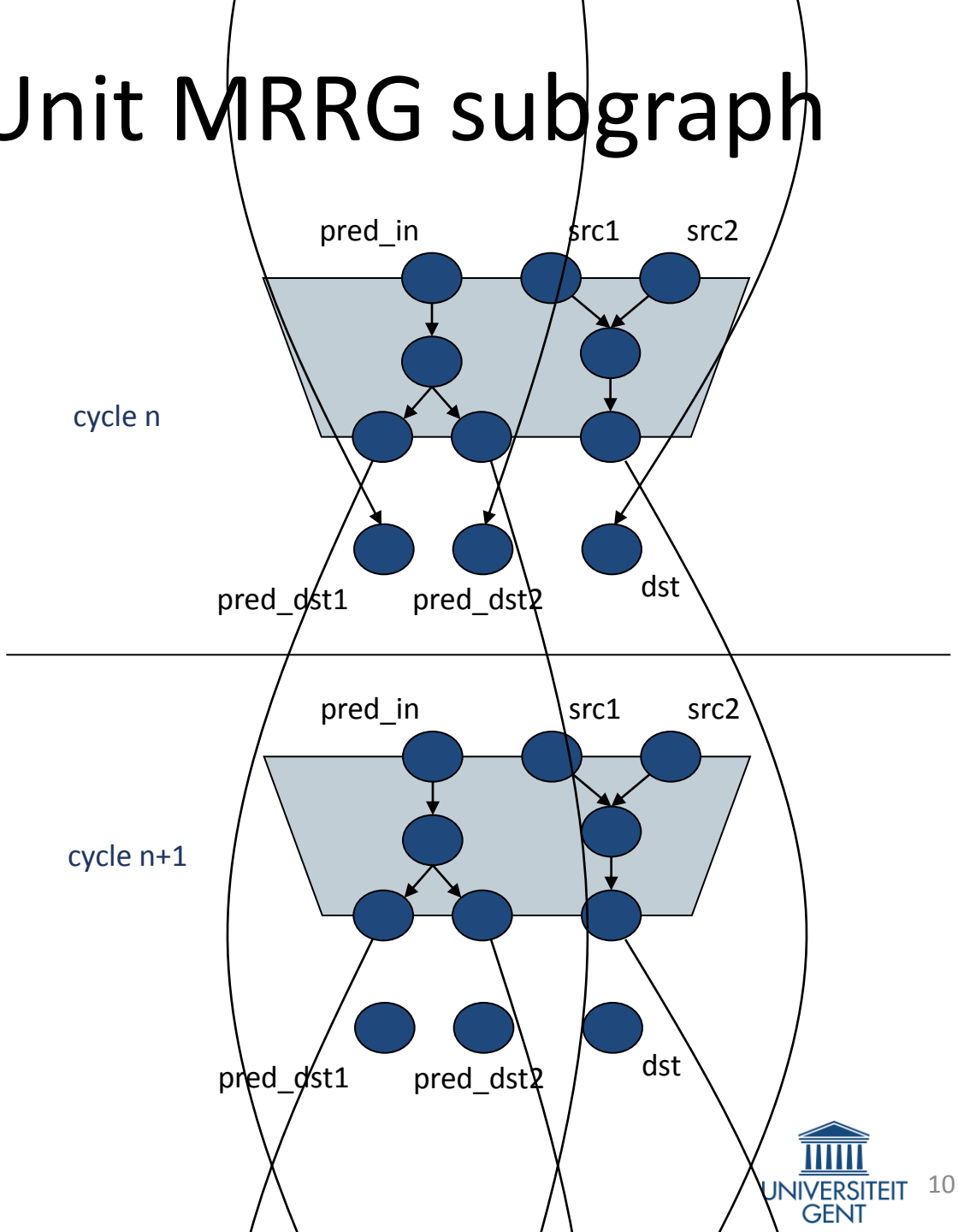
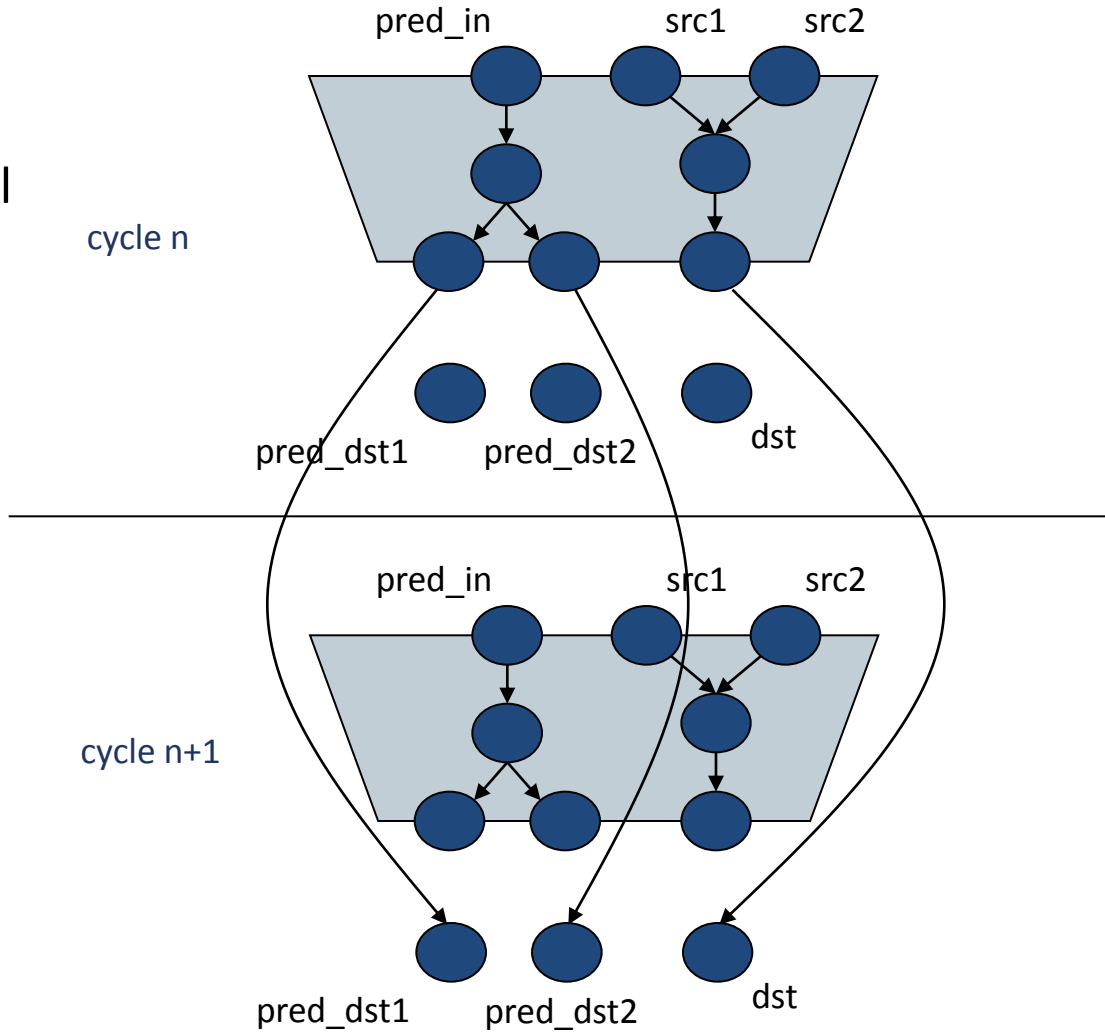




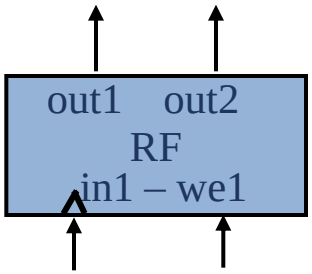
Functional Unit MRRG subgraph

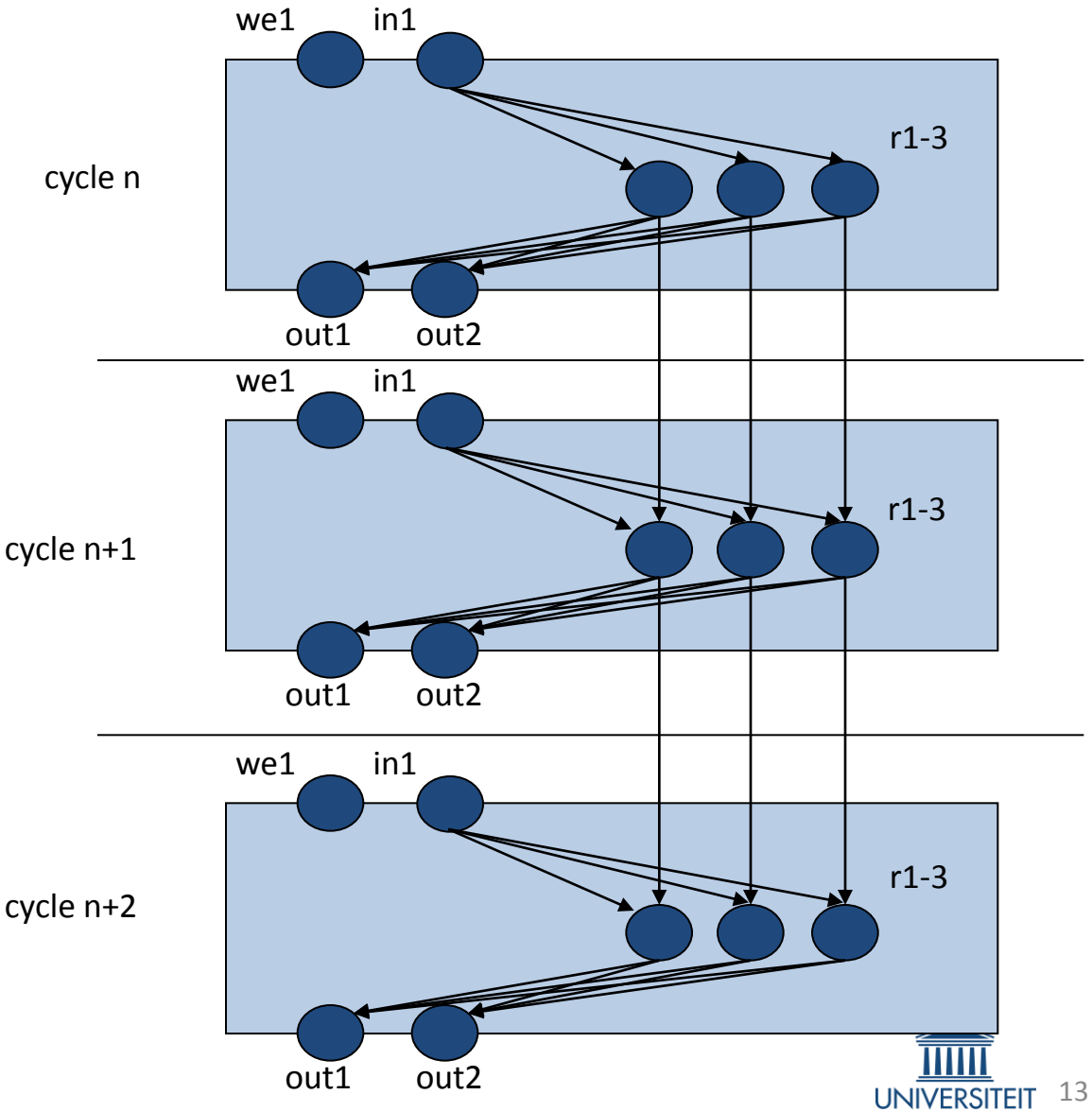
- appropriate connections model latency
- internal nodes and edges model data passing and additional routing freedom
- more src inputs are possible

- all variations use same basics
- adapting the subgraph implements differences
- without requiring changes to mapping algorithm itself
- **inherently retargetable**



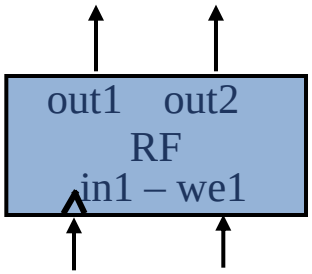
Register File MRRG subgraph

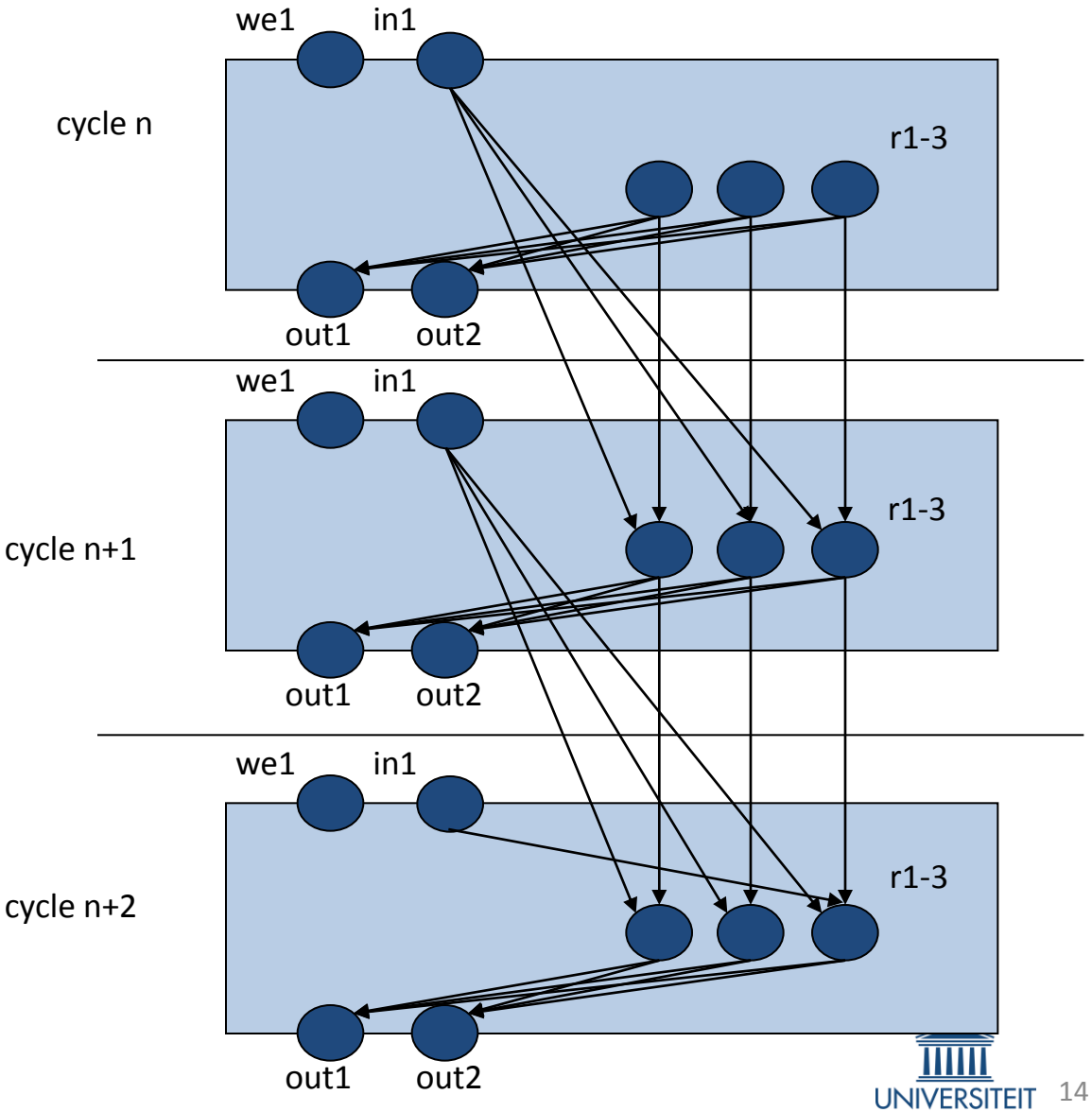




- model different delays:
  - delay 0 (forwarding)

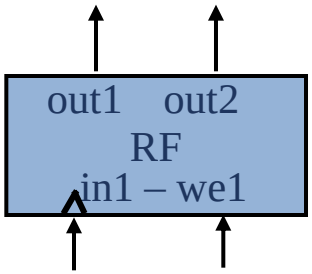
Register File MRRG subgraph

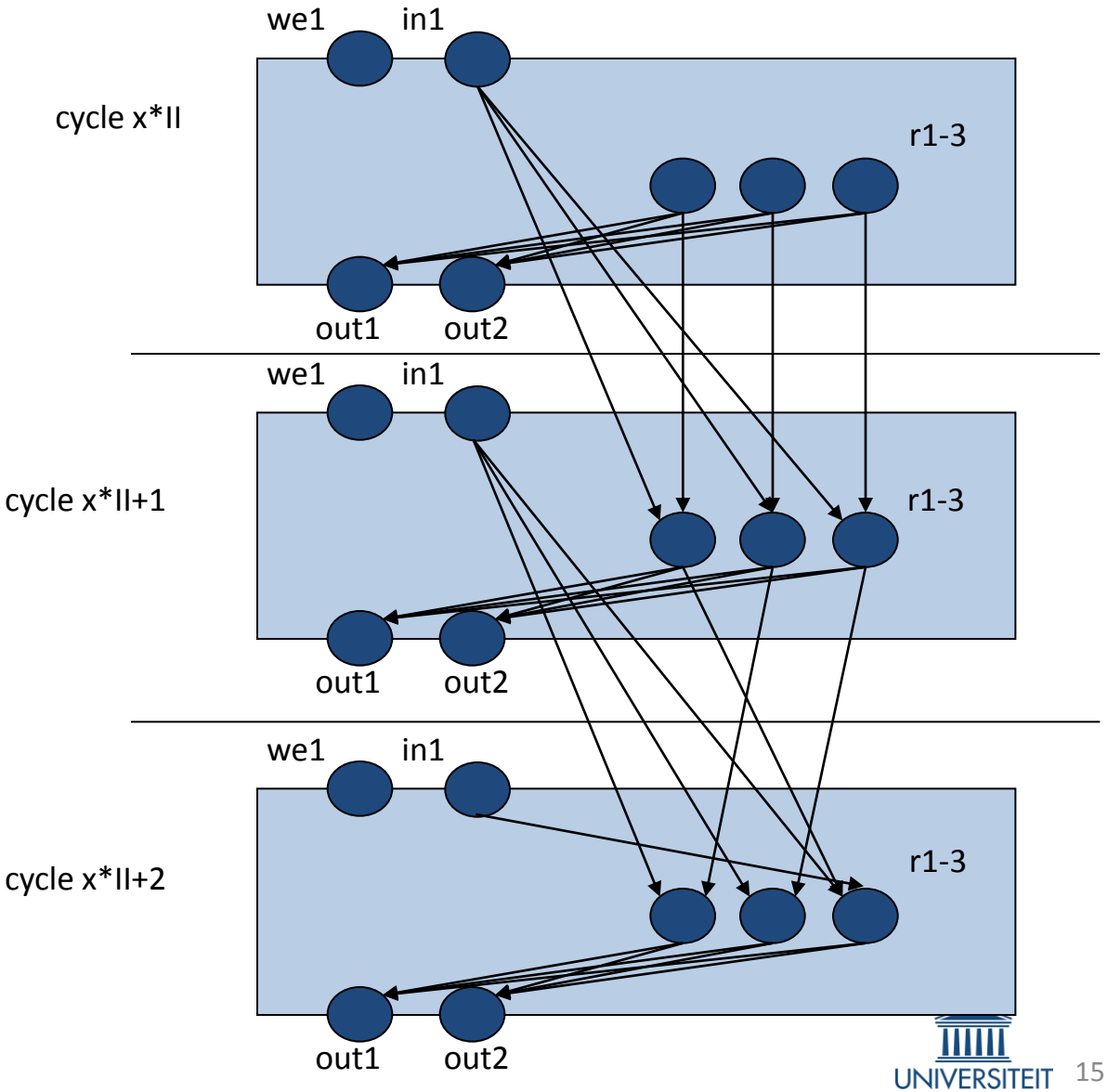




- model different delays:
  - delay 1
- model rotation
  - non-rotating

Register File MRRG subgraph

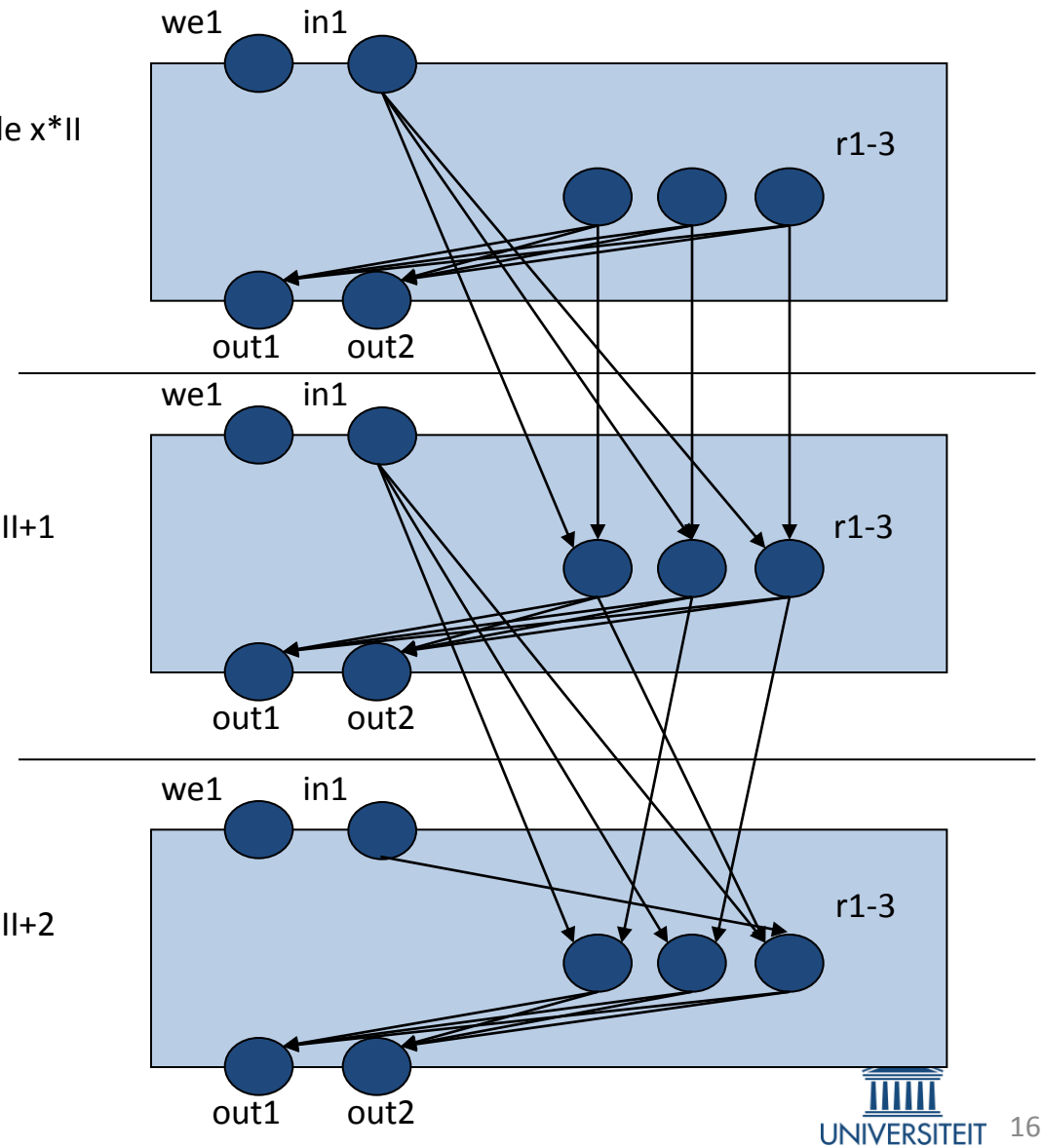




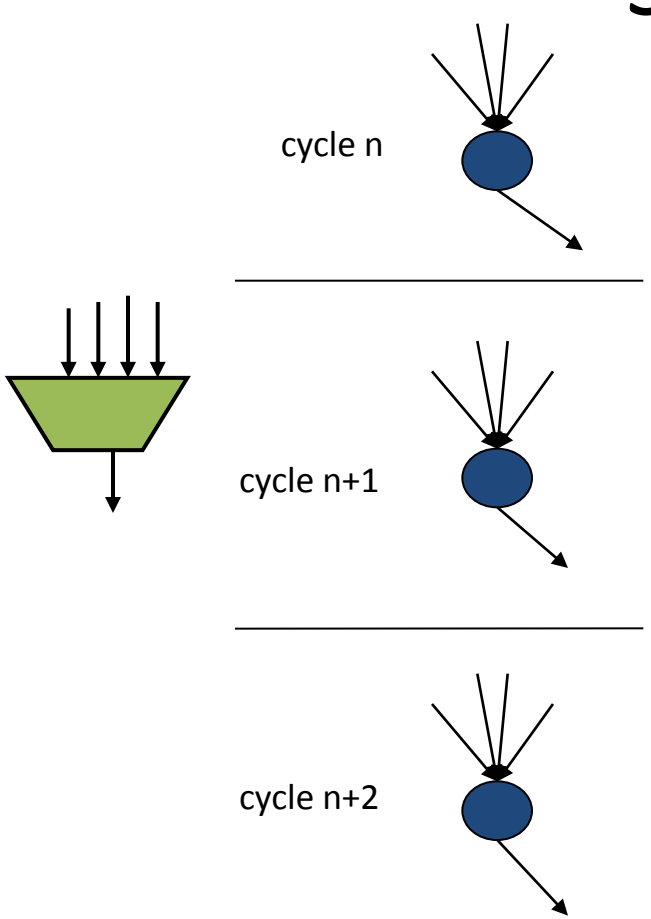
- model different delays:
  - delay 1
- model rotation
  - rotating

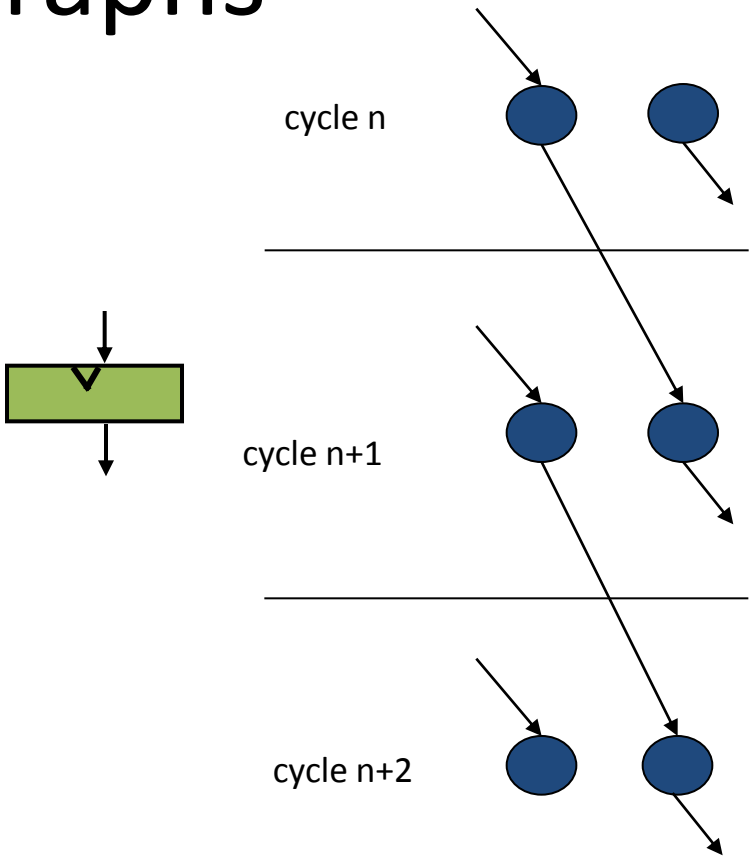
Register File MRRG subgraph

- appropriate connections model latency
- edges model non-rotating vs. rotating RFs
- no explicit register allocation performed
- when a dependency is mapped onto a net through a RF, the value is allocated in the corresponding register
- if not, the value is not allocated to a RF

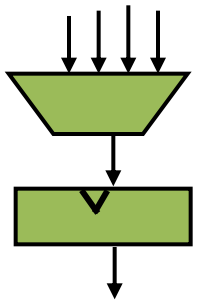


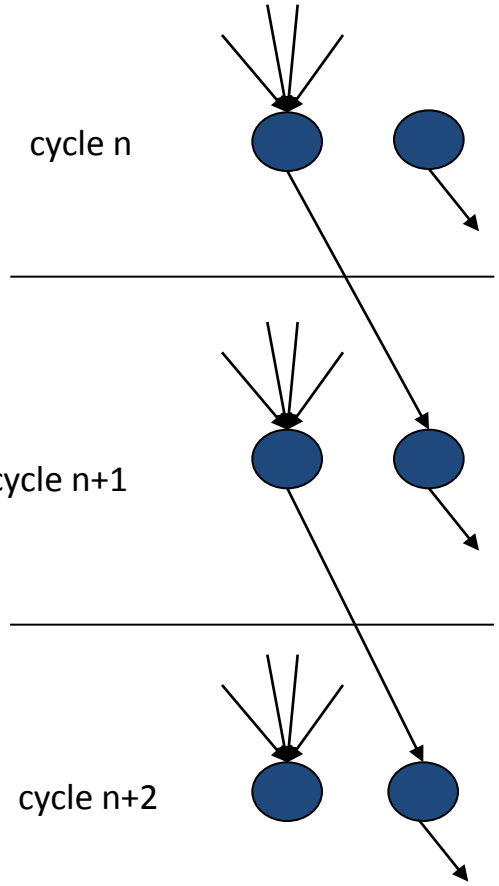
Muxes & pipelining register MRRG subgraphs

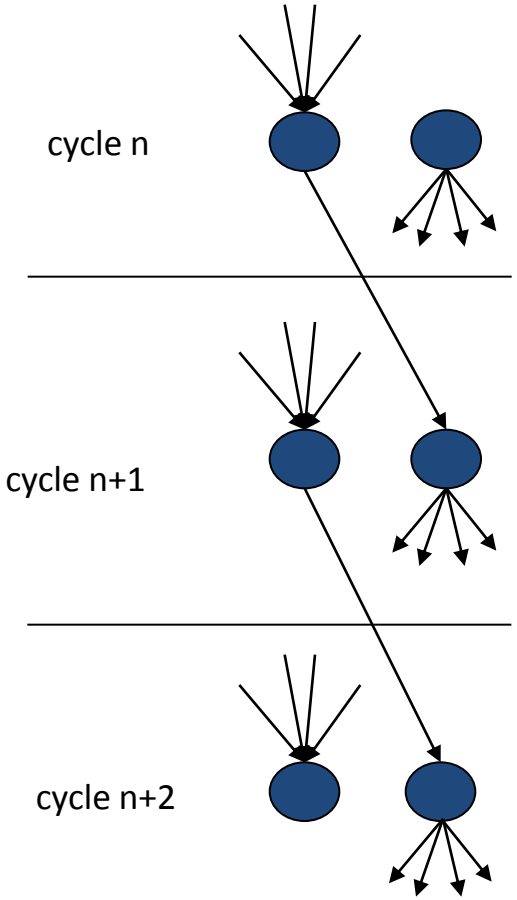




Delayed muxes & bus MRRG subgraphs







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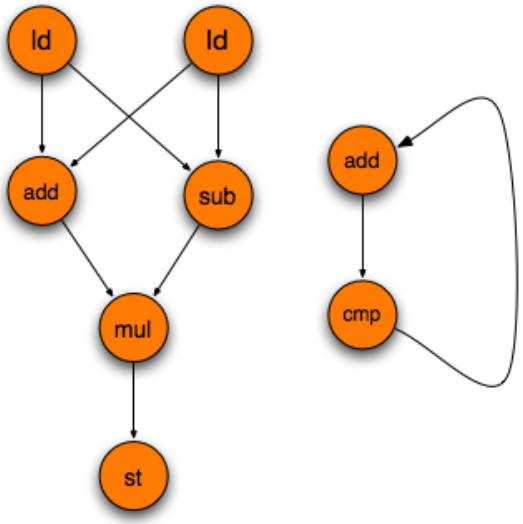
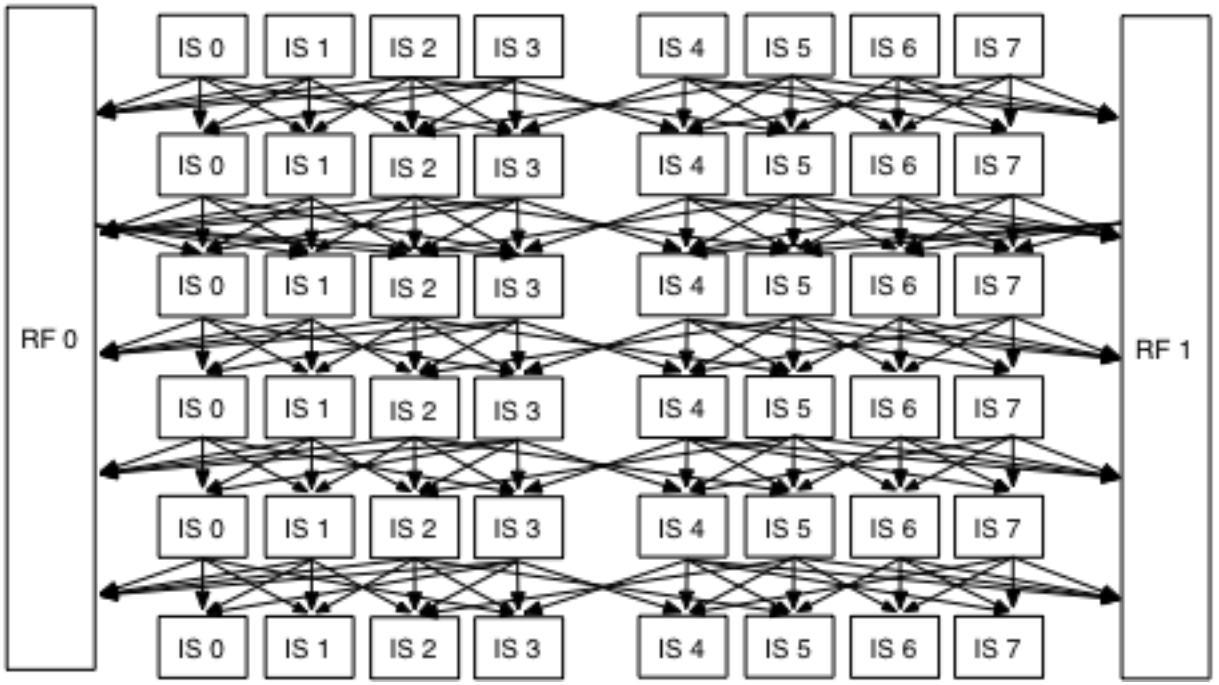


modulo routing resource graph

models the whole architecture

at some initiation interval

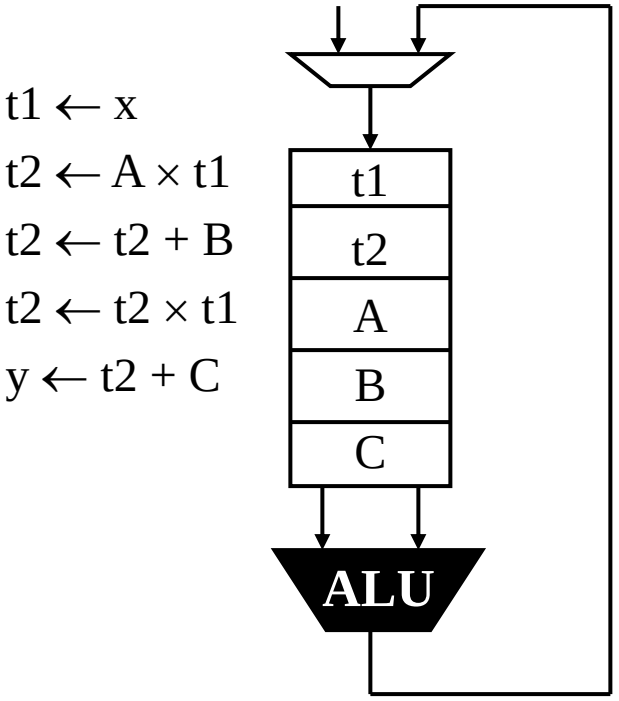


inherently retargetable

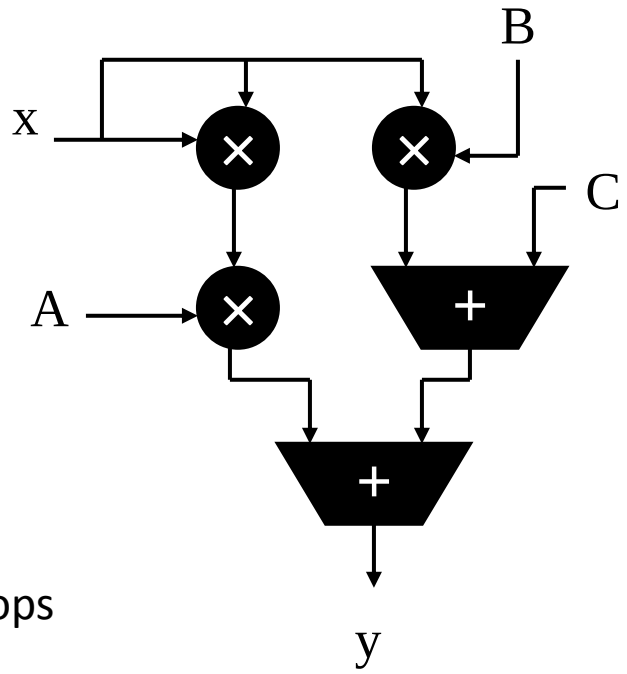
easily model heterogeneous architectures

Data dependence graph

sequential C code



parallel data dependence graph



- if-conversion
- predication
- predicate speculation
- hyperblock formation
- inspector-executor loops

- but limited
  - single loop exit
  - not too many predicates

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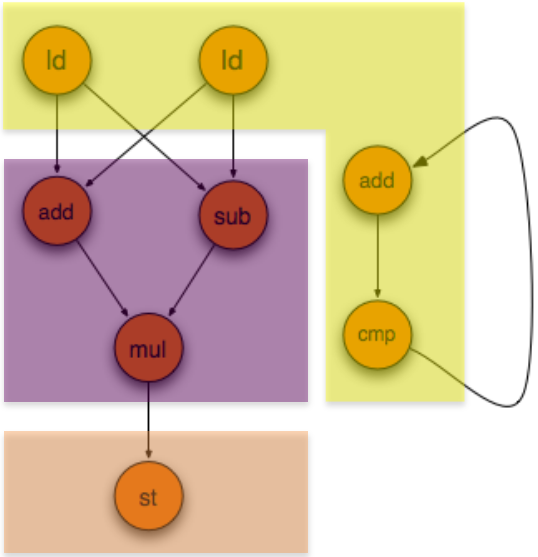

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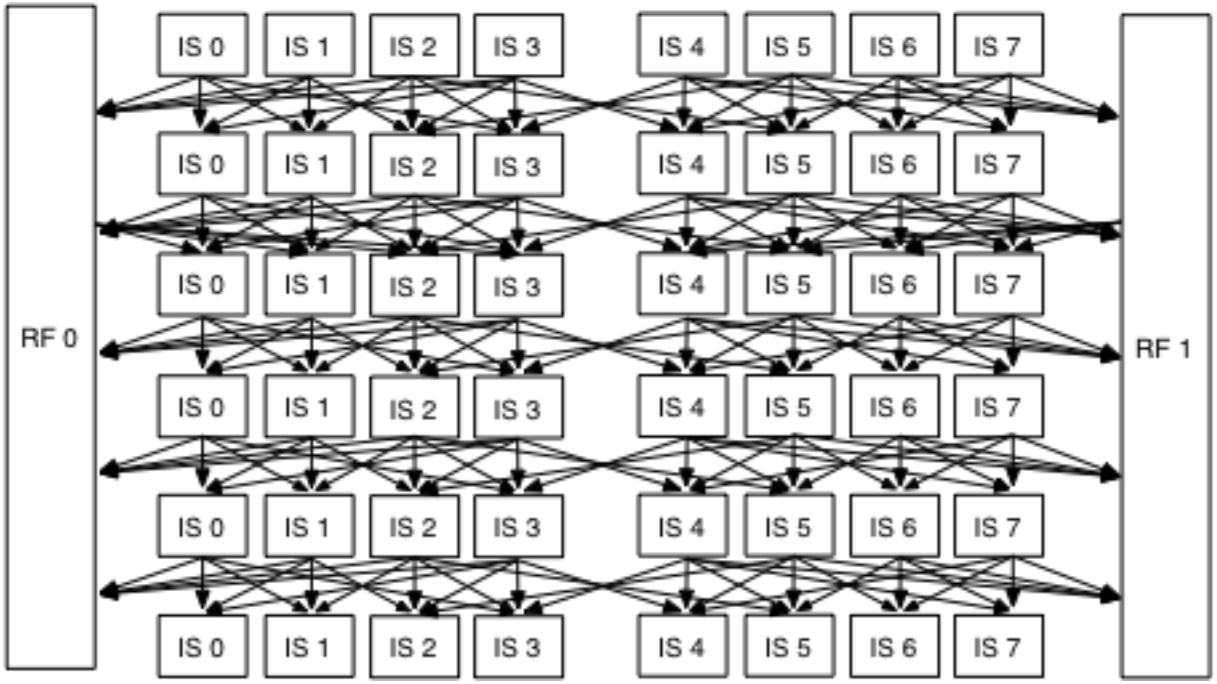
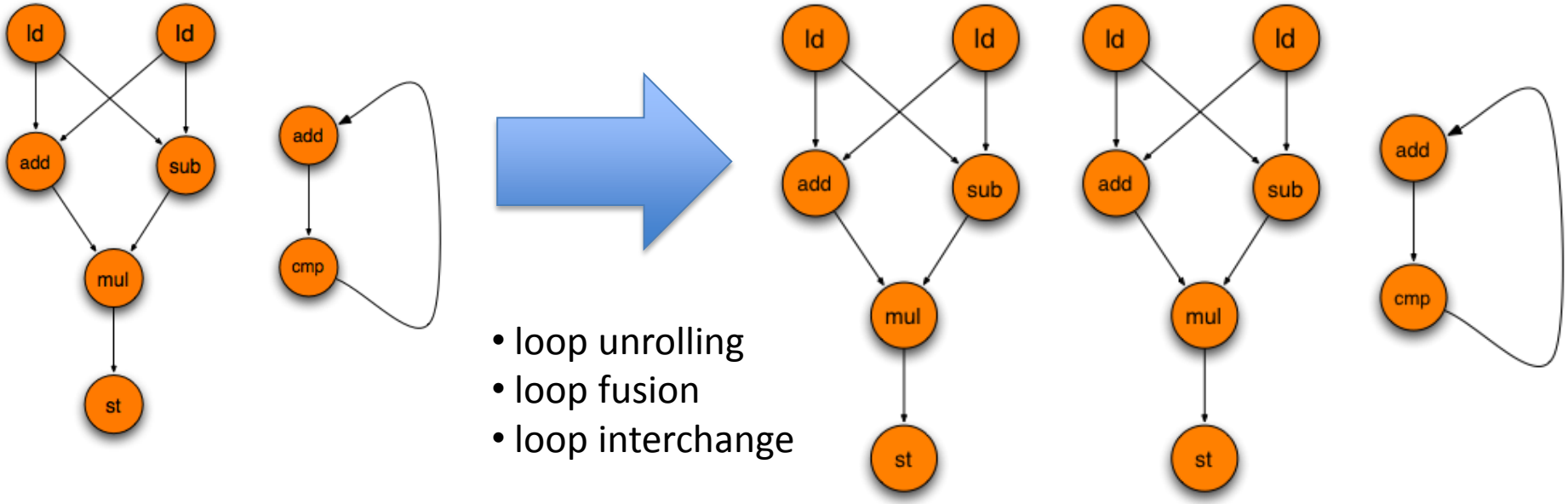


minimal initiation interval depends on
- length of recurrence cycle: 2
- number of resources: 8/8 = 1

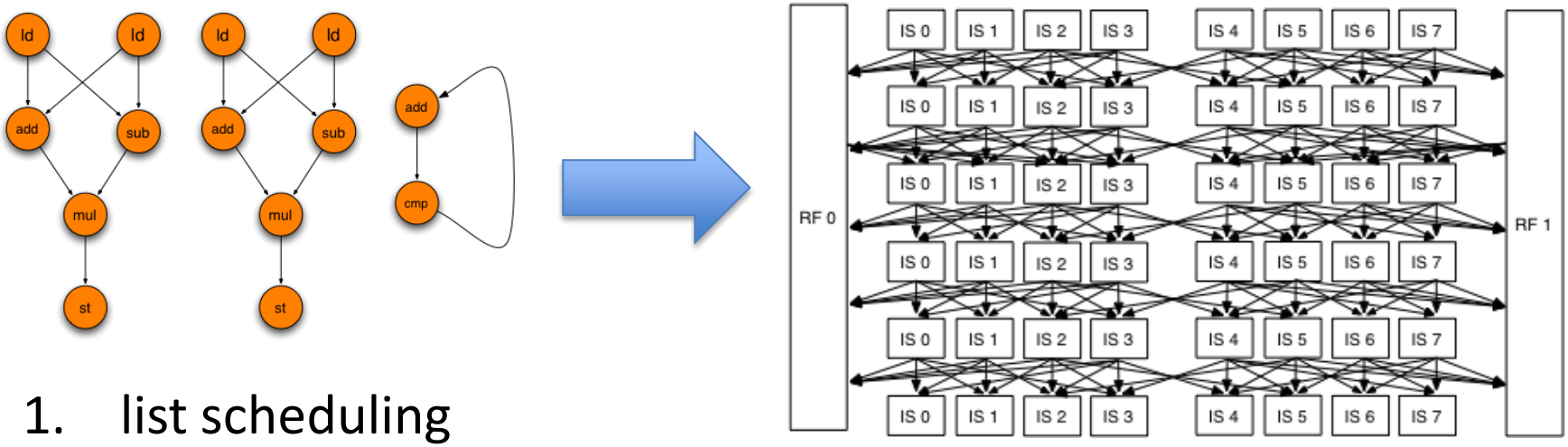
maximum utilization = 1/2

Generate ILP



- loop unrolling
- loop fusion
- loop interchange

CGRA scheduling = graph mapping

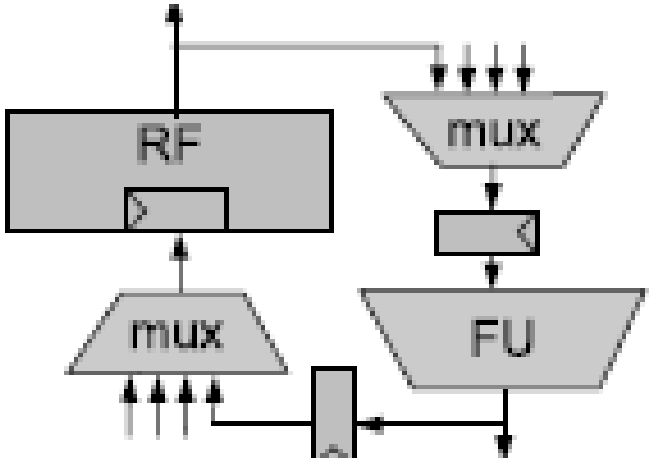


1. list scheduling
   - schedule nodes one by one
   - placement of nodes determined by router
   - resource cost models potential later need for resource
   - most constrained nodes scheduled first, almost no backtracking
2. simulated annealing
   - initial schedule overuses resources
   - try many small changes to schedule until overuse is gone
   - simpler cost function, but it includes overuse

Results multimedia processing

Application	# loops	minimal II	simulated annealing		list scheduling	
			II	time (s)	II	time (s)
3D rendering	80	290	305	44K	315	159
AAC decoder	35	123	141	35K	137	29
AMR-WB+ decoder	44	230	233	20K	235	80
eAAC+ decoder	47	204	217	25K	214	64
H.264 decoder	61	387	470	57K	456	677
mp3 decoder	8	44	45	17K	45	30
MPEG surround decoder	115	522	554	65K	557	510
overall	**390**	**1800**	**1965**	**264K**	**1959**	**1549**

Some more results WLAN



			pipelined			
Loop	#ops	ResMII	RecMII	II	IPC	Time
DemapQAM64	55	4	3	6	9.2	368.1
FFT (64point)	123	8	4	10	12.3	576.7
FFTRadix8	122	8	3	10	12.2	468.3
comp	54	4	4	5	10.8	270.6
DataShuffle	153	14	3	14	10.9	908.5
Average					**11.1**	

non-pipelined			
RecMII	II	IPC	Time
1	6	9.2	110.8
2	12	10.3	256.0
1	12	10.2	195.6
2	5	10.8	77.3
1	16	9.6	878.0
		10.0	

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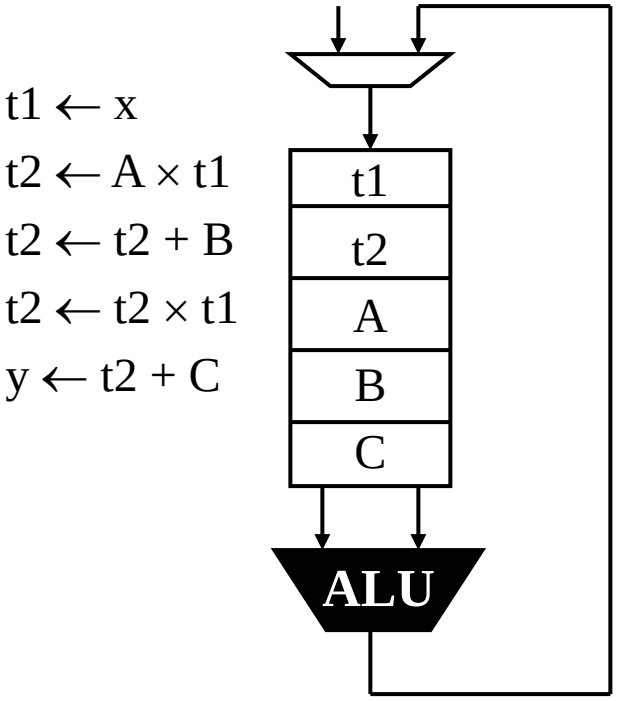
Data dependence graph

sequential C code



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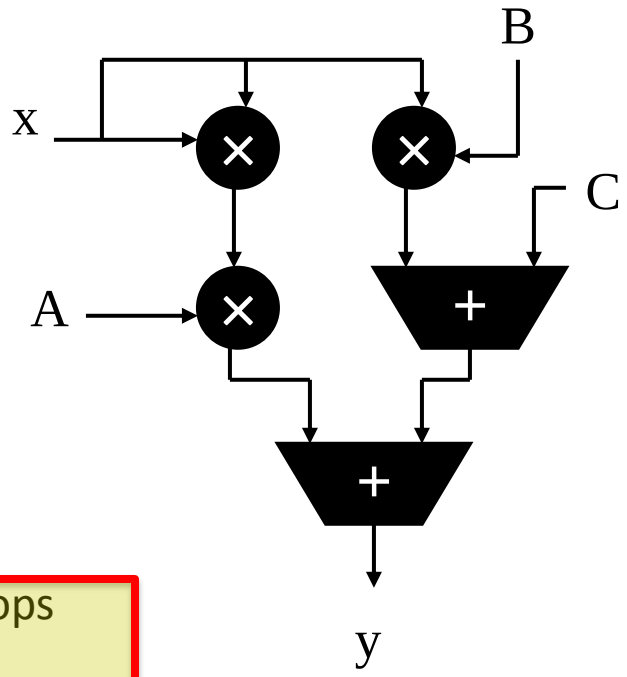

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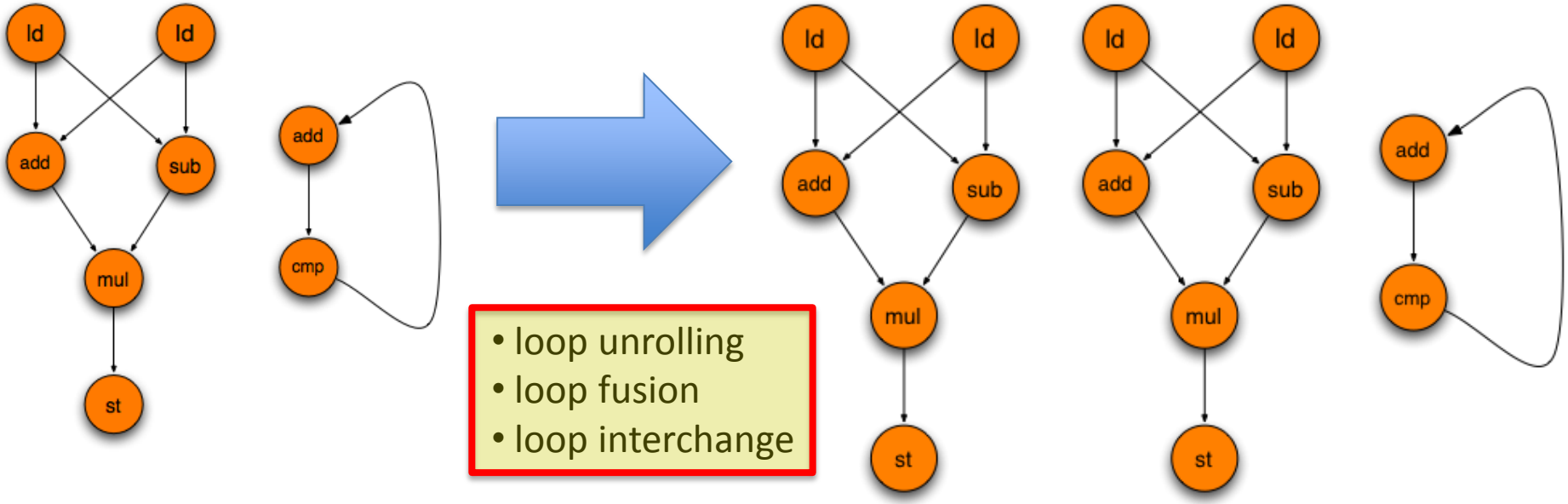

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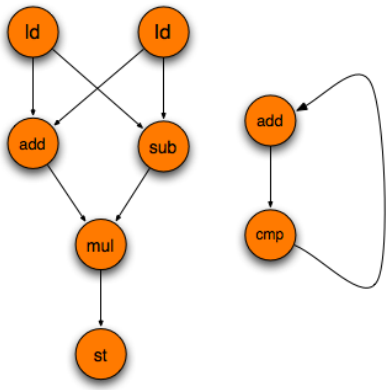

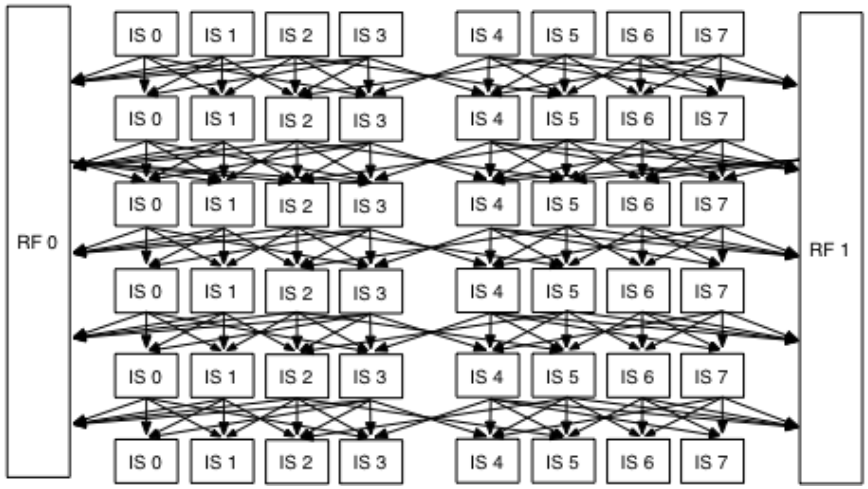

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Example: FIR filter

(a) original 15-tap FIR filter

```
const short c[15] = {-32, ..., 1216};

for (i = 0; i < nr; i++) {
  for(value = 0, j = 0; j < 15; j++)
    value += x[i+j]*c[j];
  r[i] = value;
}
```

(b) filter after loop unrolling, with hard-coded constants

```
const short c00 = -32, ..., c14 = 1216;

for (i = 0; i < nr; i++)
  r[i] = x[i+0]*c00 + x[i+1]*c01 + ... + x[i+14]*c14;
```

Example: FIR filter

(c) filter after redundant memory accesses are eliminated

```
int i, value, d0, ..., d14;
const short c00 = -32, ..., c14 = 1216;

for (i = 0; i < nr+15; i++) {
  d0 = d1;
  ... ;
  d13 = d14;
  d14 = x[i];
  value = c00 * d0 + c01 * d1 + ... + c14 * d14;
  if (i >= 14) r[i - 14 ] = value;
}
```

loop	4x4 ADRES		TI C64+	
	cycles	mem accesses	cycles	mem access
(a)	11828	6221	1054	1618
(b)	1247	3203	1638	2799
(c)	664	422	10062	416

Further reading

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- **register allocation for CGRAs**
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- **Results on real-world applications on ADRES using simulated-annealing**
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