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Electronic Systems of Computers

Lecture 1: Course introduction

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About the course

- Basic organization of a modern computer system
- Main digital electronic components
- Practical approach: design, verify (simulate), and implement in silicon
- Commercial design tools and IP are very expensive (millions)
- Today there are open-source design tools and IP
  - Hardware design is being democratized!

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About me

- José Teixeira de Sousa
  - IST/DEEC professor
  - IObundle manager
- https://www.**linkedin**.com/in/jose-t-de-sousa-a34b86/

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The classes

- Misc lectures (theory/practice/lab)
  - 2 x 1h30 per week
- Laboratory sessions
  - 1 x 1h30 per week

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Theory lectures

- Presentation of materials: 1 hour or less

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Lab sessions

- Groups of 2 students
- 2 Introductory lab assignments (Fibonnacci, GPIO)
- 1 project
  - A simple system for the BASYS3 board will be developed
- Each group element must have a git repository
  - The project will be contained in the repo of one of the group elements
  - Software: C code
  - Hardware: Verilog code of an accelerator for the software
  - Documentation: user guide done in Latex

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Lab tools

- Linux distro and associated tools: Make, code editor (Emacs recommended), bash, sed, etc. 40+GB recommended size
- Icarus Verilog for digital circuit simulation
- Gtkwave for visualizing waveforms
- Tex Live (full installation)
- *FPGA synthesis and implementation*
  - *Xilinx ISE/Vivado?*

Evaluation

- Exam (50%)
- Lab (50%)

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Exam

- Duration:
  - Exam: 2h00
- Check Fénix for dates

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Evaluation criteria

- Instructor will
  - Git clone individual’s git repository
  - Run simulation (make sim)
  - Run FPGA implementation (make fpga)
  - Generate document (make doc)
  - Make sure the above works flawlessly
  - Quality of the solution (performance, frequency, size trade-offs and presentation)

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Course program

- Processor Systems on Chip
- The Verilog Hardware Description Language (HDL)
- The Arithmetic and Logic Unit
- Memories (SRAM, DRAM, CACHE)
- Peripherals, especially for acceleration

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Bibliography

- The Internet!
- Lecture slides
- Lab materials

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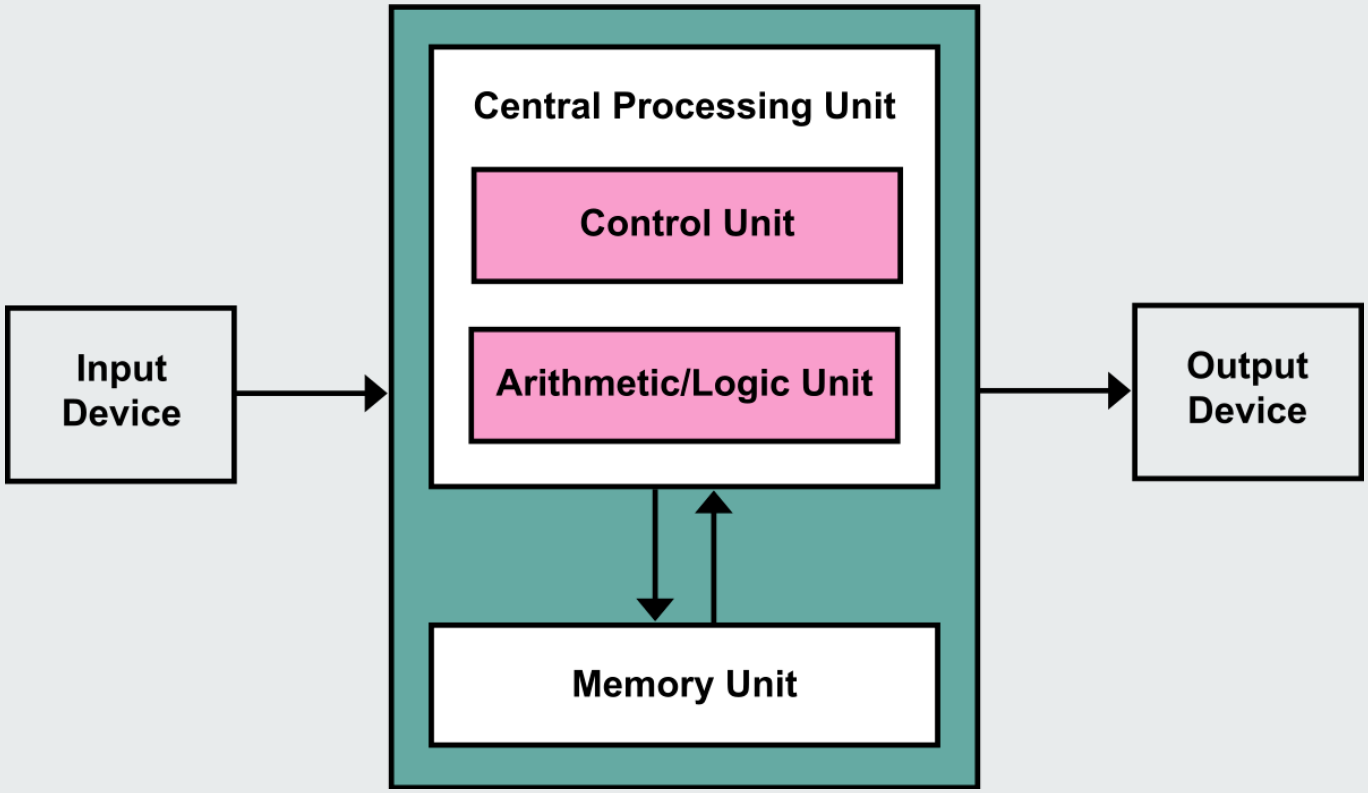
The von Neumann Architecture



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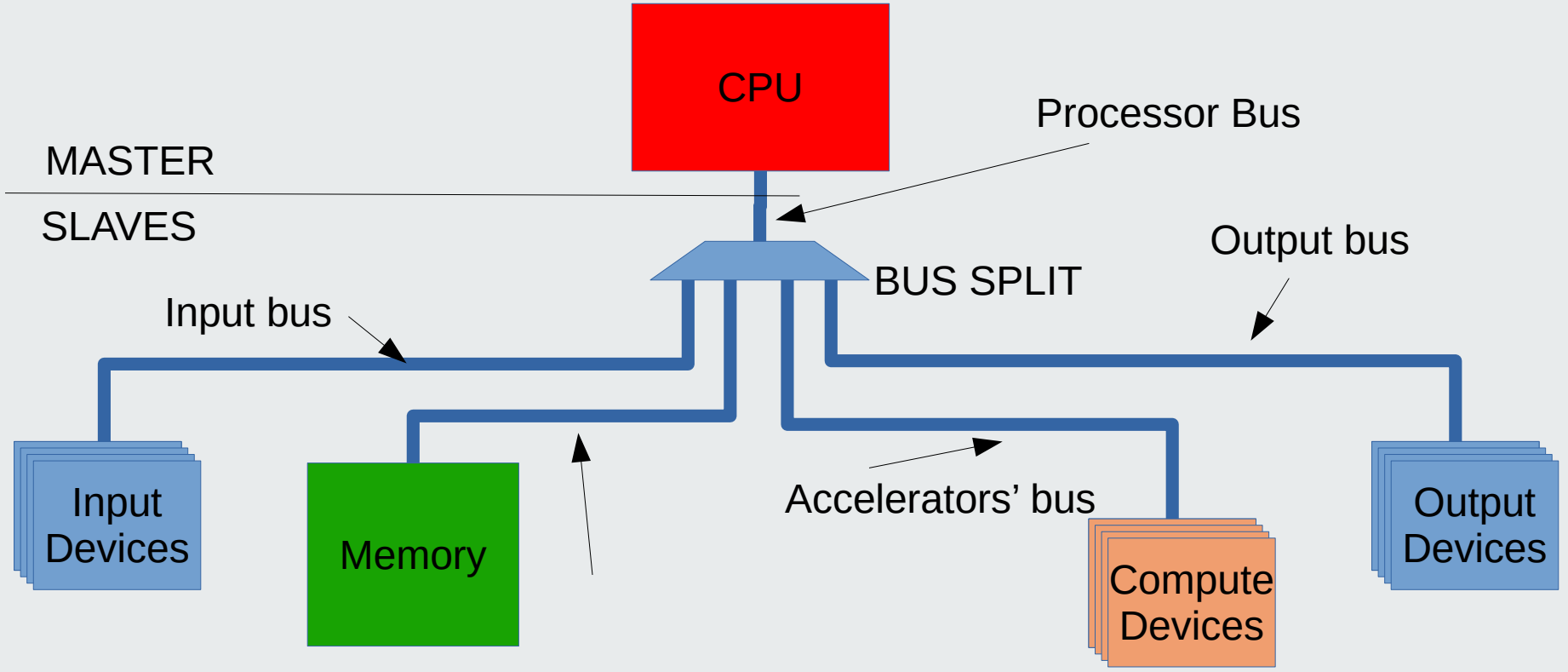
The von Neumann Architecture in practice



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The Processor Bus

- Processor buses can be complex, for example ARM's AXI
- In this course a minimalistic yet effective 6-signal bus called the Native Bus will be used:

	Signal Name	Direction wrt CPU	Width in bits (wires)	Description
REQUEST	Valid	Output	1	CPU wants to access data or instructions
	Address	Output	32	Address of the data
	Wdata	Output	32	Data to write
	Wstrb	Output	4	Byte write
	Rdata	Input	32	Data read
	Ready	Input	1	Slave is ready

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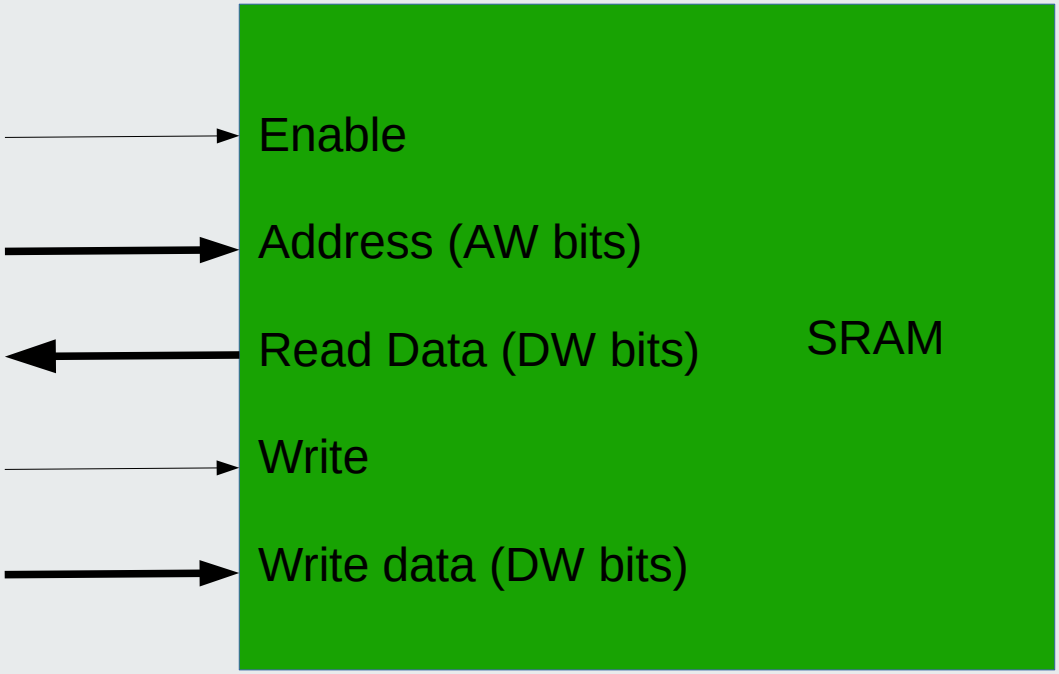
Static Random Access Memory (SRAM): the simplest memory



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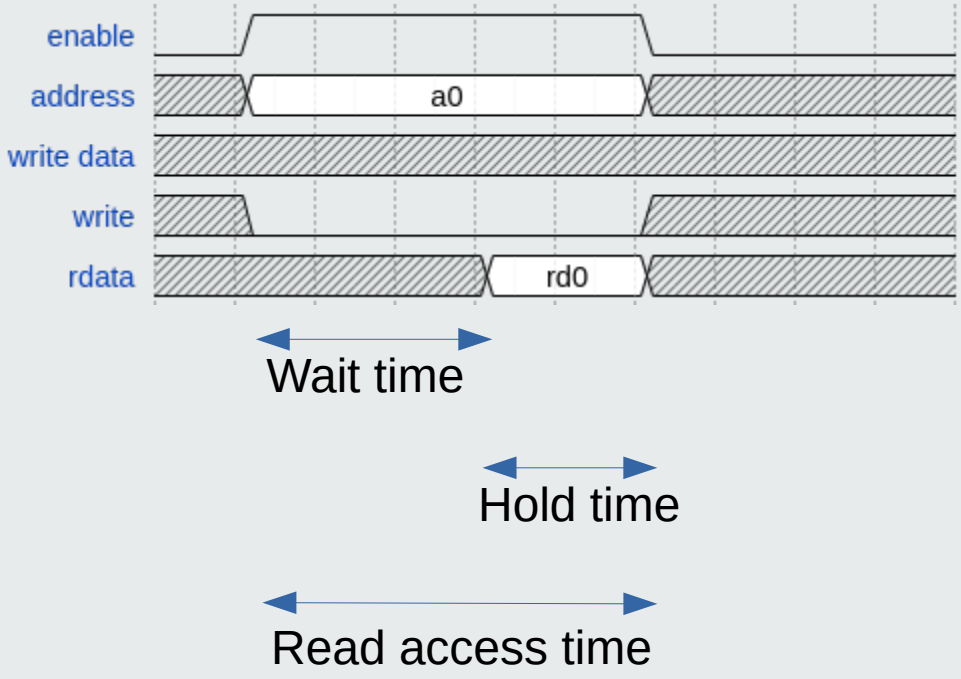
SRAM: reading the memory



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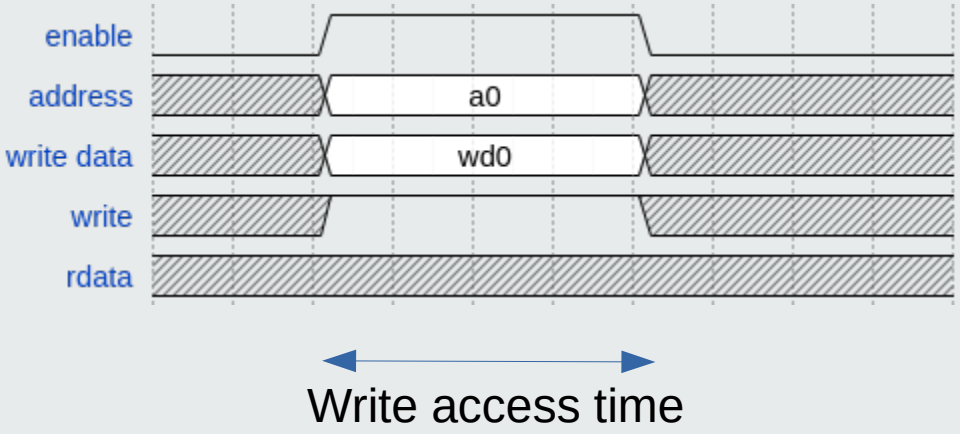
SRAM: writing the memory



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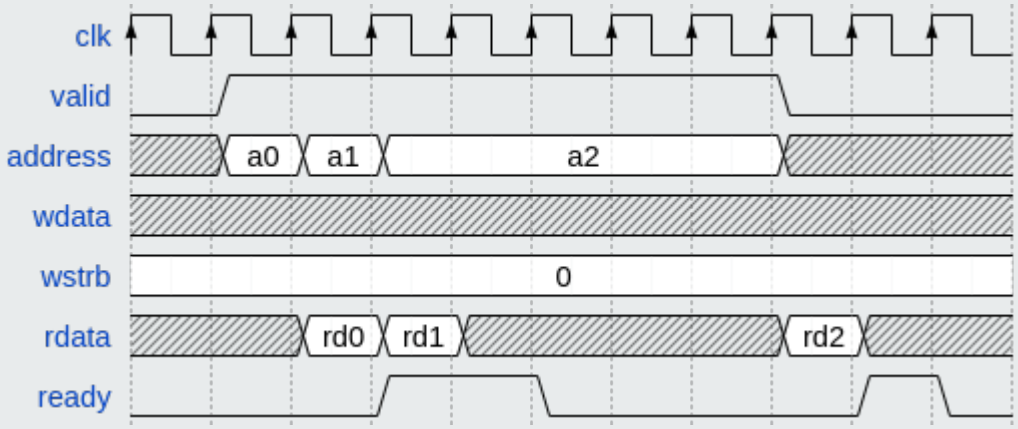
Master reading from slave



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Master writing to slave