TÉCNICO LISBOA

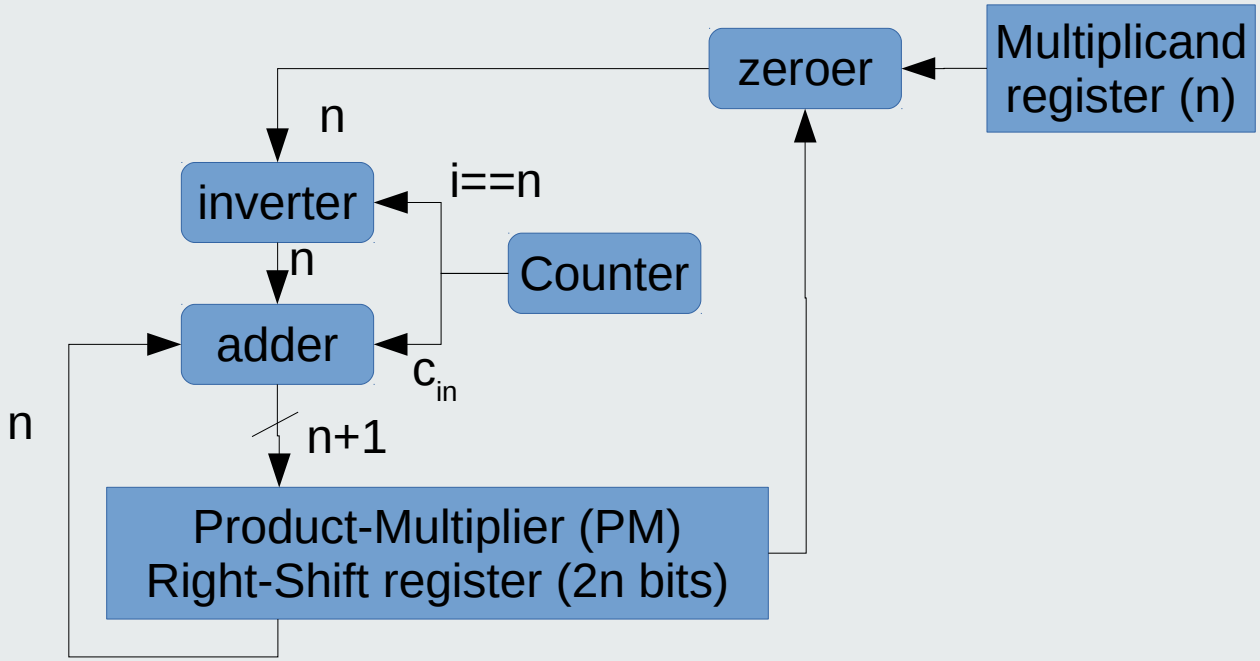
Computer Electronics

Lecture 19: Add-Shift Multiplier, Divider and Shifter Circuits

Add-shift multiply: fundamentals

- Use accumulator register
- Successively add and shift the partial products
- Multiplication ready after N partial products are accumulated
- One accumulation per clock cycle

Add-shift signed multiply: circuit



Add-shift signed multiply: example

$M=-7_{10}=1001$, $m=2_{10}=0010$

$M*m = -14_{10} = 11110010$

Clock cycle	Product /multiplier reg	Comments
0	00000010	Initial: P=0, m=0010
1	00000001	Nop, SRA
2	11001000	Add M, SRA
3	11100100	Nop, SRA
4	11110010	Subtract M, SRA

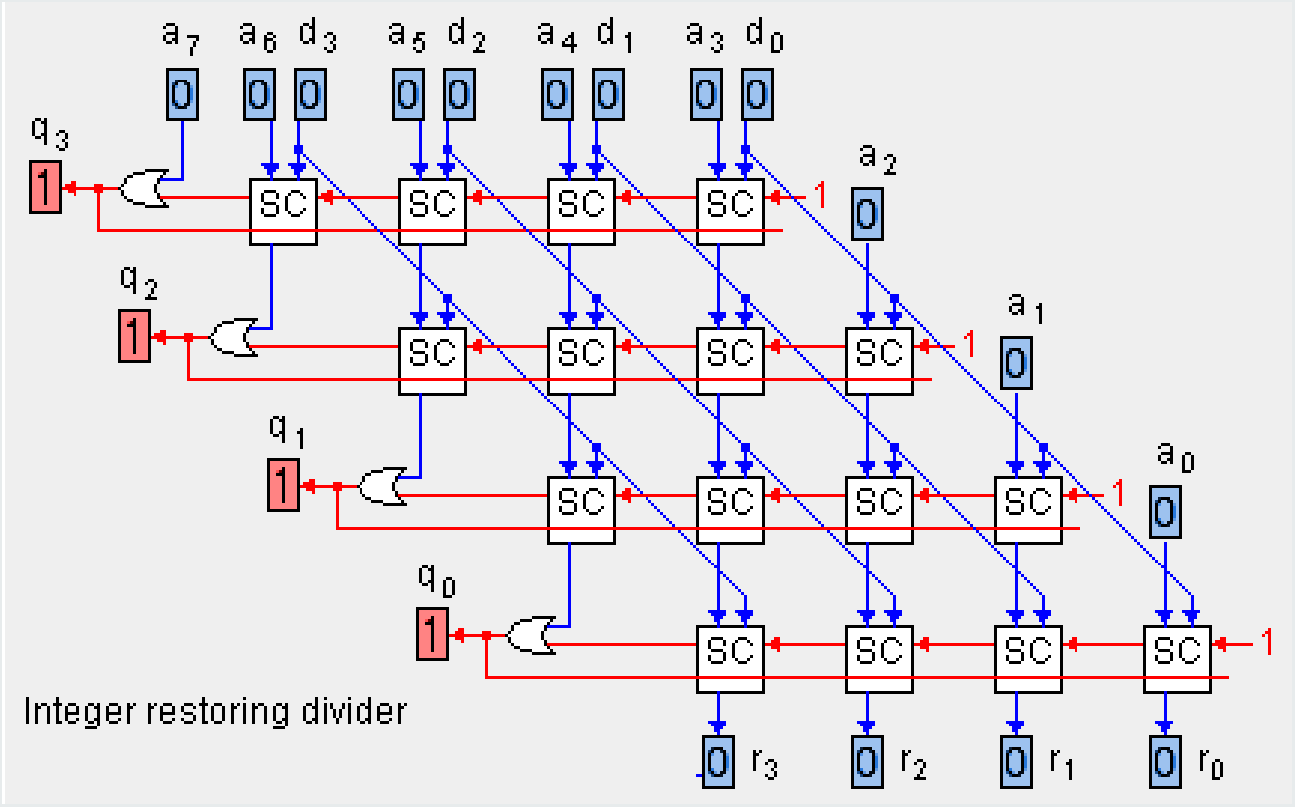
Division algorithm

		1	4		0	3
-	0	3			0	4
		1	4			
	-	1	2			
		0	2			

Dividend: 14 or 1110
Divisor: 3 or 11
Quotient: 4 or 100
Remainder: 2 or 10

				1	1	1	0		0	0	1	1
-	0	0	1	1					0	1	0	0
		0	0	1	1							
	-	0	0	1	1							
			0	0	0	1						
		-	0	0	1	1						
				0	0	1	0					
			-	0	0	1	1					
				0	0	1	0					

Matrix divider



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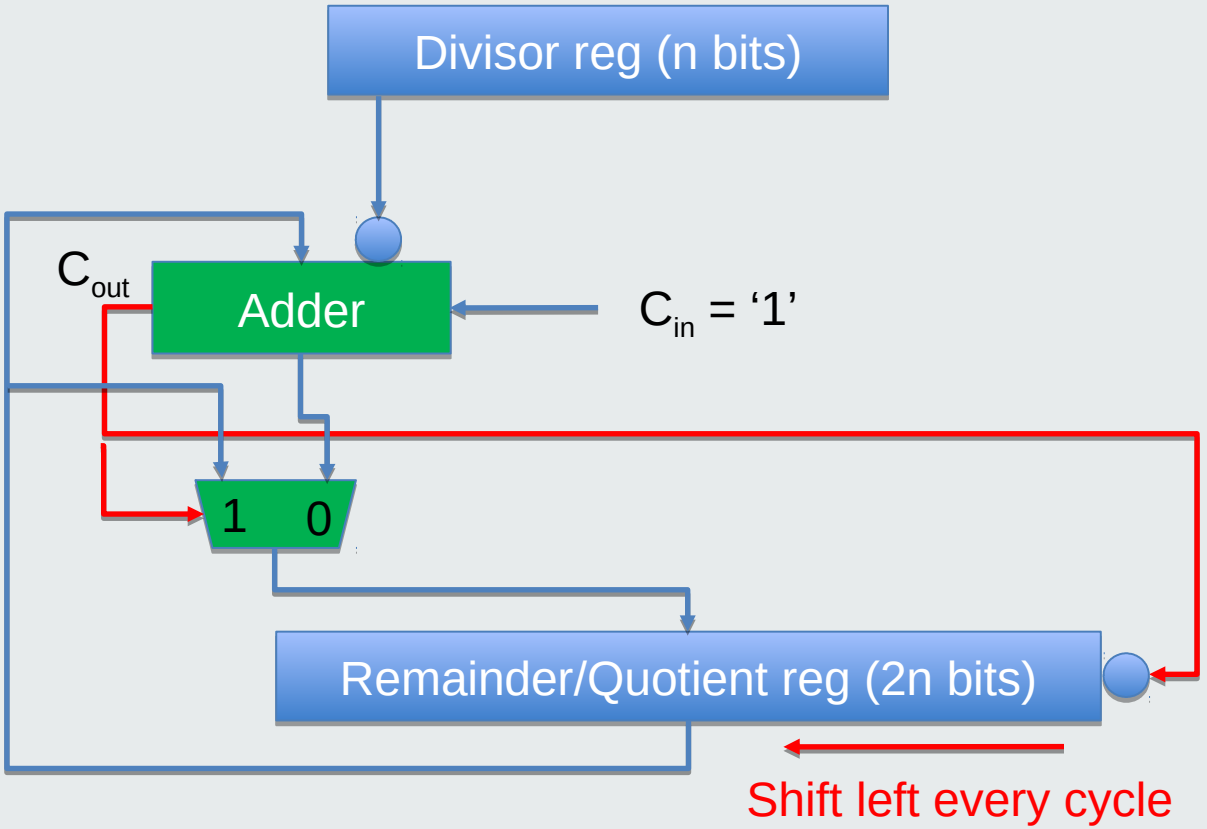
Subtract-shift divider: fundamentals

- Very similar to add-shift multiply
  - Same circuit with few additions does both
- Successively subtract divisor from current remainder and shift left
- Division ready after N subtractions are accumulated
- One accumulation per clock cycle

Subtract-shift divider: circuit



Subtract-shift divide: example

Clock cycle	Remainder/quotient reg	Comments
0	00001110	Initial: r=0000, D=1110
1	00011100	No Sub, SL, q3=0
2	00001001	Sub d, SL, q2=1
3	00010010	No Sub, SL, q1=0
4	00100100	No Sub, SL, q0=0

D=14, d=3 D=1110, d=0011

D/d = q =4, D%d = r = 2, q=0100, r=0010

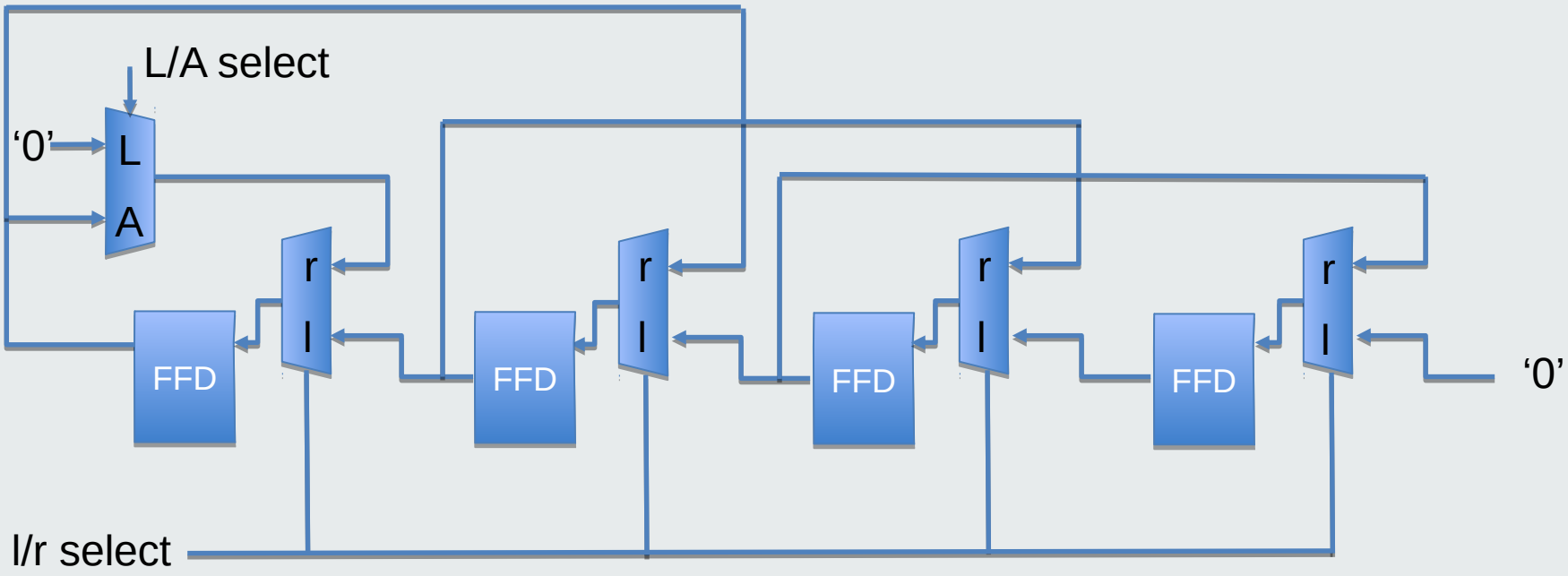
Bit shifting

- Left or right bit shifting is a useful operation
- 1-bit shifting can be accomplished with a shift register
- N-bit shifting is accomplished with a barrel shifter circuit

Single bit shifting

Legend

l/r: left/right
L/A: logical/arithmetic



Shifting types (1-bit displace)

- Left: $b_0 <= 0$, $b_i <= b_{i-1}$
- Left circular: $b_0 <= b_{n-1}$, $b_i <= b_{i-1}$
- Right logical; $b_{n-1} <= 0$, $b_{i-1} <= b_i$
- Right Arithmetic: $b_{n-2} <= b_{n-1}$, $b_{i-1} <= b_i$
- Right circular: $b_{n-1} <= b_0$, $b_{i-1} <= b_i$

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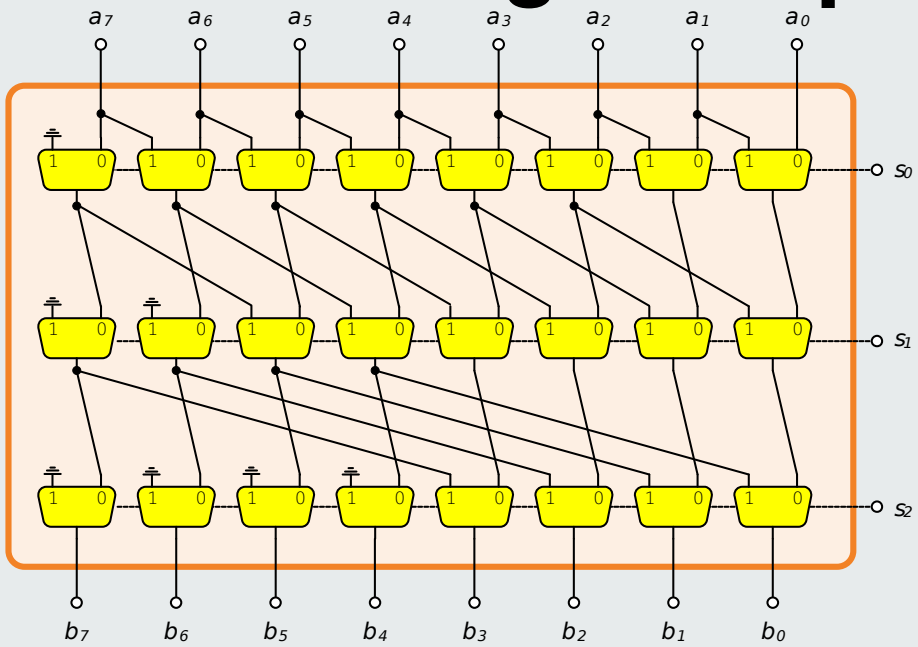
Barrel shifting (*d*-bit displacement)

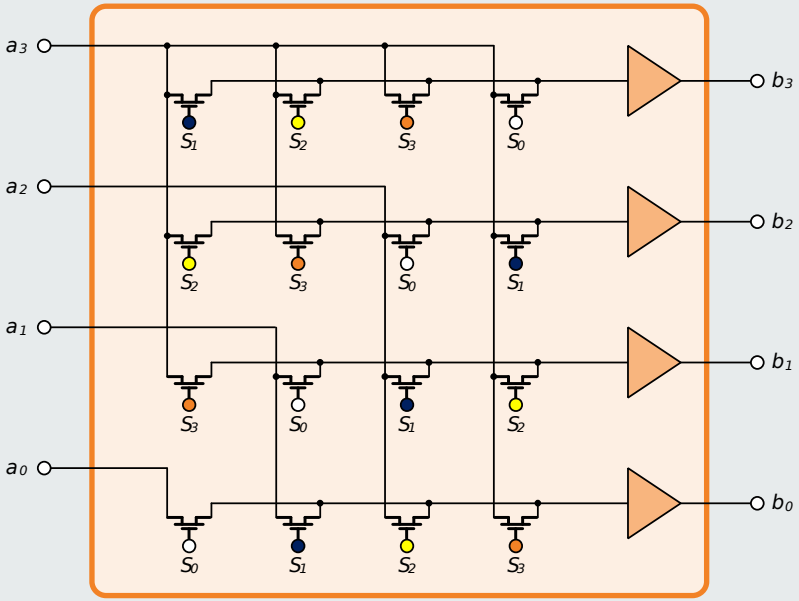
- Displace by *d* bits left or right
- Circular or not
- Arithmetic or logical if right shift

Barrel shifter using multiplexers



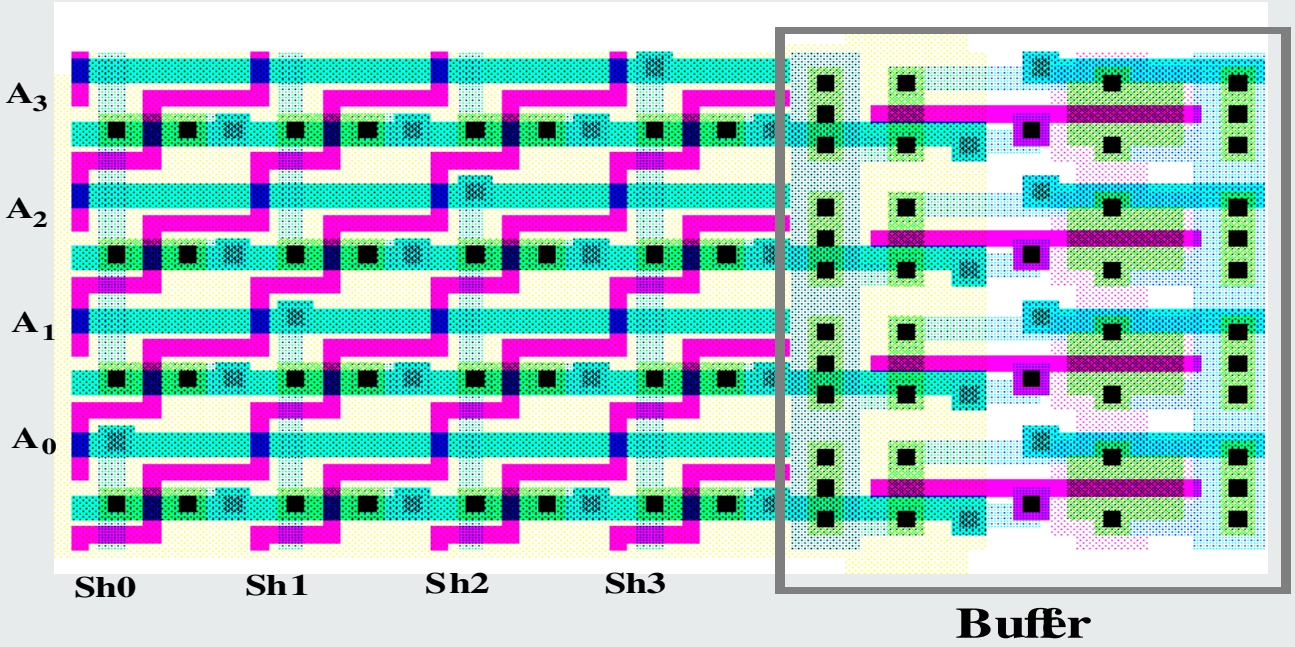
- Spatial complexity O(N*logN)
- Right logical

Barrel shifter using transistor matrix



- Spatial complexity $O(N^2)$
- Right arithmetic

Transistor matrix BS – layout



- Most space taken by interconnects rather than transitors