

# Computer Electronics

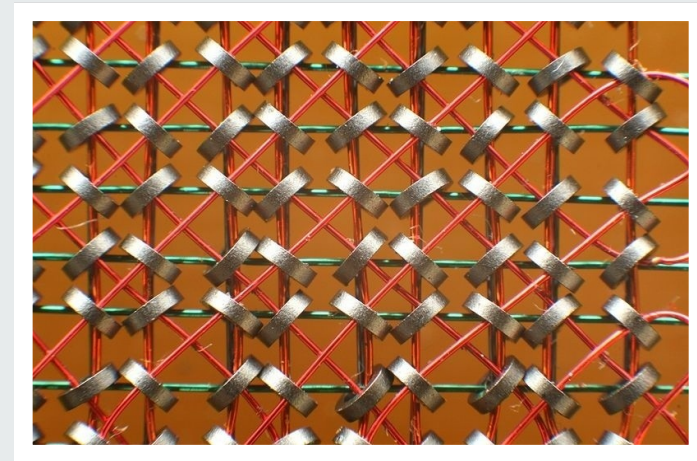
## Lecture 23: Memory Organization

# Outline

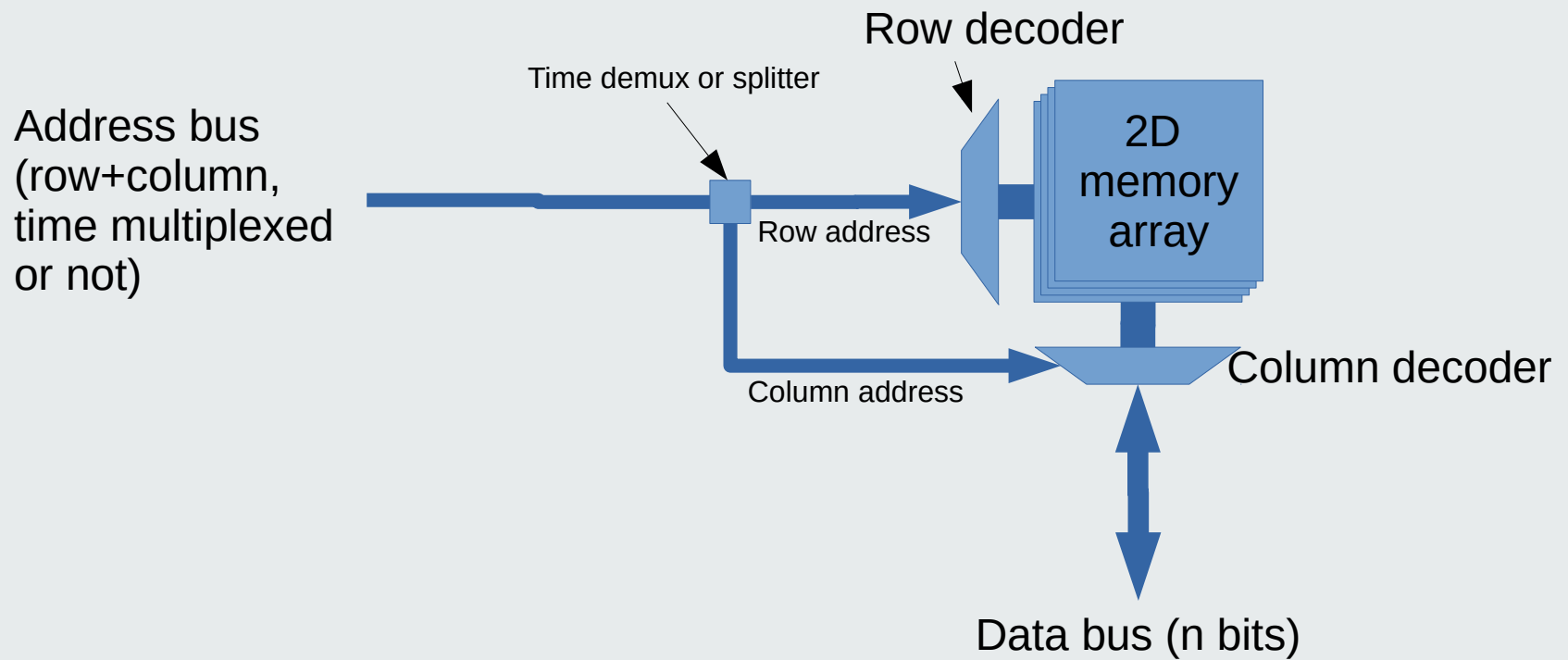
- Organization of memory cells
- Address and data busses
- Memory hierarchy
- DRAM devices revisited
- Bank interleaving
- SIMM and DIMM
- Combining memory chips for width and depth
- Rank, bank, row, column

# Memory cell organization

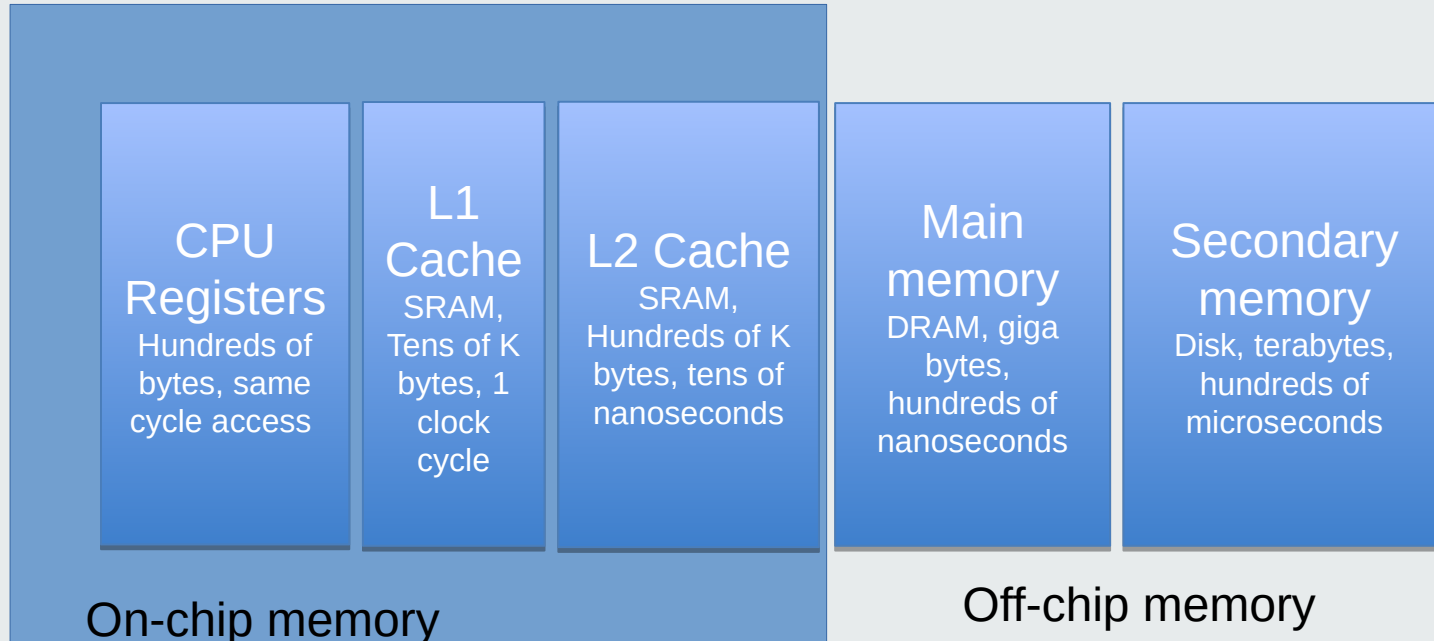
- Matrix organization since ferrite memories
- Optimal 2D organization
- Future
  - 3D organization (layer, row, column)
  - nD organization with quantum memories



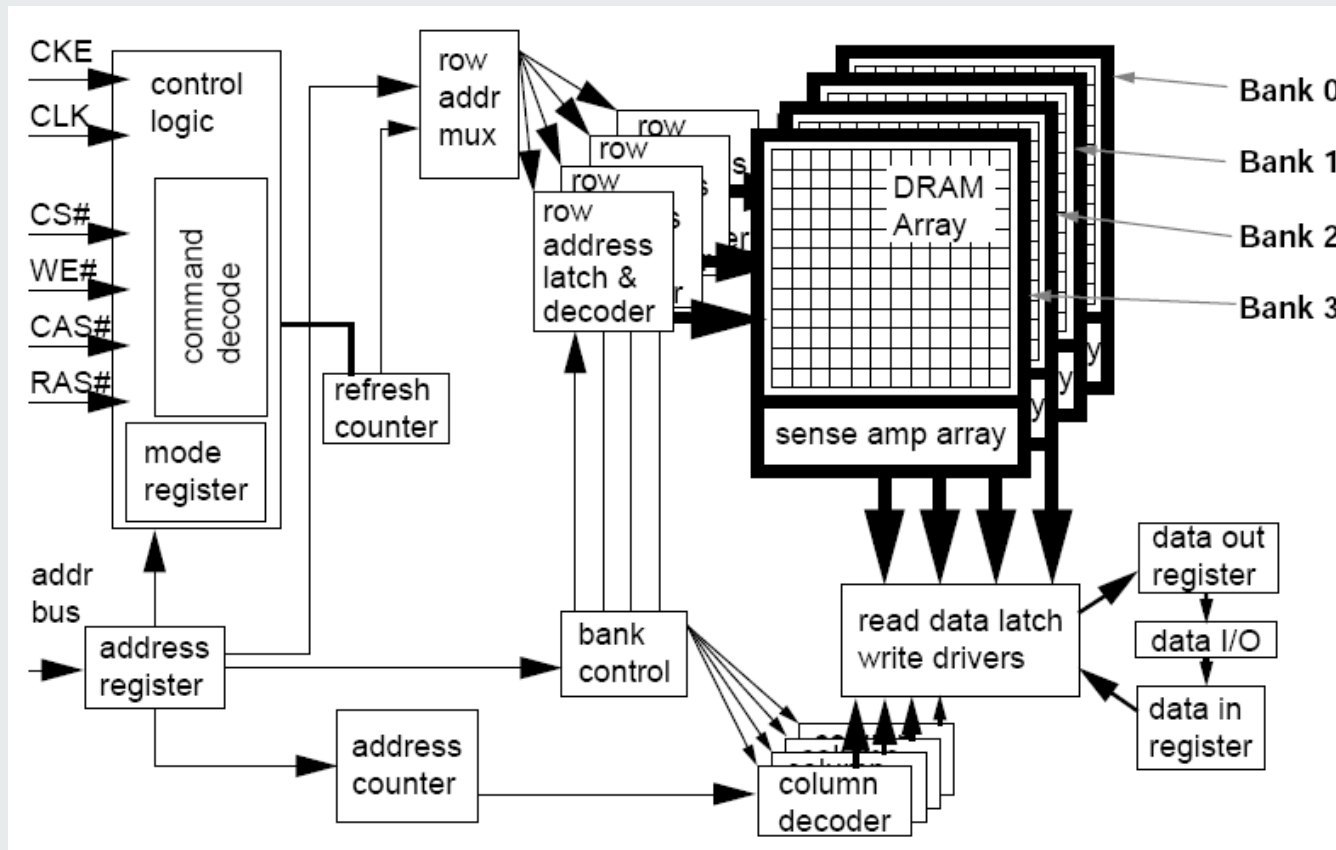
# Address and data busses



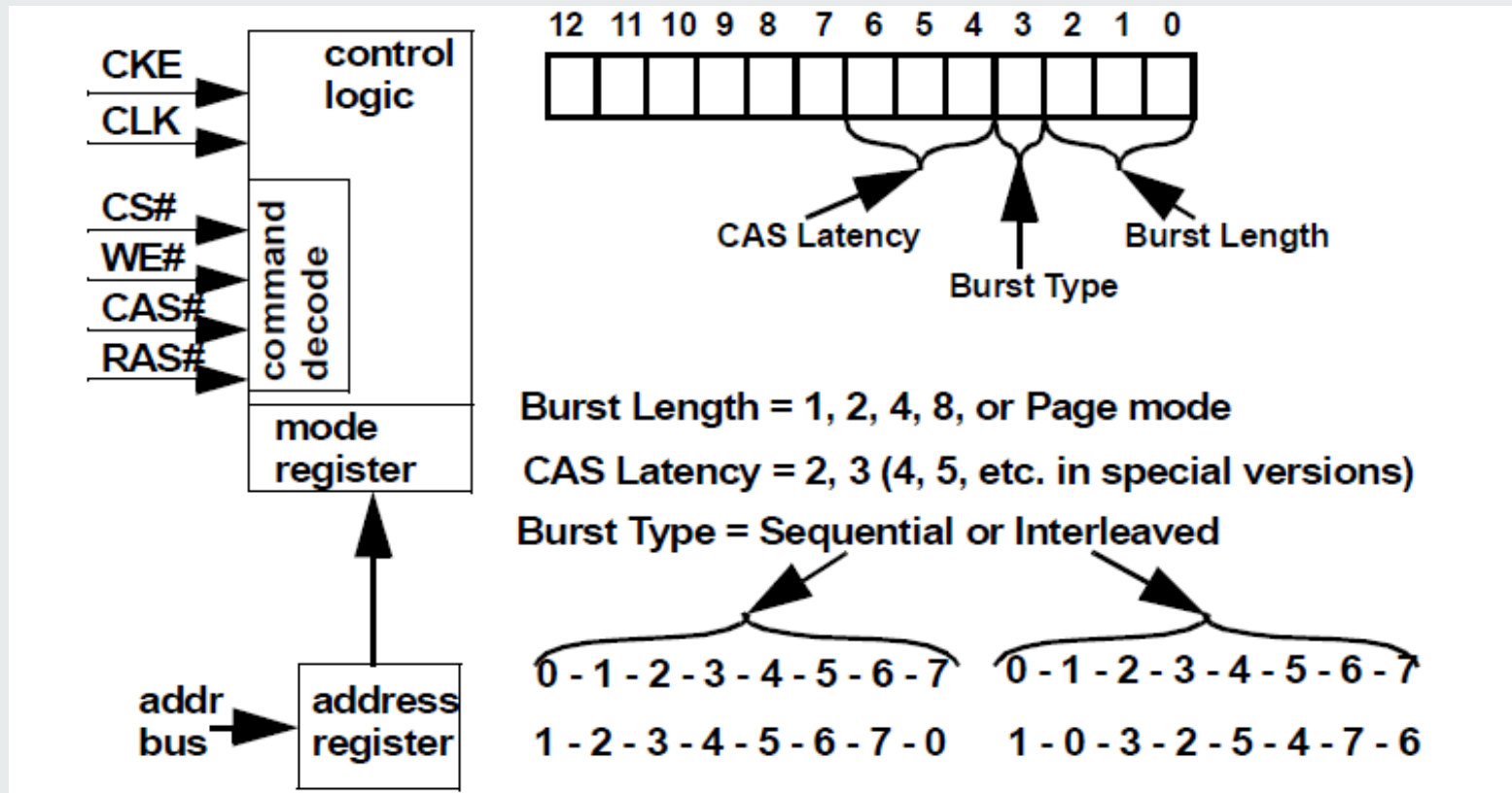
# Memory hierarchy



# SDRAM chip example architecture



# SDRAM chip control



# Possible device configurations

Device configuration	64 Meg x 4	32 Meg x 8	16 Meg x 16
Number of banks	4	4	4
Number of rows	8192	8192	8192
Number of columns	2048	1024	512
Data bus width	4	8	16

Super cell size

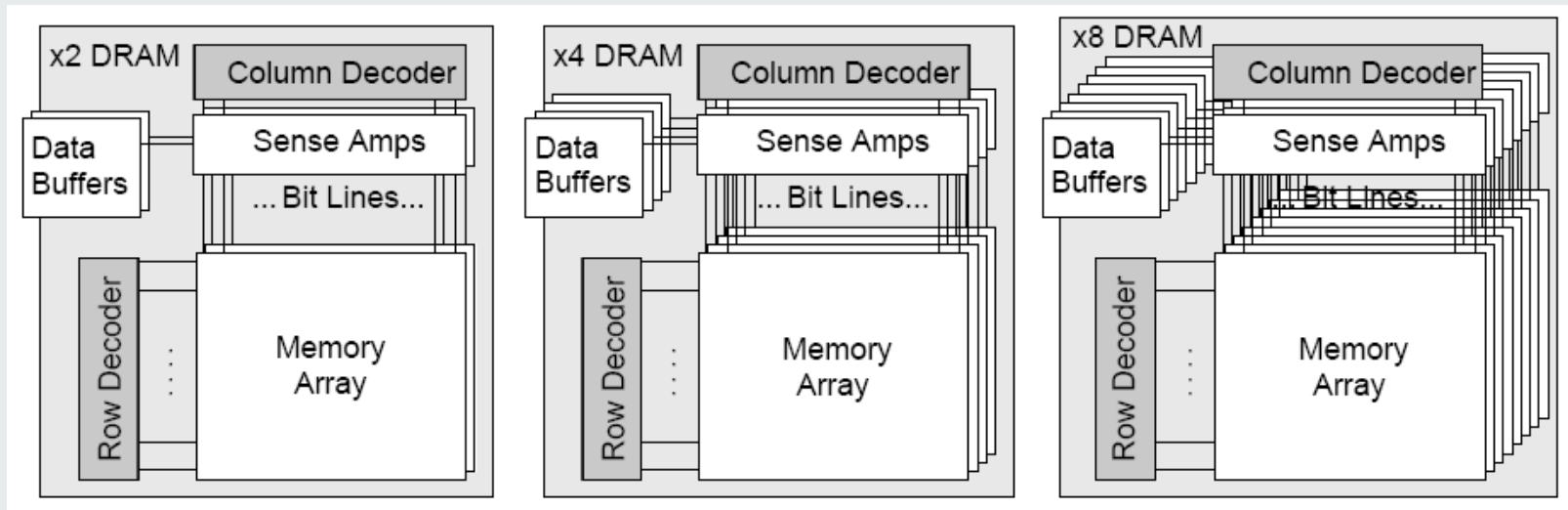
1

2

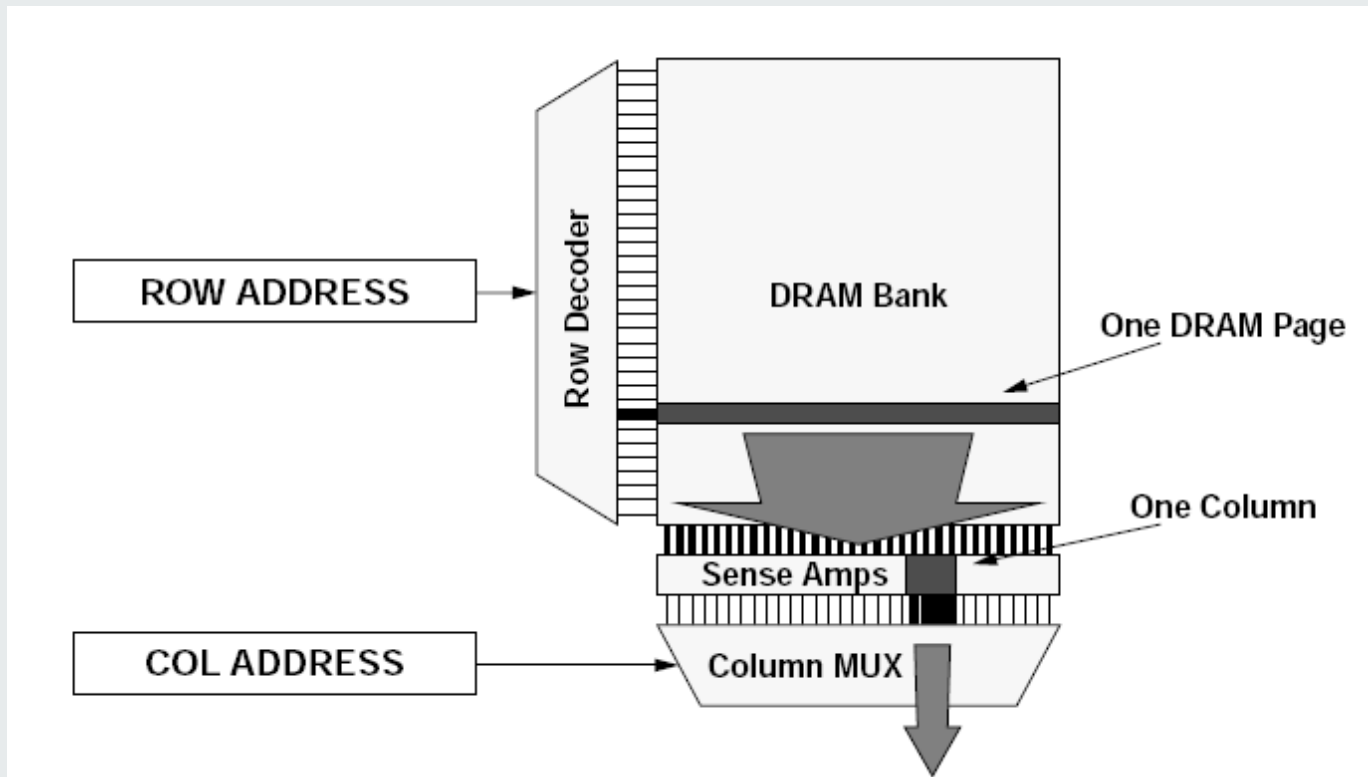
4



# DRAM: different data widths



# DRAM page



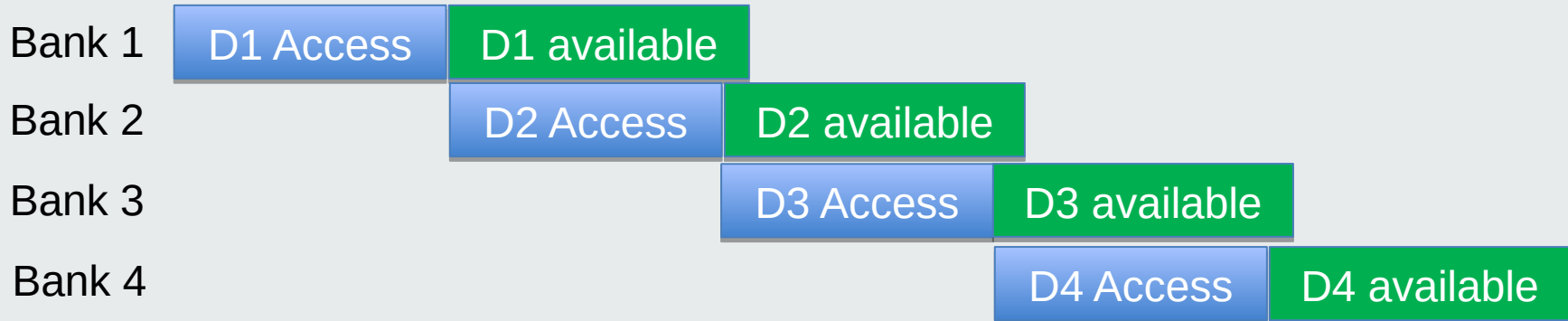
# Bank interleaving

- Increase bandwidth by interleaving

Without interleaving – slower

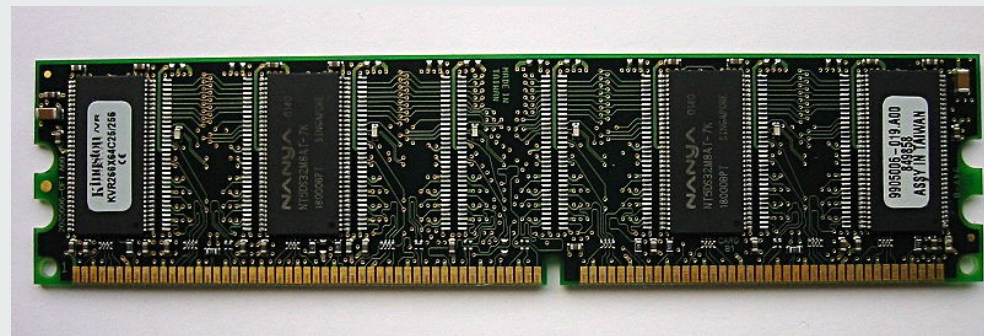
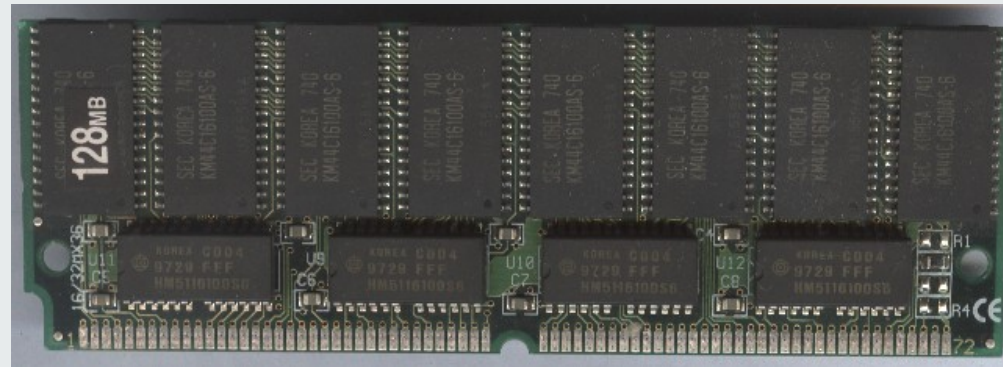


With interleaving – faster, pipelined

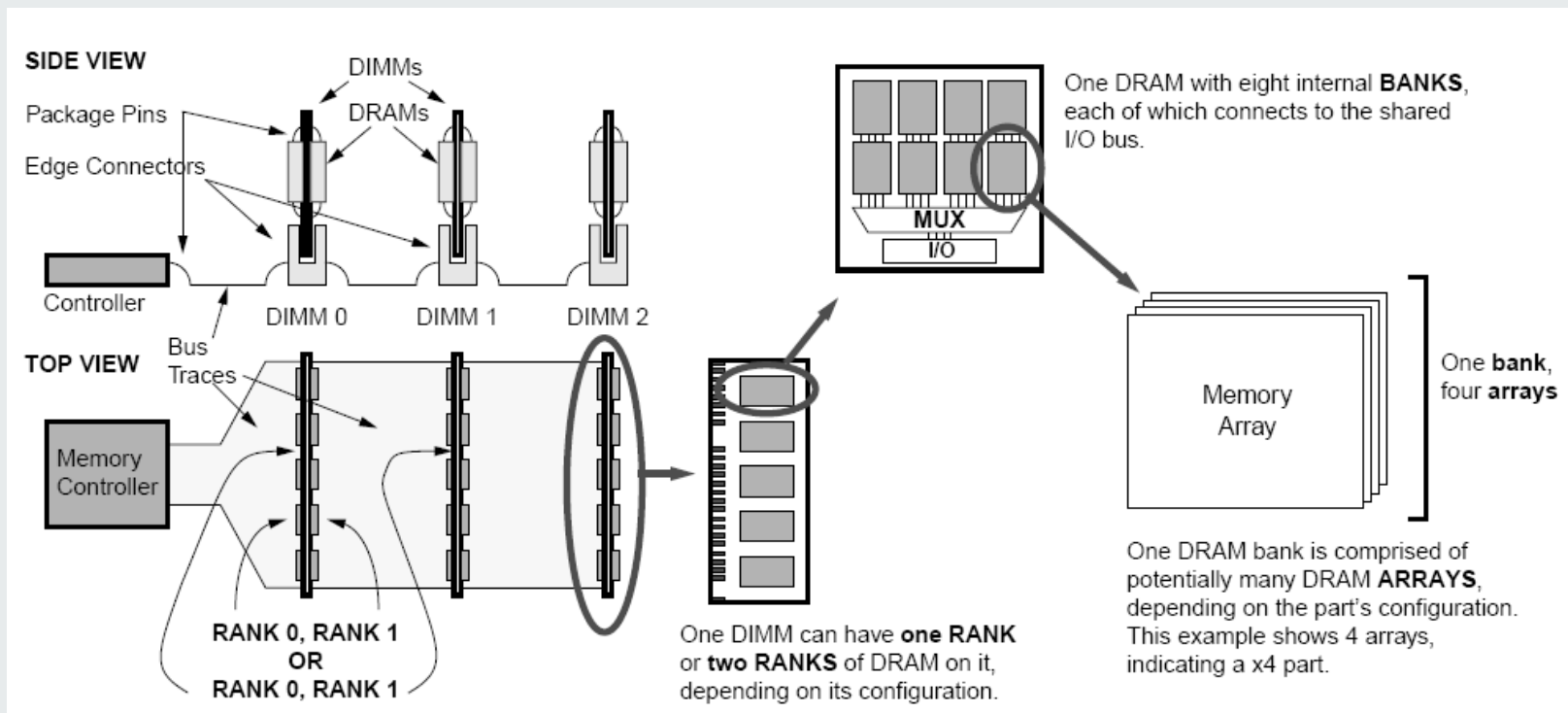


# SIMM and DIMM

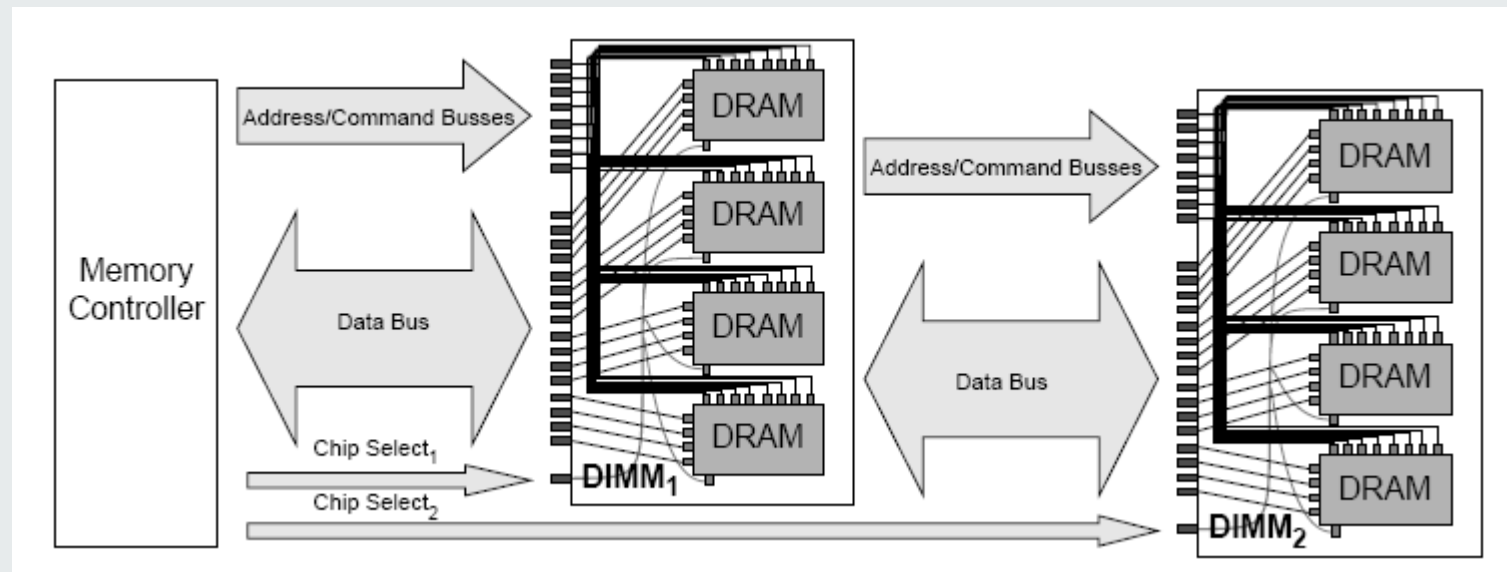
- Single Inline Memory Module
  - Same connectors on both sides
  - Obsolete
- Dual Inline Memory Module
  - Different connectors on either side



# Dual Inline Memory Module (DIMM)

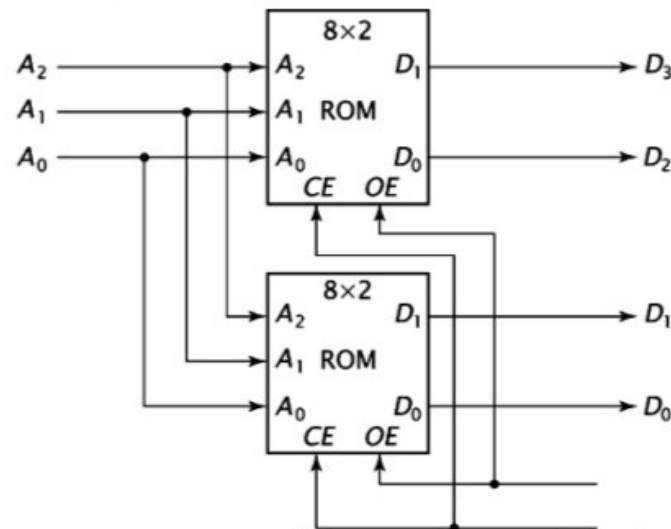


# DIMM connections



# Combining memory chips to increase data width

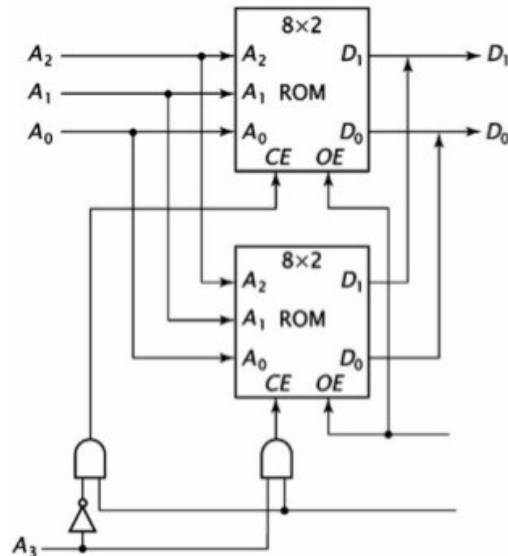
## Memory Subsystems Organization (1)



- Two or more memory chips can be combined to create memory with more bits per location (two 8X2 chips can create a 8X4 memory)

# Combining memory chips to increase memory locations

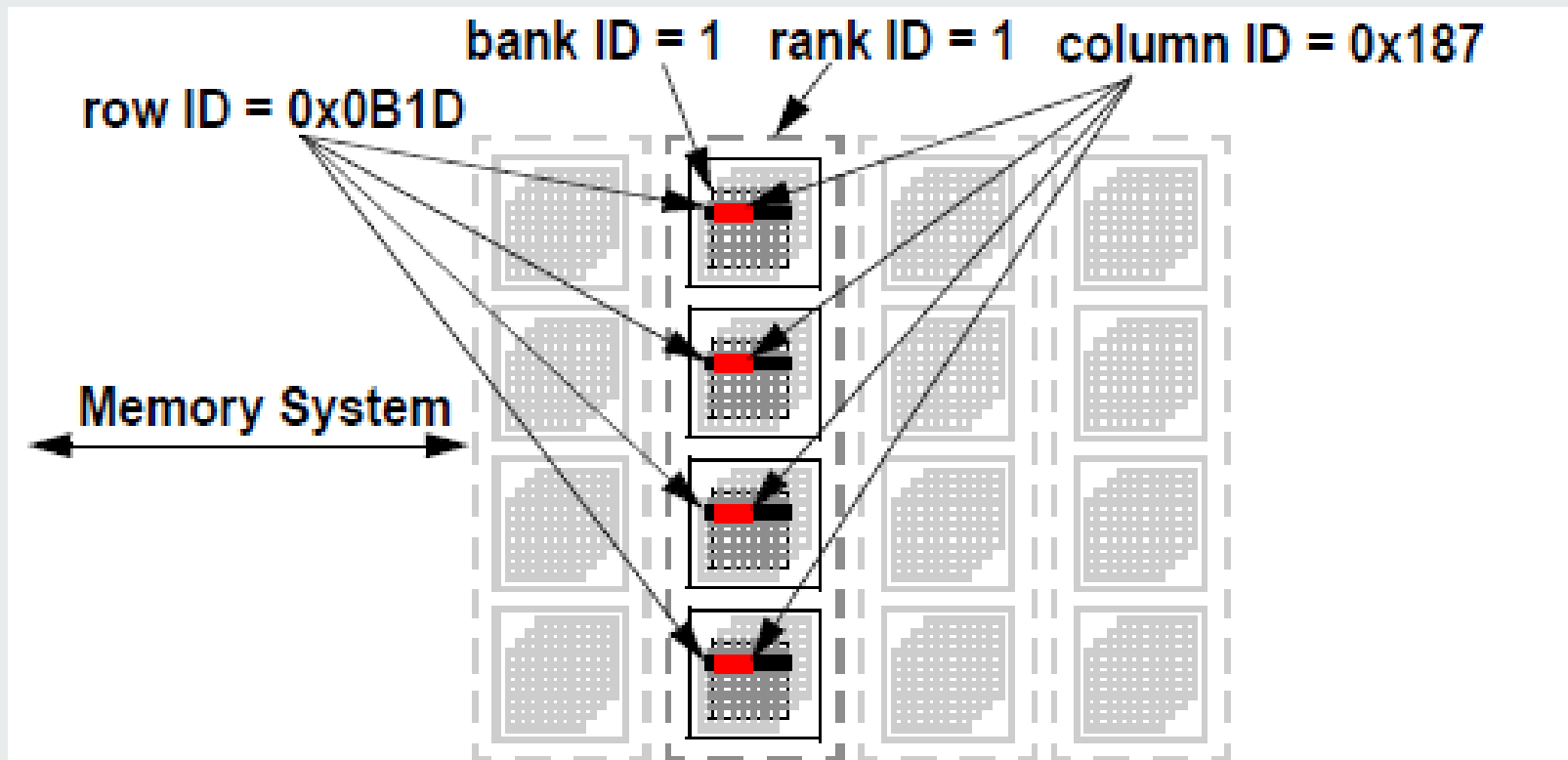
## Memory Subsystems Organization (2)



- Two or more memory chips can be combined to create more locations (two 8X2 chips can create 16X2 memory)



# Rank, Bank, Column, Row



# 128MB module example

Capacity	device density	number of ranks	devices per rank	device width	number of banks	number of rows	number of columns
128 MB	64 Mbit	1	16	x4	4	4096	1024
128 MB	64 Mbit	2	8	x8	4	4096	512
128 MB	128 Mbit	1	8	x8	4	4096	1024
128 MB	256 Mbit	1	4	x16	4	8192	512