Computer Electronics

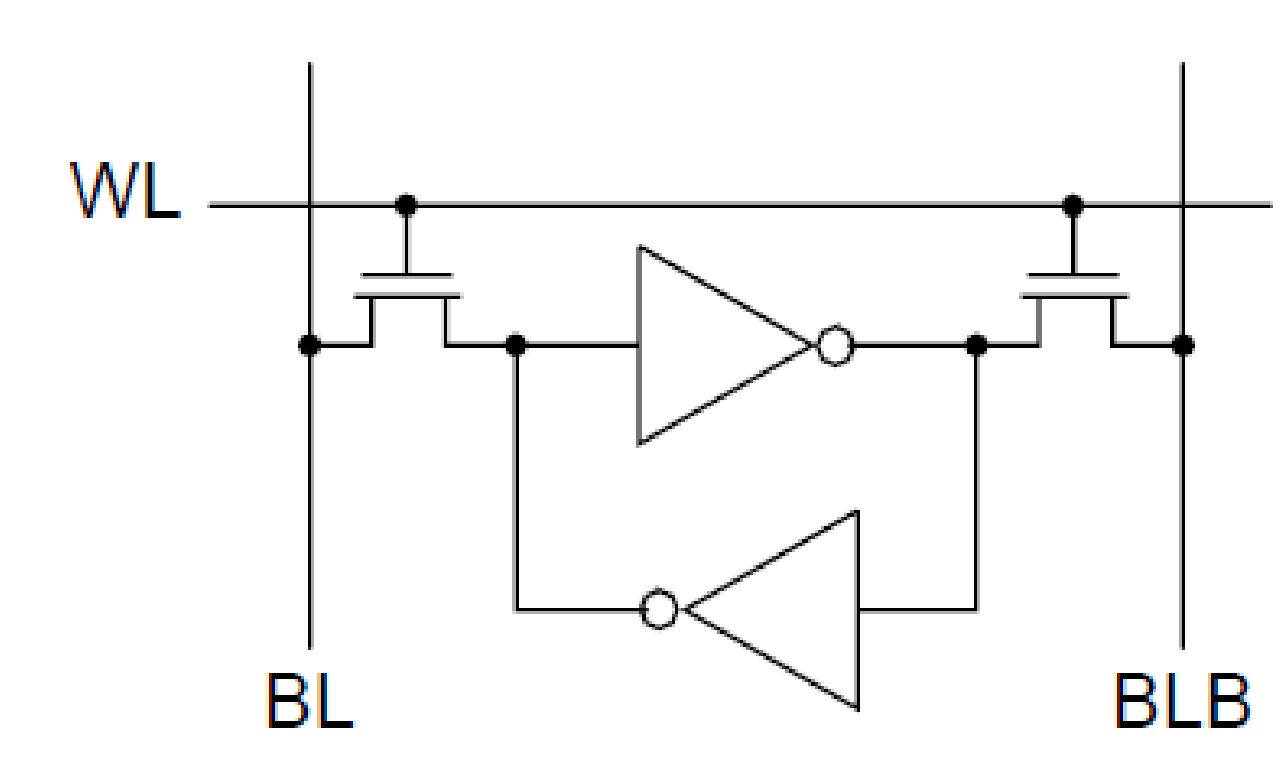
Lecture 22: SRAM

TÉCNICO LISBOA

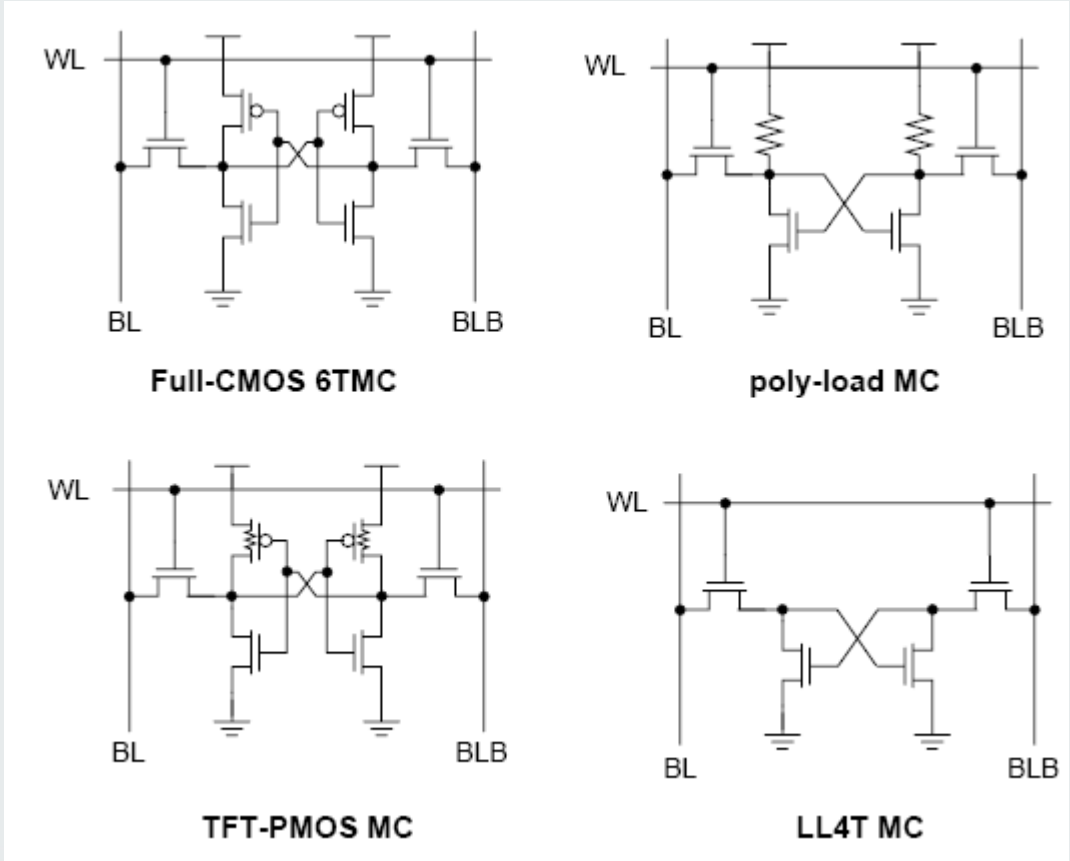
Outline

- Static memory cells
- DRAM vs. SRAM
- SRAM read operation
- SRAM write operation
- SRAM sense and write amplifiers

A static memory cell

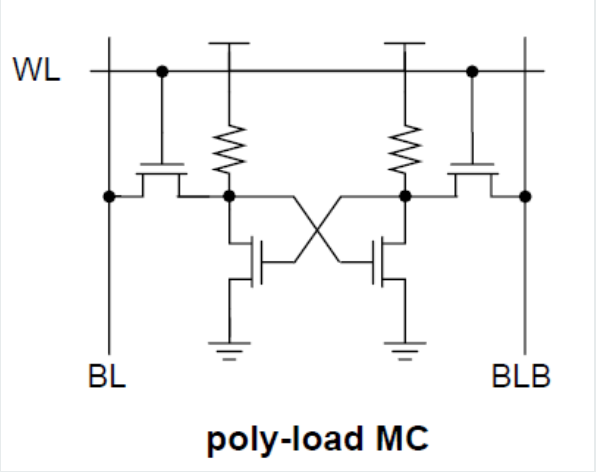


Static cell types



Poly load

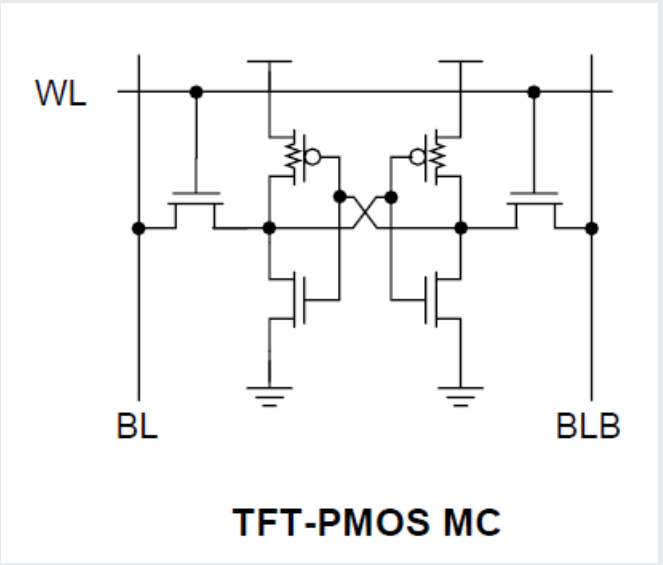
- Implemented in a separate polysilicon layer
- Advantage:
  - 30% area reduction
- Disadvantages
  - Non standard technology
  - Resistors can’t be shrunk anymore



poly-load MC

TFT PMOS

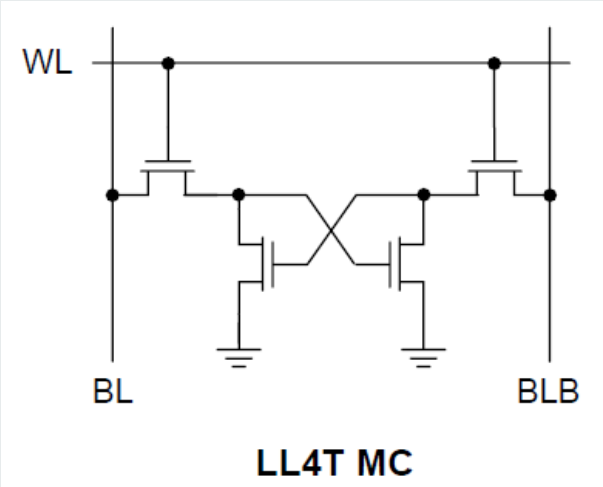
- Polysilicon transistor built on top of NMOS transistor
- Advantage:
  - Area reduction
- Disadvantage
  - Non standard technology



TFT-PMOS MC

Loadless SRAM Cell

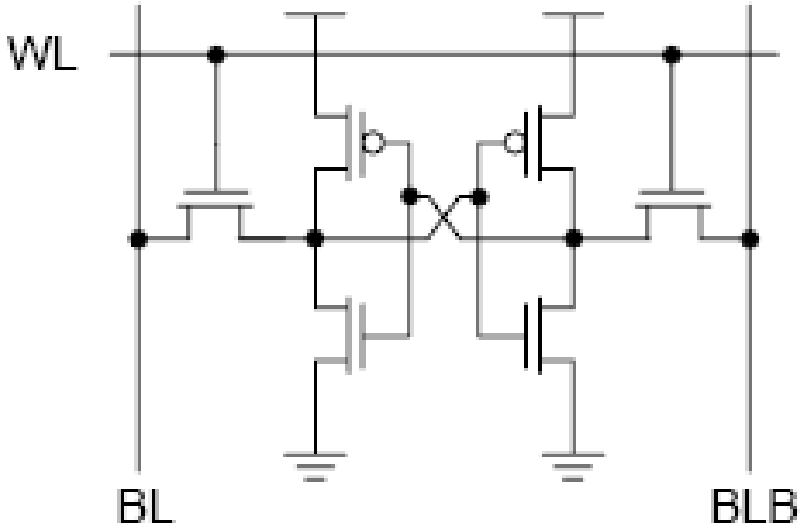
- Information stored in gate capacitor
- Advantages:
  - Standard technology
  - Up to 65% area reduction!
- Disadvantage
  - Leakage current may wipe info away



LL4T MC

6T standard SRAM cell

- Most common SRAM cell
- Advantage:
  - Implemented with regular CMOS technology
- Disadvantage
  - Larger area

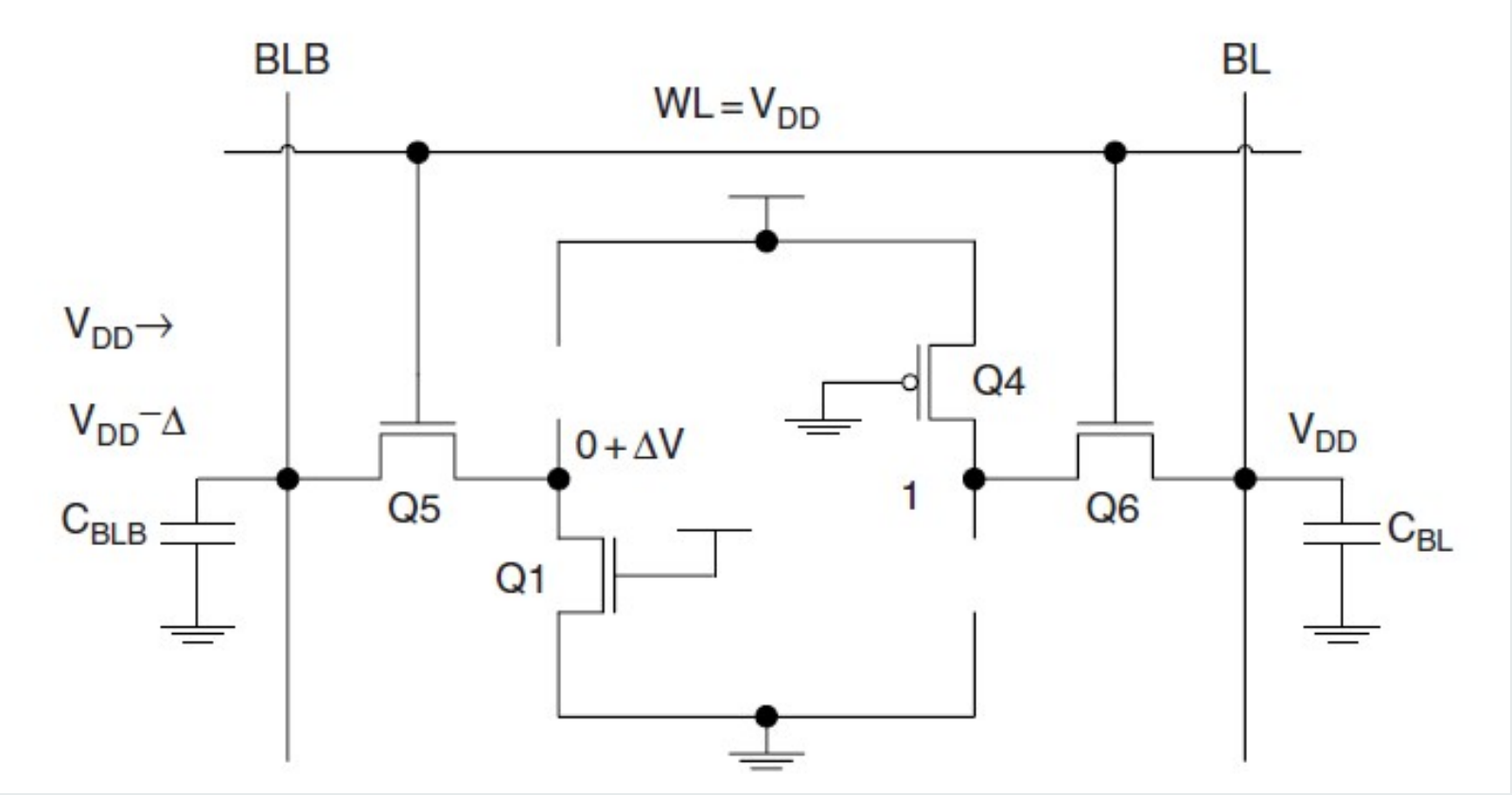


Full-CMOS 6TMC

SRAM vs DRAM

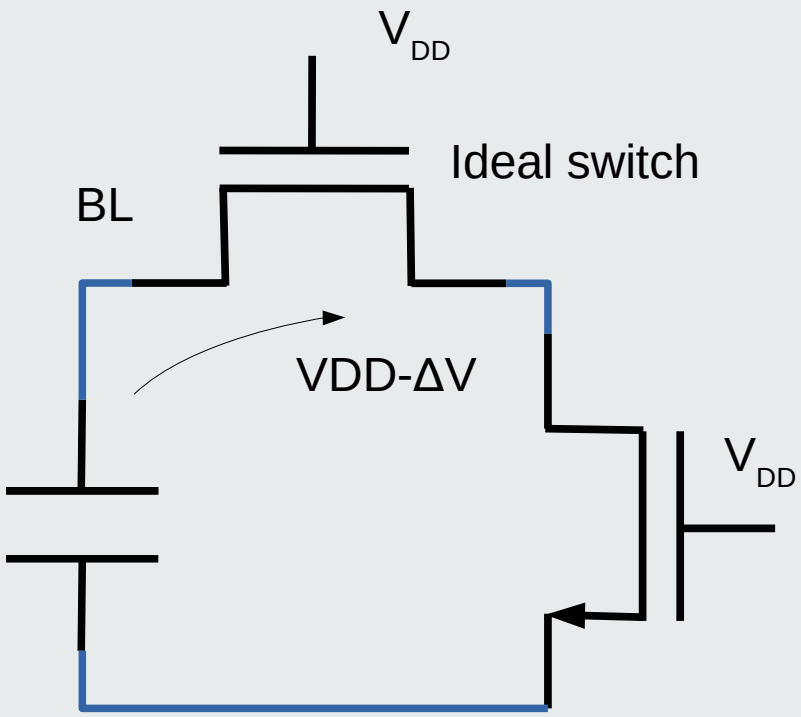
- Cells are much larger: 6T instead of 1T+1C(parasitic). DRAM is denser
- Cells consume only leakage current, no expensive periodic refresh. SRAM is lower power
- Cost is exponential with area due to Yield problems
- SRAM much more expensive than DRAM (cost per bit)

SRAM read operation



SRAM read circuit

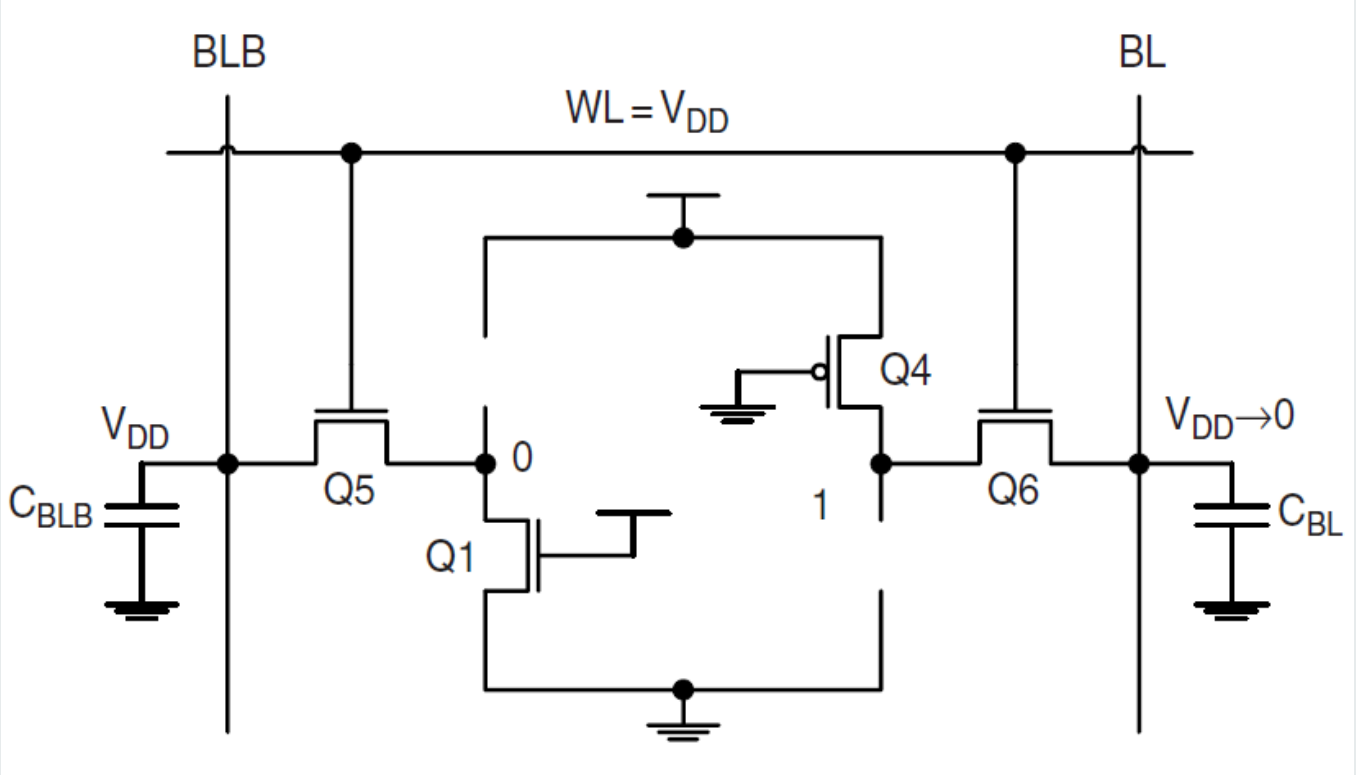
- Pre-charge BL at VDD
- Turn on the access switch
- Wait for a voltage at BL to drop
- Note that BLB voltage stuck at V_{DD}
- $I_D = k(V_{DD}-V_T)^2$ (constant current discharge)
- $\Delta t = C_d \Delta V / I_D$



SRAM read procedure

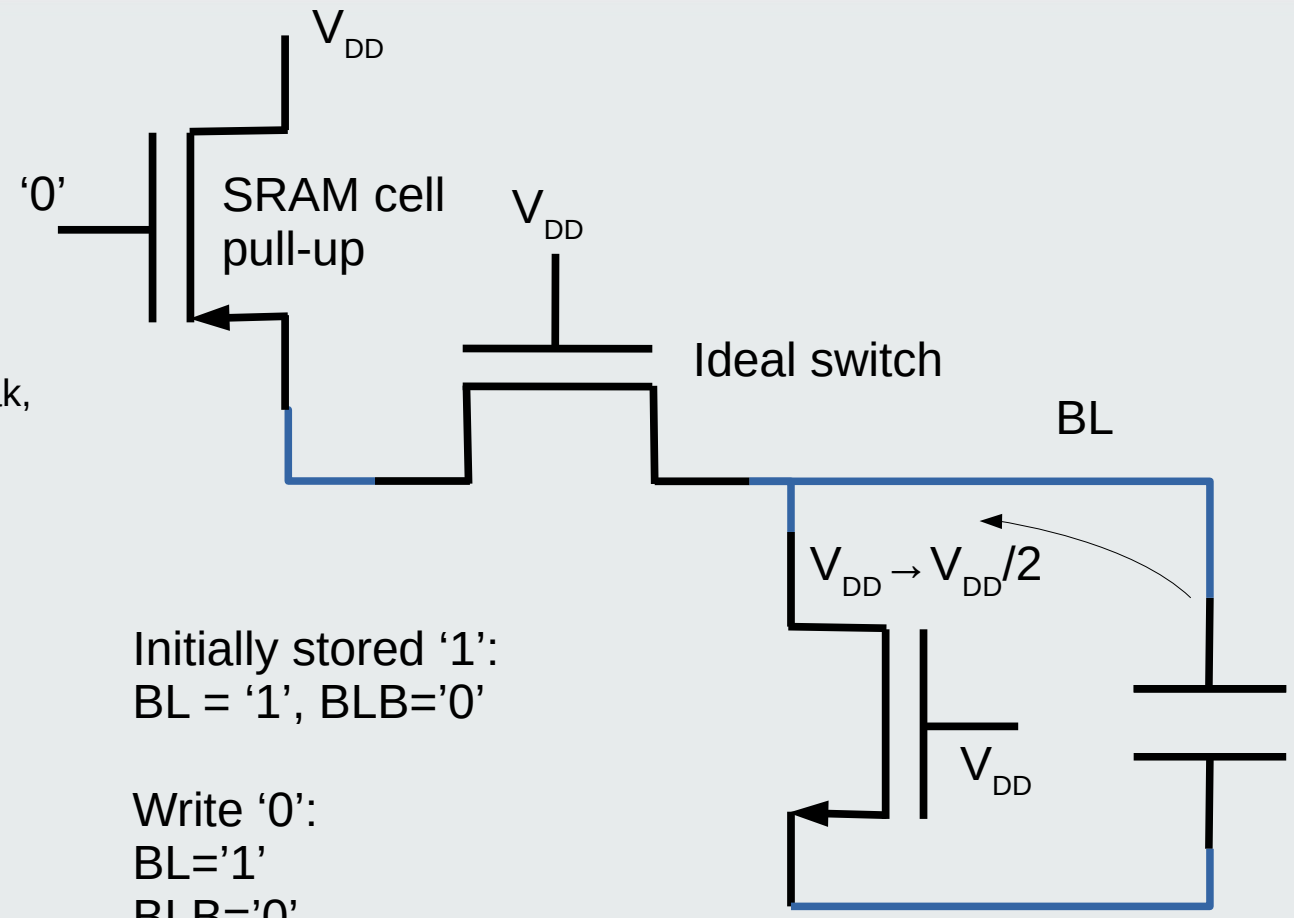
1. Pre-charge BL and BLB at the same voltage VDD
2. Turn on the access transistors (row decoder)
3. Wait for a voltage difference to develop between BL and BLB
4. Select the column (column decoder) to access the (shared) sense amplifier and wait for voltage levels to be restored
5. Read the SRAM data IO pins

SRAM write operation



SRAM write circuit

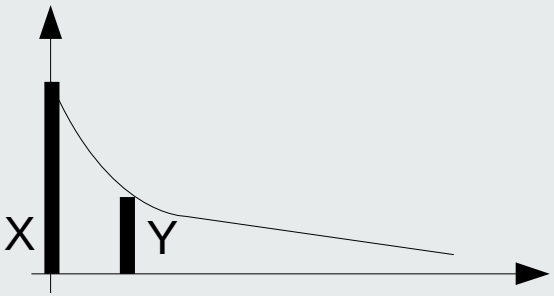
- Pre-charge BLB at VDD
- Turn on the access switch (row)
- Apply write amp (column)
- BL discharges slowly via cell
- BLB discharges fast via write transistor
- Simple model: write transistor is resistor Ra, cell transistor too weak, ideal switch



$$\Delta t = R_A C_D \ln\left(\frac{V_{DD}}{V_{DD}/2}\right) = R_A C_D \ln(2)$$

Initially stored '1':
BL = '1', BLB='0'

Write '0':
BL='1'
BLB='0'

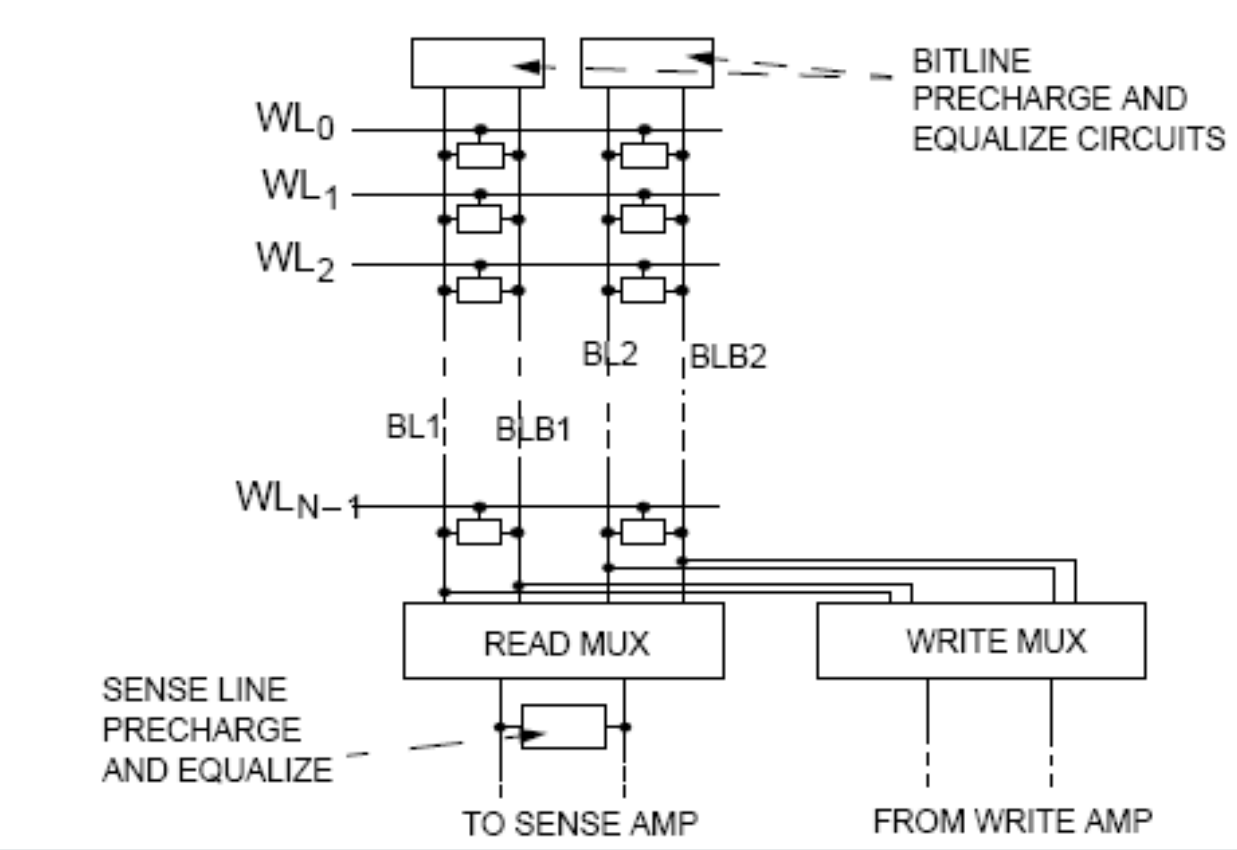


Δt = RC ln(X/Y)

SRAM write procedure

1. Pre-charge BL and BLB at VDD
2. Apply the write values to the chip IO pins
3. Select the row to provide an electrical access to the cell
4. Select the column so that the (shared) write amplifier will drive and force the cell to the desired state

Shared sense and write amps



SRAM write amplifier

- Use pre-charge facility already in place for reading
- Use simple pull-down transistors for writing
- If pre-charge value is VDD then only one line needs to be pulled down!