TÉCNICO LISBOA

Computer Electronics

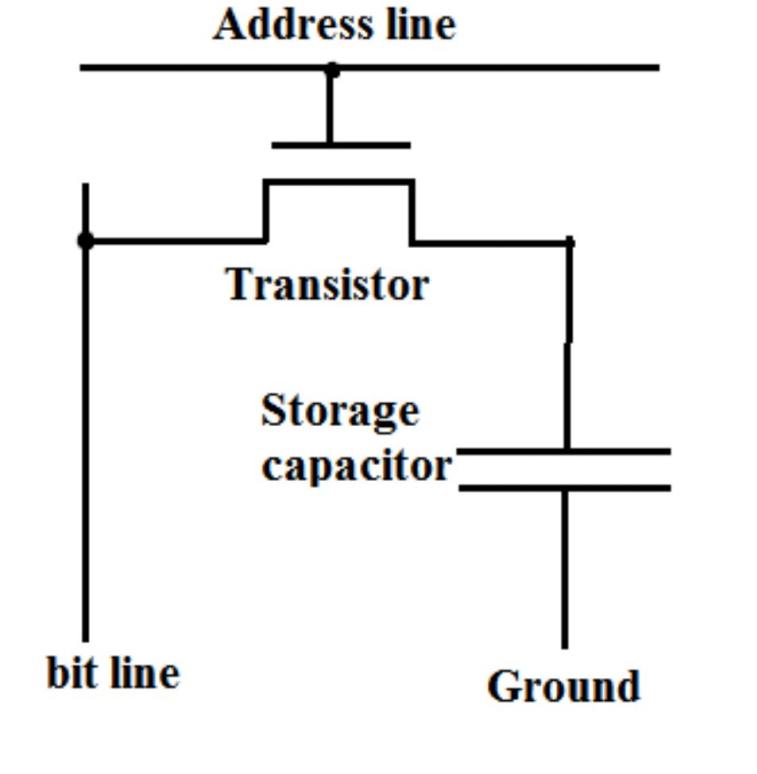
Lecture 17: Dynamic Random Access Memory (DRAM)

TÉCNICO LISBOA

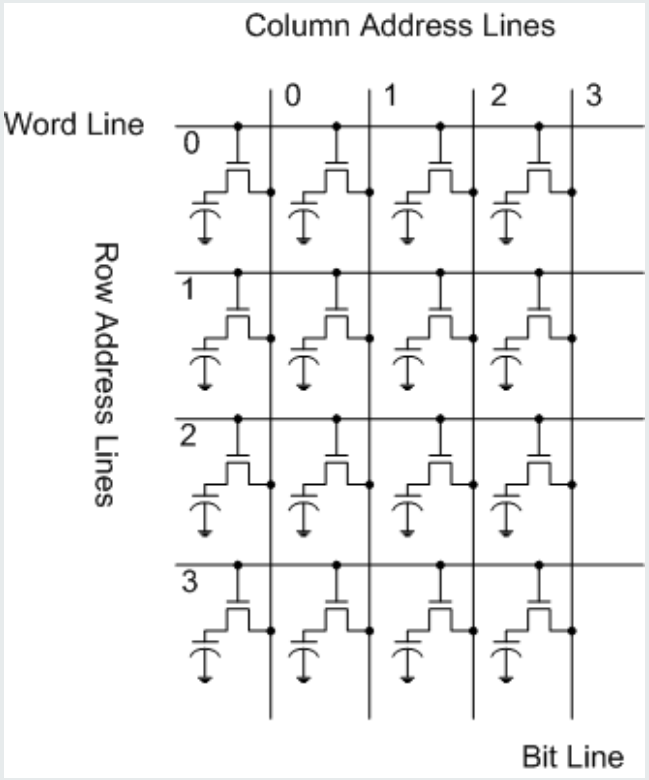
Outline

- DRAM cell
- DRAM matrix
- DRAM read
- DRAM write
- DRAM high-level operation
- DRAM module organization
- DRAM refresh
- Real DRAM chips

DRAM Cell

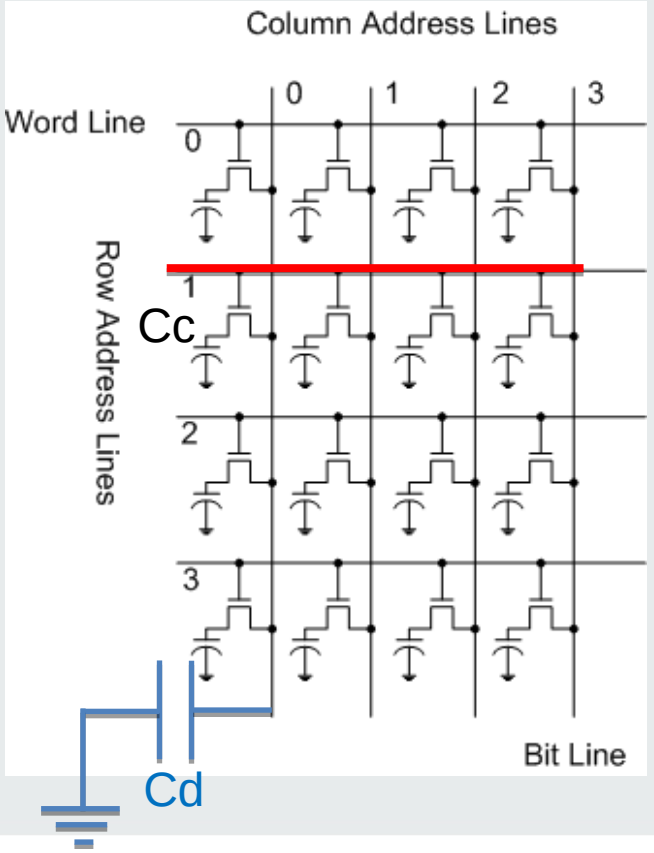

Address line
Transistor
Storage
capacitor
bit line
Ground

DRAM cell matrix

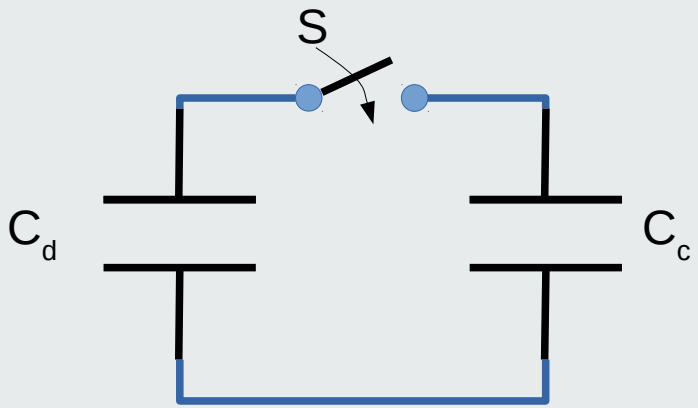


DRAM Reading problem

- Select Row using address
- Cell charge has little effect on line voltage Vd because Cc << Cd
- Final voltage $V = \frac{C_d}{C_c + C_d} V_d + \frac{C_c}{C_c + C_d} V_c$
- For Cc=40fF, Cd=1pF, Vc=5V then the variation in Vd is only 200mV
- Since the transistors leak current, then variation is even smaller
- Difficult to detect this small variation!



Charge redistribution



Switch closes at time t=0

Charge is conserved

$$Q(t=\infty)=Q(t<0)$$

$$Q=CV$$

$$C_d V_d+C_c V_c=(C_c+C_d)V(t=\infty)$$

$$V=\frac{C_d}{C_c+C_d}V_d+\frac{C_c}{C_c+C_d}V_c$$

Energy NOT conserved: part of it is dissipated in the switch S (resistance Rs)

$$E=\frac{1}{2}CV^2$$

$$E(t<0)=\frac{1}{2}C_d V_d^2+\frac{1}{2}C_c V_c^2$$

$$E(t=\infty)=\frac{1}{2}(C_d+C_c)V^2(\infty)$$

$$E(t=\infty)=\frac{1}{2}(C_d+C_c)\left(\frac{C_d}{C_c+C_d}V_d+\frac{C_c}{C_c+C_d}V_c\right)^2$$

$$E(t=\infty)=\frac{1}{2}\frac{C_d^2}{C_d+C_c}V_d^2+\frac{C_d C_c}{C_d+C_c}V_d V_c+\frac{1}{2}\frac{C_c^2}{C_d+C_c}V_c^2$$

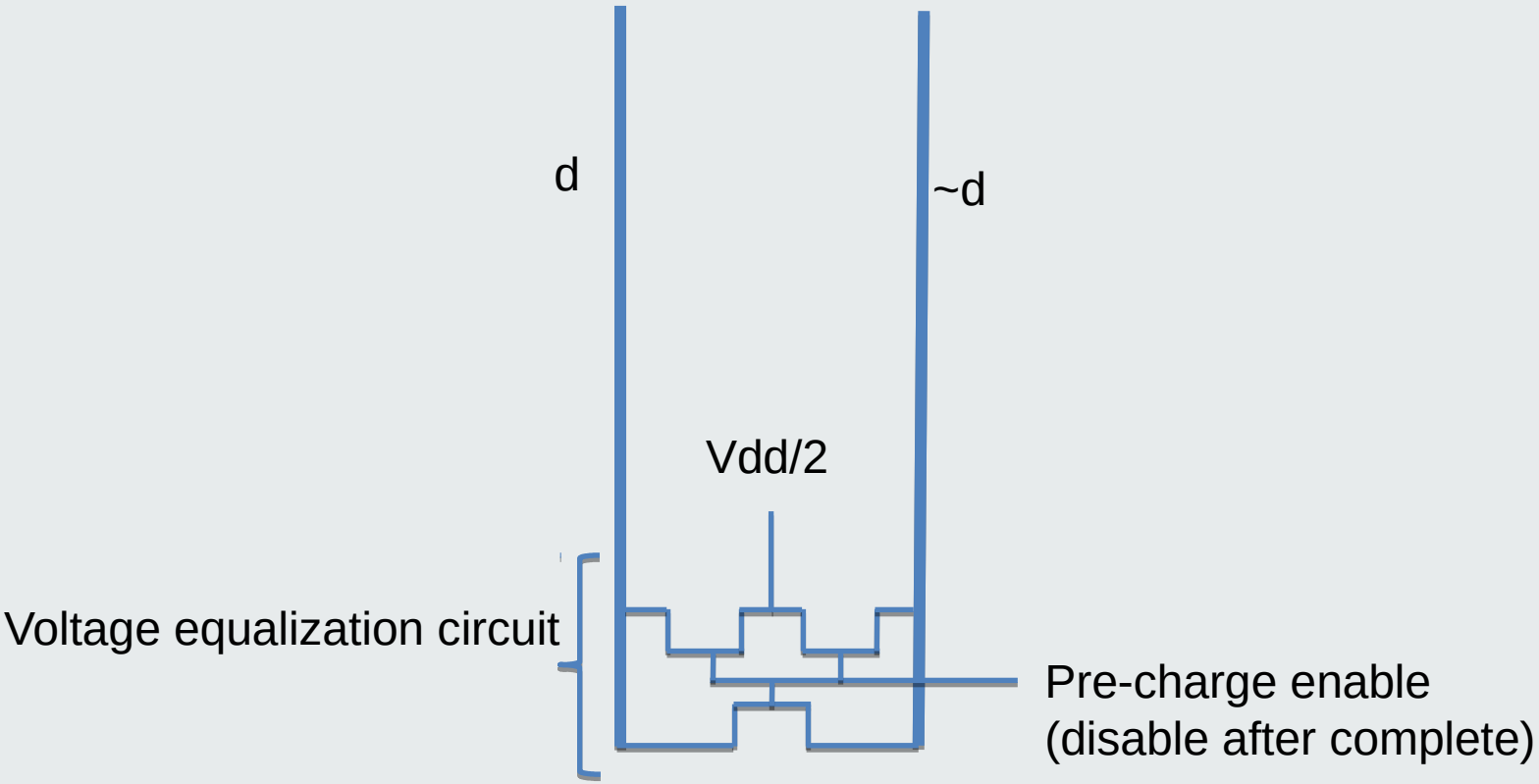
$$E(t<0)>E(t=\infty)$$

$$V(t)=V(\infty)+\left[\frac{VDD}{2}-V(\infty)\right]e^{\frac{-t}{R_s\frac{C_d C_c}{(C_d+C_c)}}}$$

Solving the read problem

- Use complementary column bit lines to store d and ~d (doubles circuit area, not necessary but eases explanation)
- Pre-charge the bit lines at Vdd/2
- Select row and cells will drive bit lines
  - Vd=Vdd/2+ΔV/2 and V~d=Vdd/2-ΔV/2
- Amplify ΔV using sense amp
- Select column to read data

Pre-charge complementary bit lines



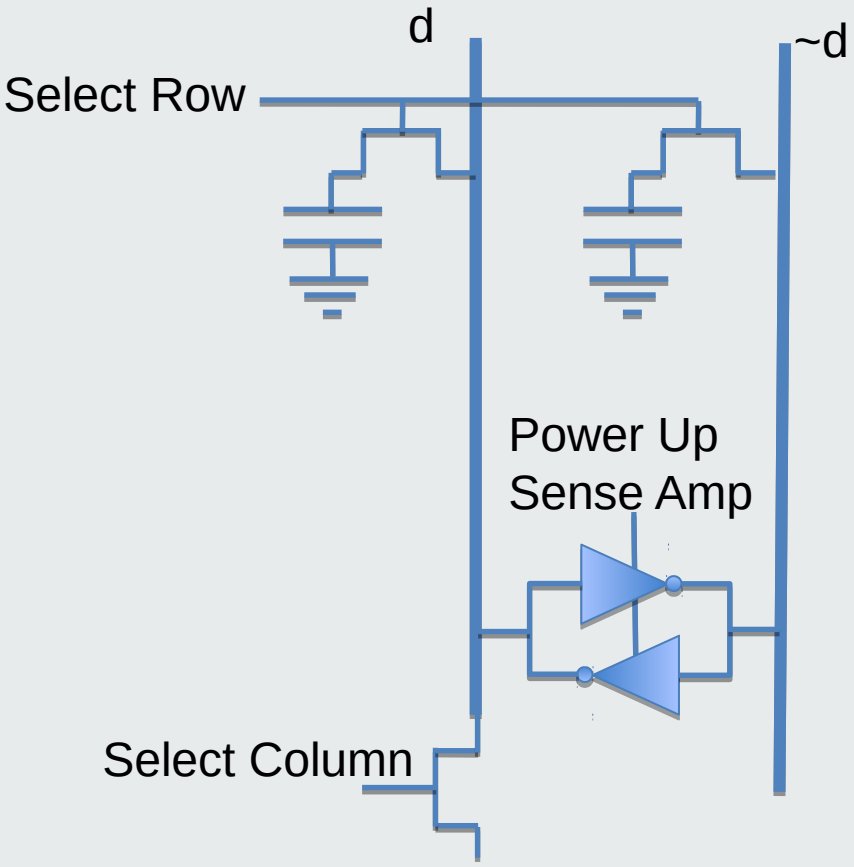
Select row, sense and read

- Select row to drive bit lines

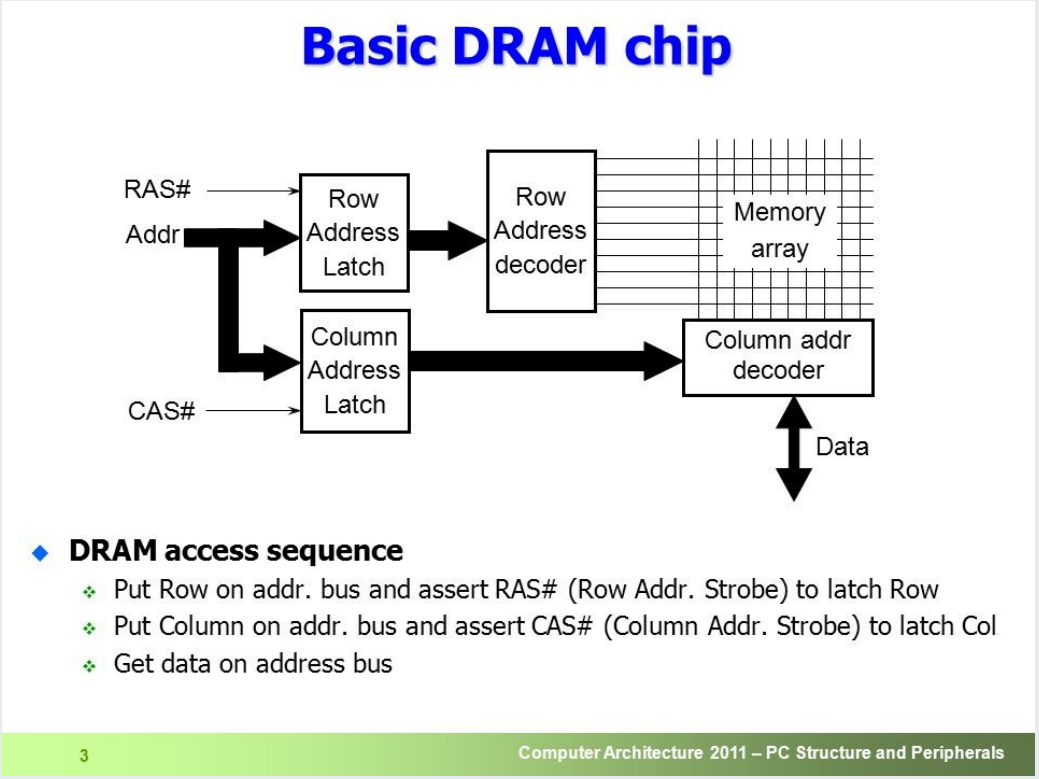
  Vd=Vdd/2+ΔV/2

  V~d=Vdd/2-ΔV/2

- Amplify ΔV using sense amp – This also restores the cells!
- Select column to read data



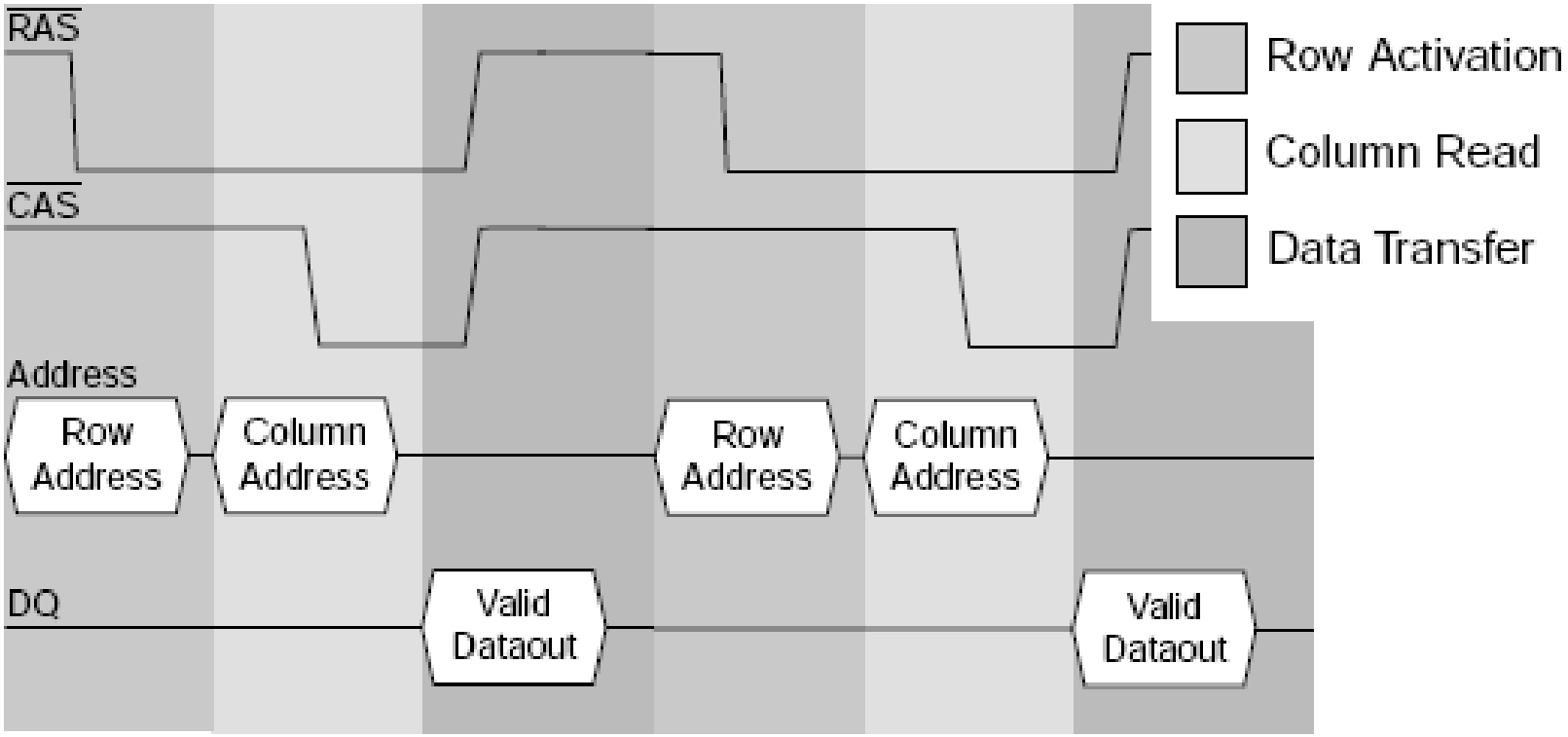
DRAM high-level view



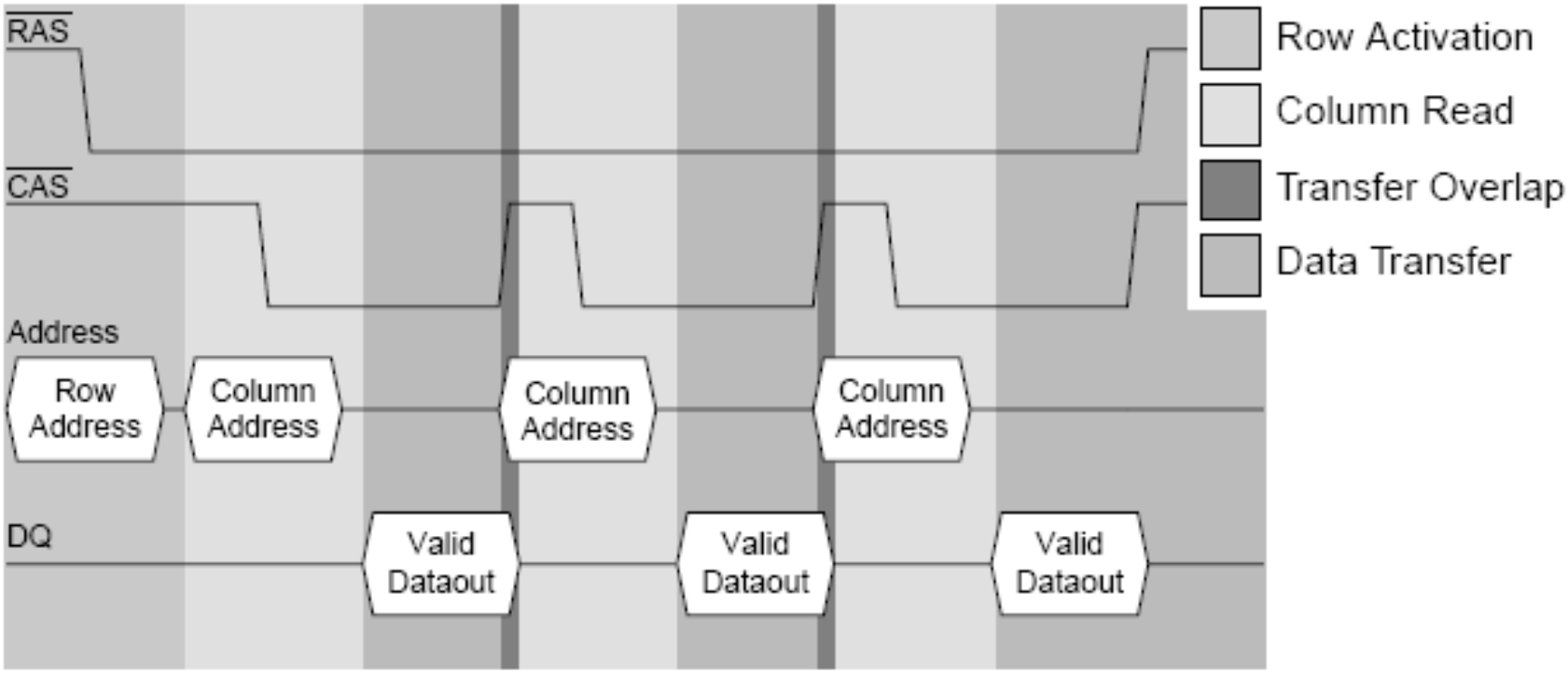
Example:

- 1024 x 1024 mem array
- 20 address bits
- Only 10 address pins
- Send row address
- Then send column address

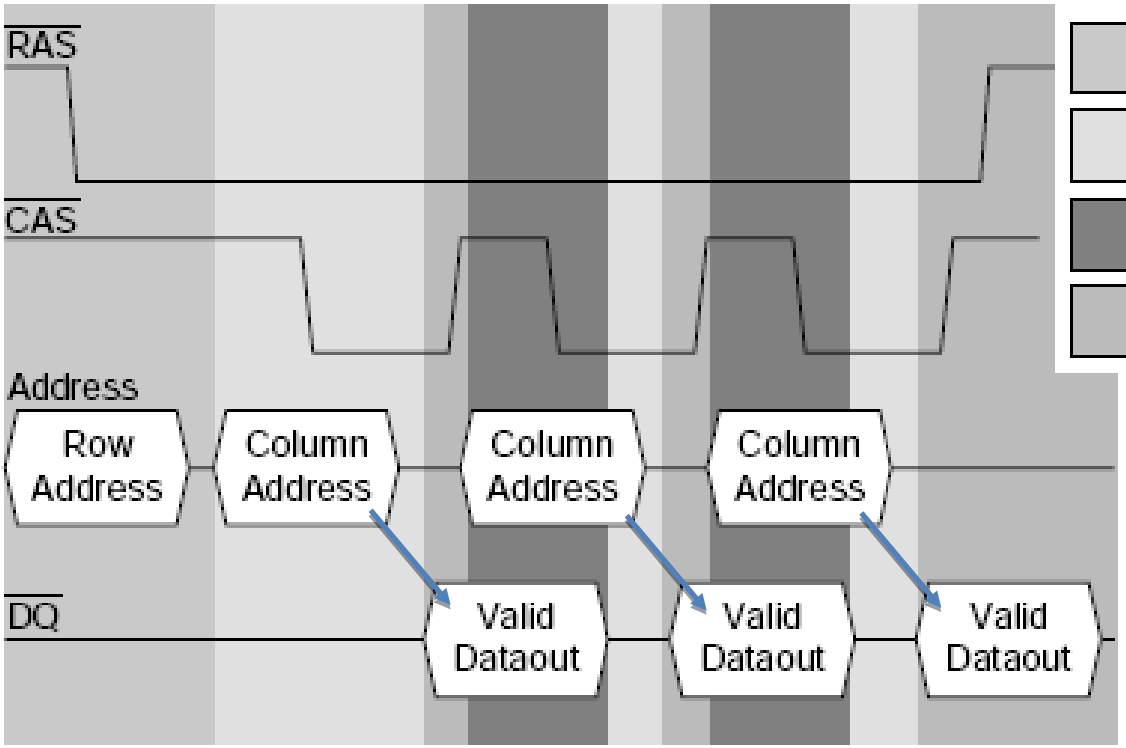
DRAM timing diagram



DRAM fast page mode



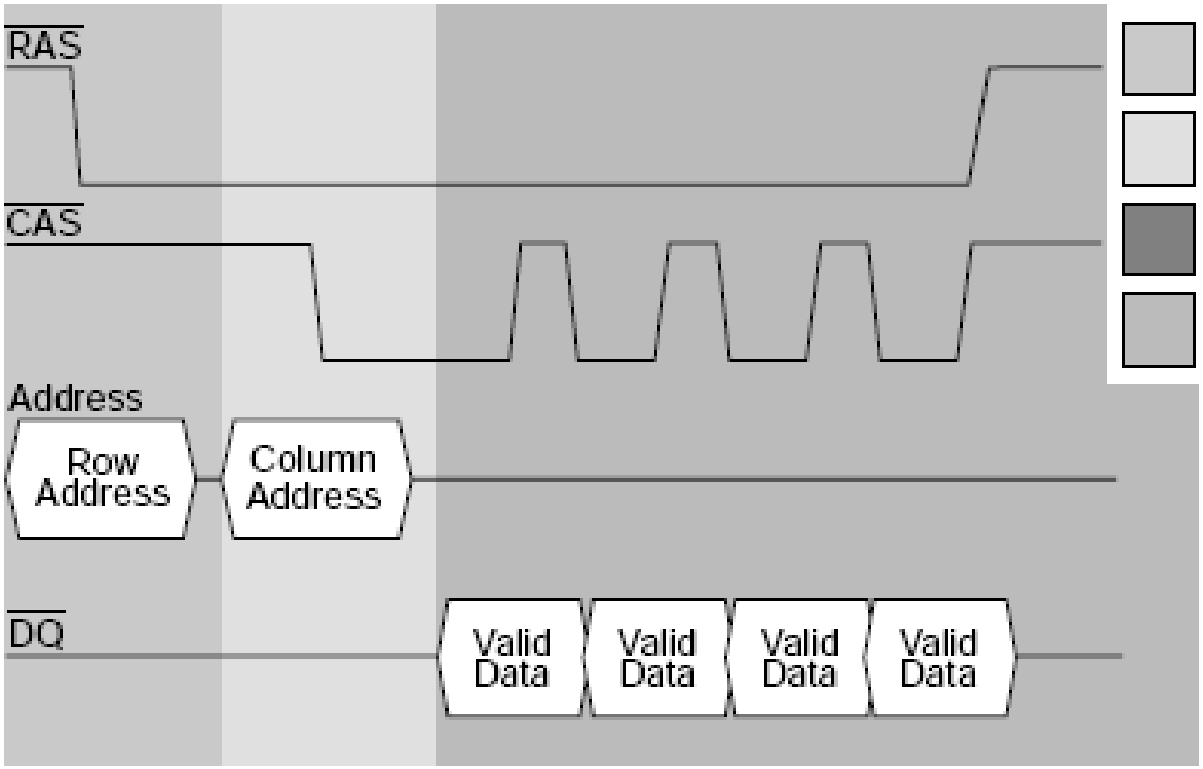
DRAM Extended Data Output (EDO)



Uses register to hold previously read data while new data is read

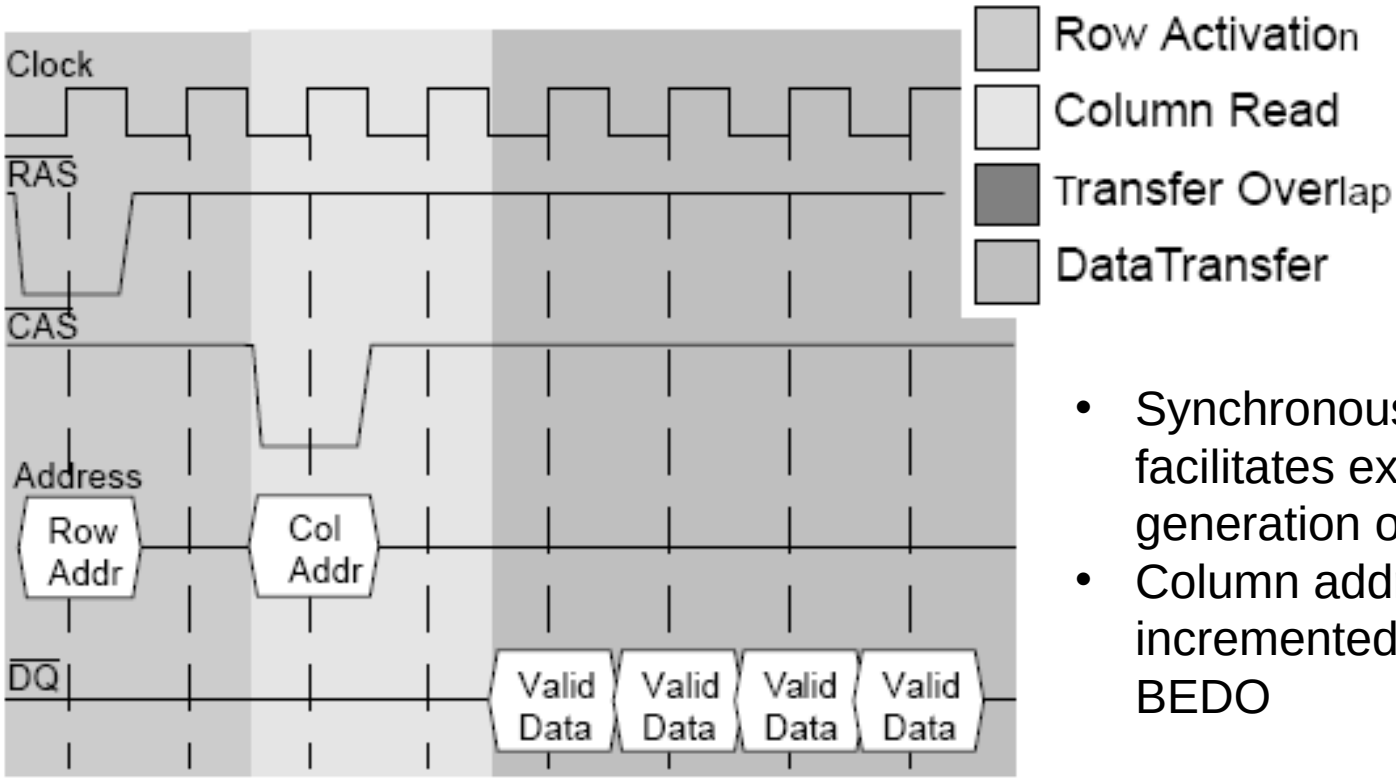
Pipelined access!

Burst Extended Data Output (BEDO)



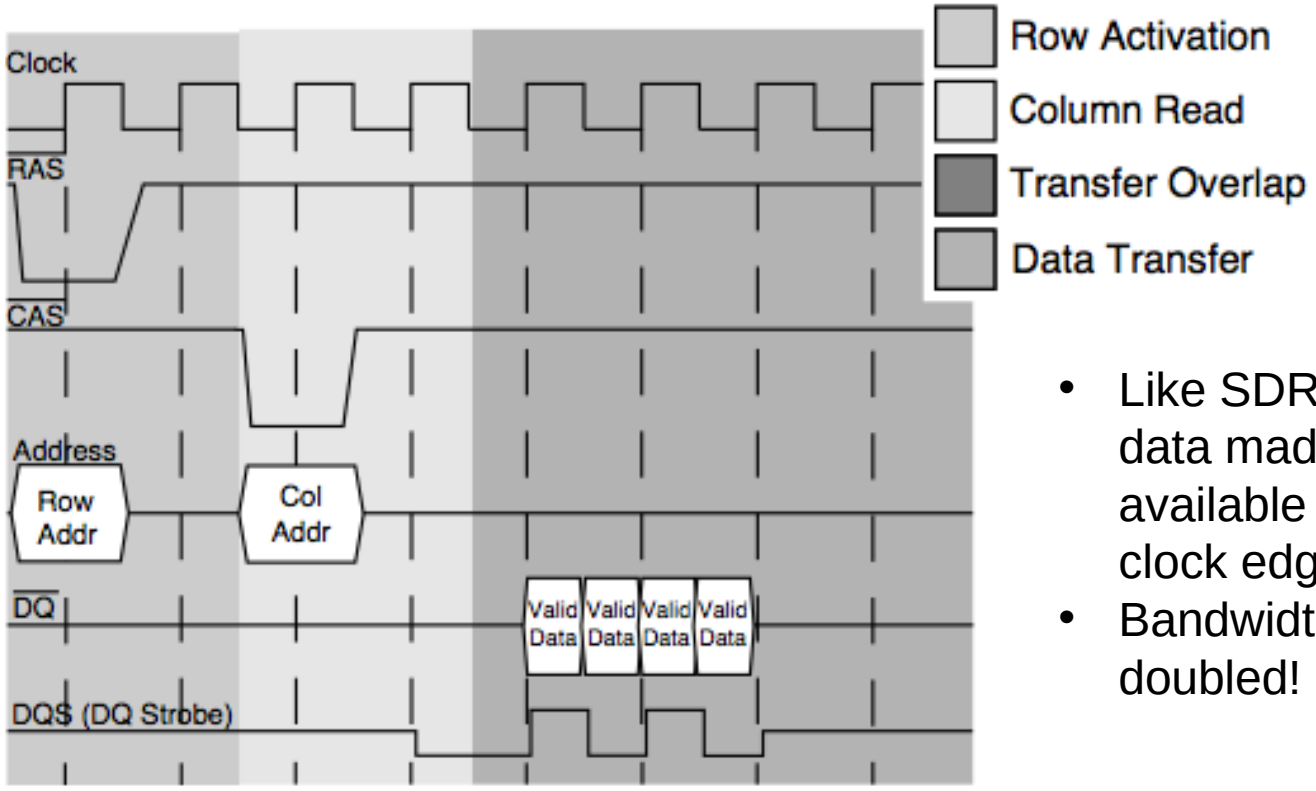
Column address is incremented internally for greater speed!

Synchronous (SDRAM)



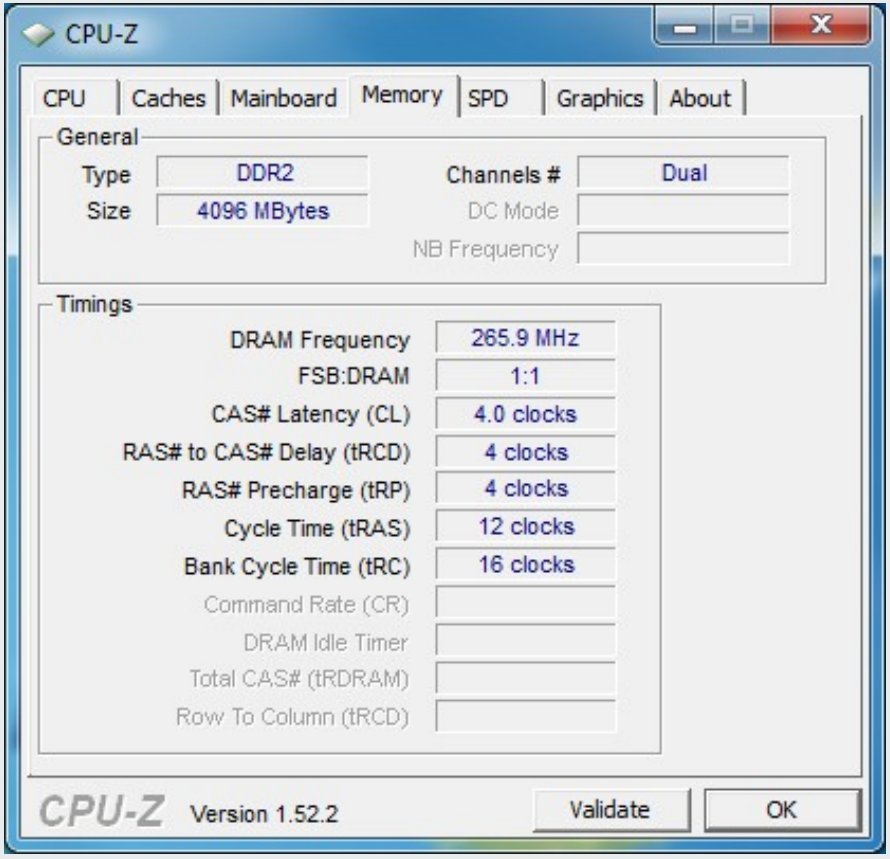
- Synchronous operation facilitates external generation of signals
- Column address still incremented internally like BEDO

Double Data Rate (DDR)



- Like SDRAM but data made available at both clock edges
- Bandwidth is doubled!

Configuring CPU to use some DRAM

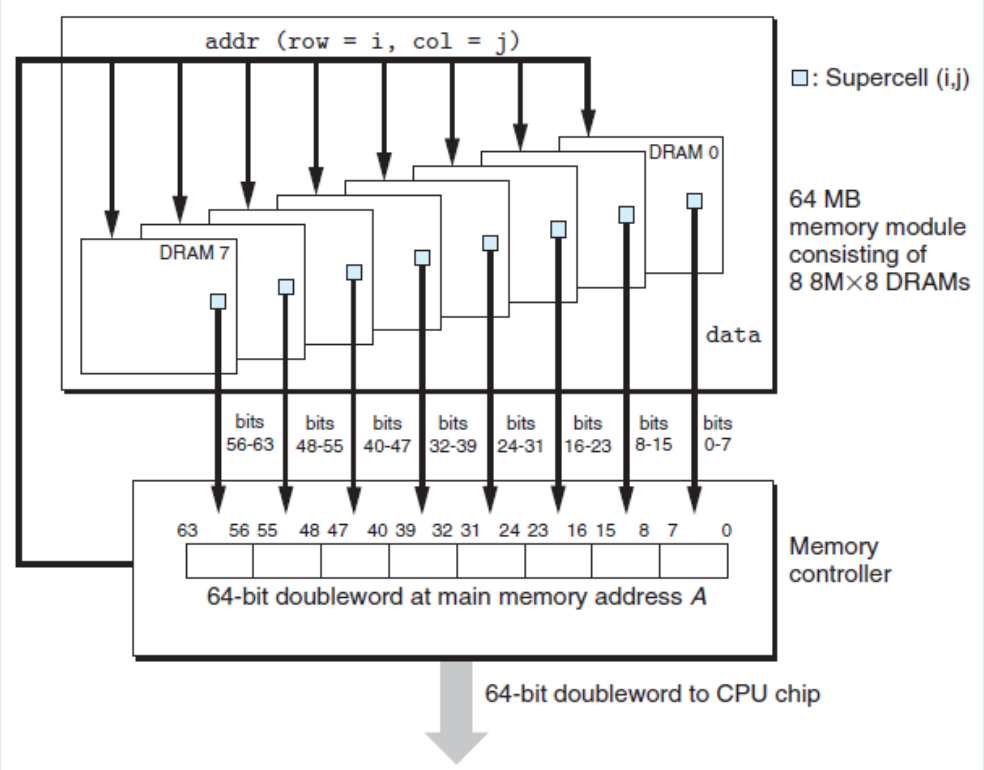


BASIC COMMANDS

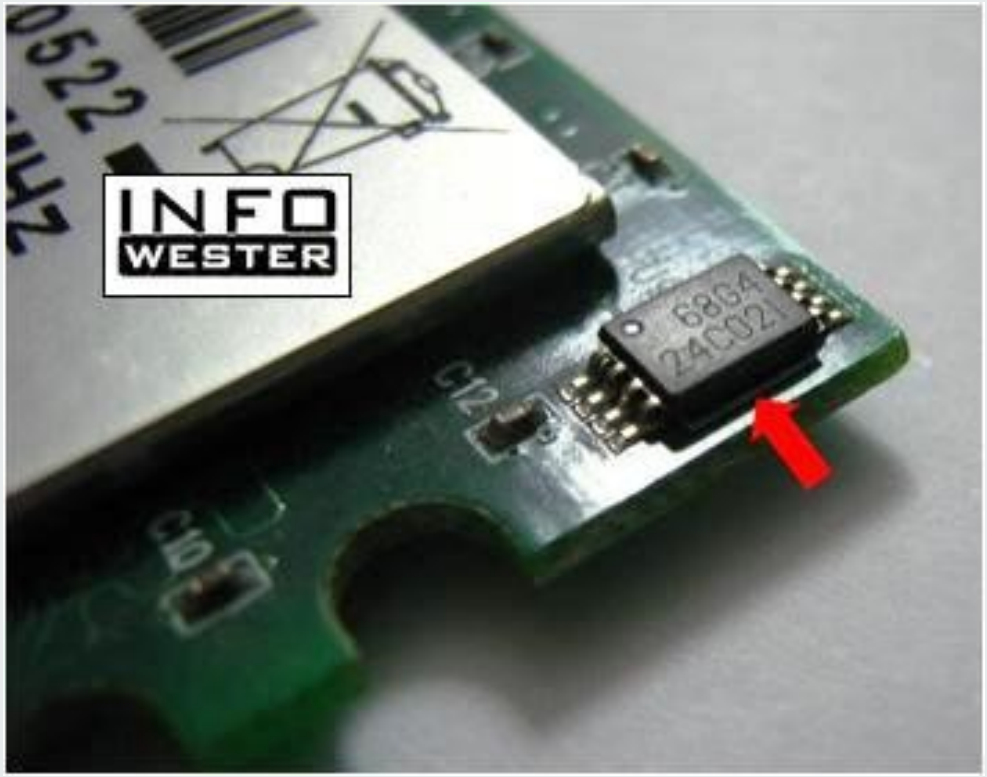
- Next row precharge
- Activate row
- Activate column
- Read/Write data

- tRP: precharge time new row
- tRCD: RAS to CAS delay
- tCL: CAS to data delay
- tRAS = tRCD+2tCL
- tRC = tRAS+tRP

Memory module organization



Serial presence detect



- Modules have a small chip to inform whether they are present
- Useful in Power On Self Test (POST)

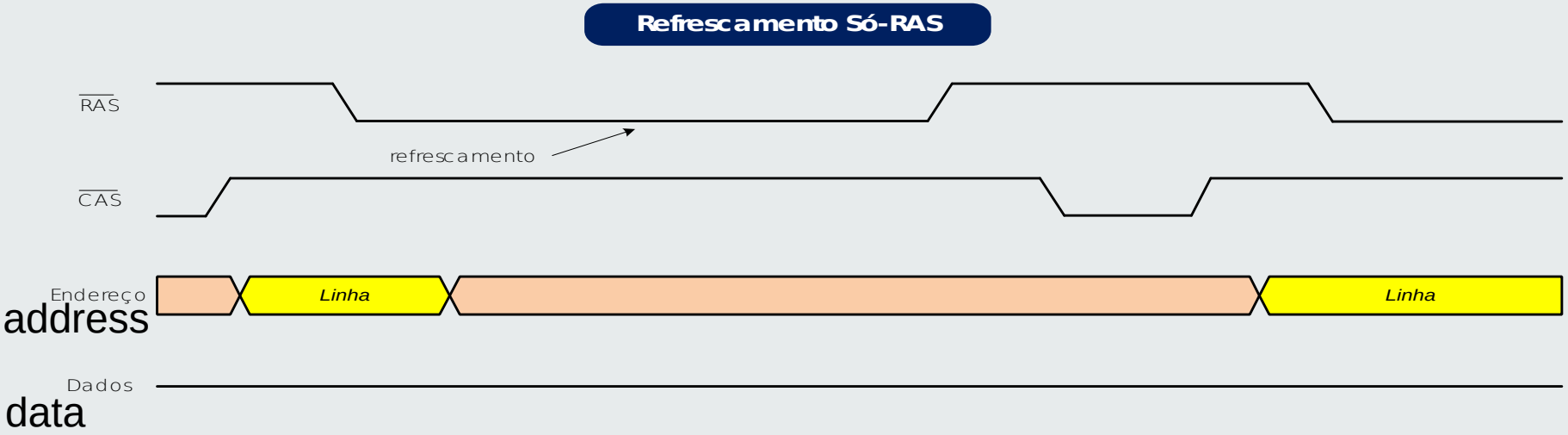
DRAM refreshing

- Cell transistors leak and lose charge
- Cell needs refreshing before stored info is lost
- When a cell is read it is restored (refreshed)

DRAM refresh modes

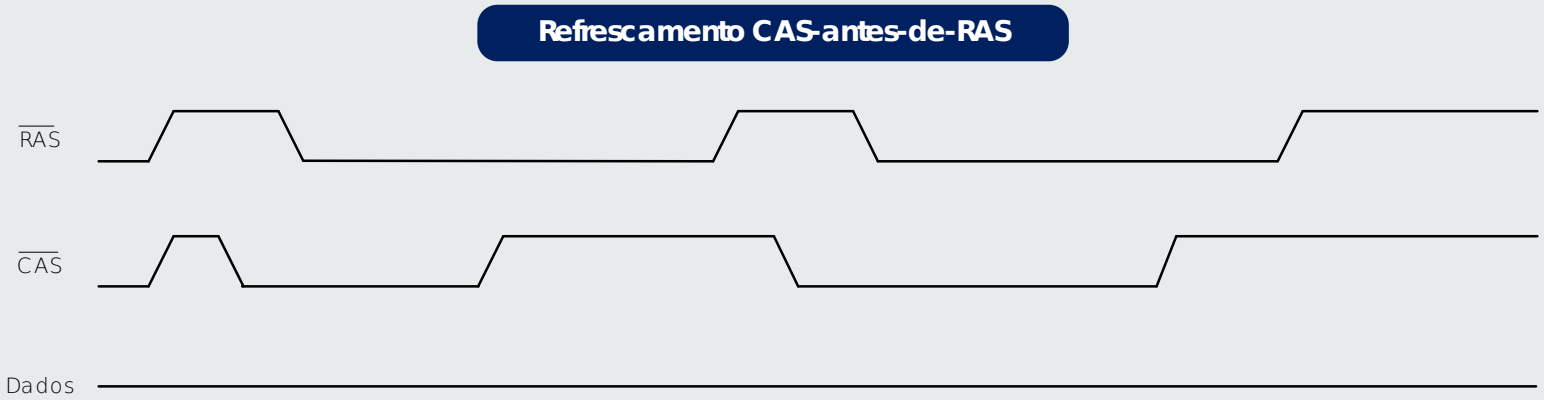
- RAS only
- CAS before RAS
- Hidden

RAS only refresh



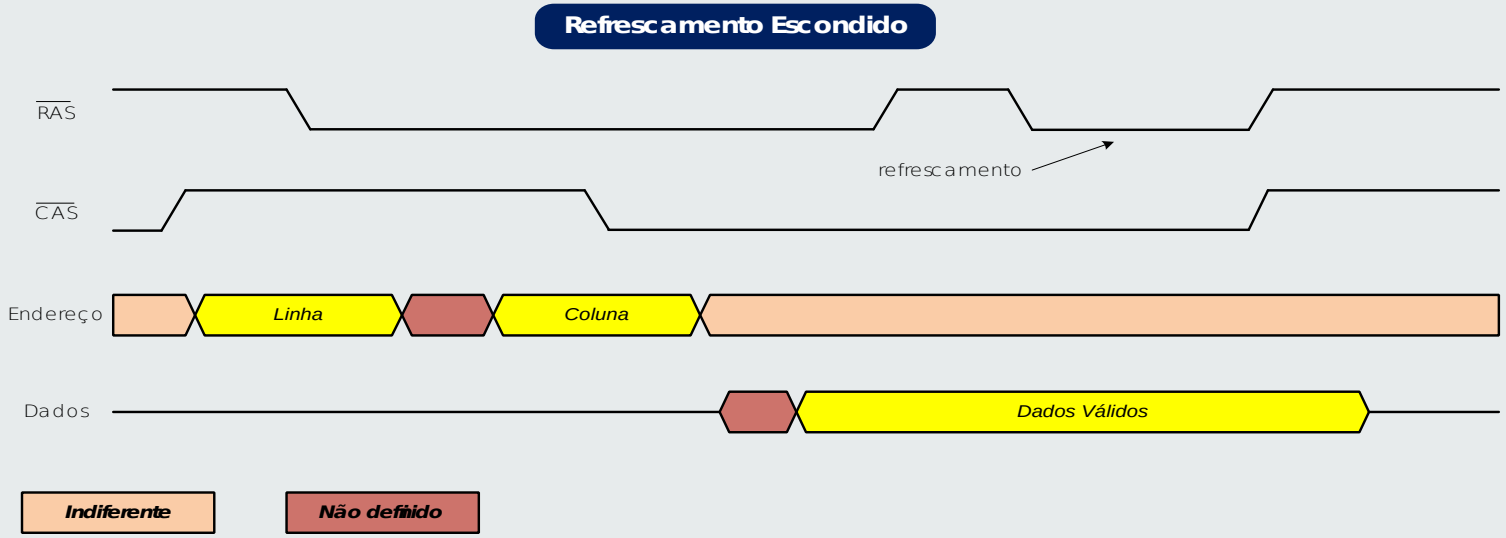
- Provide Row address and activate RAS
- No need to activate CAS

CAS before RAS refresh



- No need to provide Row address (incremented internally)
- This is signaled by activating CAS before RAS

Hidden refresh



- Performs refresh *while* data is output
- Reduces refresh overhead

Refresh overhead

- Refresh interval: every row must be refreshed within this interval
- Refresh time: time to refresh all rows
- Overhead = refresh time/refresh interval