MARVELL™

SpicaPlus: Line Side Receiver

Receiver Types

Digital DSP	Analog
PKR50 (Polaris/Vega/Atlas)	PSR
PKR100 (Porrima/Alcor)	Sun/Sun II
Syrma IP (PKR50)	PMR
Capella IP (PKR100)	POR (SpicaA)

- Digital DSP receivers have longer reach but at expense of higher power
- Analog receivers have complex software (ignoring the complexity of AN/LT)

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Different Receivers on Different Designs

- We use different receivers depending on what market is being targeted.
- Lowest power is critical so sometimes we don’t want to put a digital receiver on both sides of the device.

Device	Host	Line
Polaris/Atlas	PSR	PKR50
Vega	PKR50	PKR50
Porrima/Alcor	PSR	PKR100
STC	Sun	Syrma
CTC	Capella (PKR100)	Capella
Mira (Skywalker)	Syrma (PKR50)	Capella
Mira (Polaris II)	Sun II	Syrma
SpicaA	PMR	POR
PG3	Sun II	POR
Spica+	PMR	Capella
PG4	Sun II	Capella
Spica5	Capella	Capella

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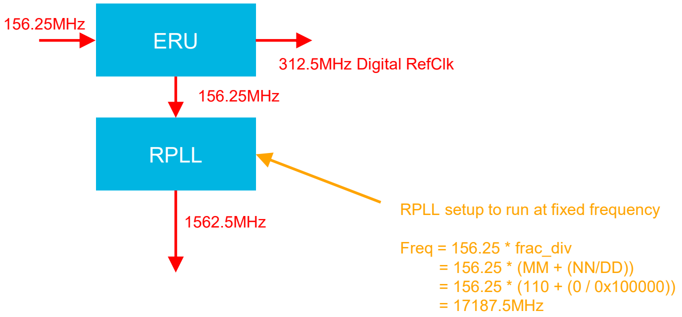
RX Overview – ERU + RPLL



156.25MHz

ERU

312.5MHz Digital RefClk

156.25MHz

RPLL

1562.5MHz

RPLL setup to run at fixed frequency

Freq = 156.25 * frac_div
= 156.25 * (MM + (NN/DD))
= 156.25 * (110 + (0 / 0x100000))
= 17187.5MHz

- ERU = ESD Reference Unit
  - Provides
    - analog reference clock
    - digital reference clock(s)
      - 156.25 or 312.5MHz
- RPLL = Reference PLL
  - Generates the 1.5625GHz clock required for the System PLLs (SPLL)
  - System PLLs need a higher reference clock to achieve 28GHz speeds
    - Older devices like Syrma could use 156.25MHz ref but this is not fast enough for 28GHz VCO speeds.

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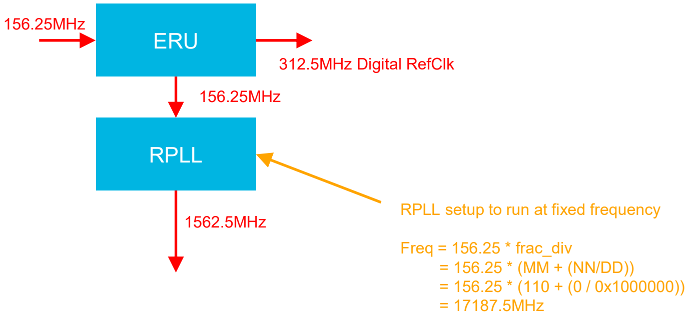
RX Overview – ERU + RPLL



RPLL setup to run at fixed frequency

Freq = 156.25 * frac_div
= 156.25 * (MM + (NN/DD))
= 156.25 * (110 + (0 / 0x1000000))
= 17187.5MHz

- PLL Divider Configuration
  - DD = Fixed divider of 0x1000000
    - PLLD_FBDSM_CFG4-7
  - MM = Integer divide portion
    - PLLD_FBDSM_CFG8
  - NN = Fractional divide portion
    - PLLD_FBDSM_CFG0-3

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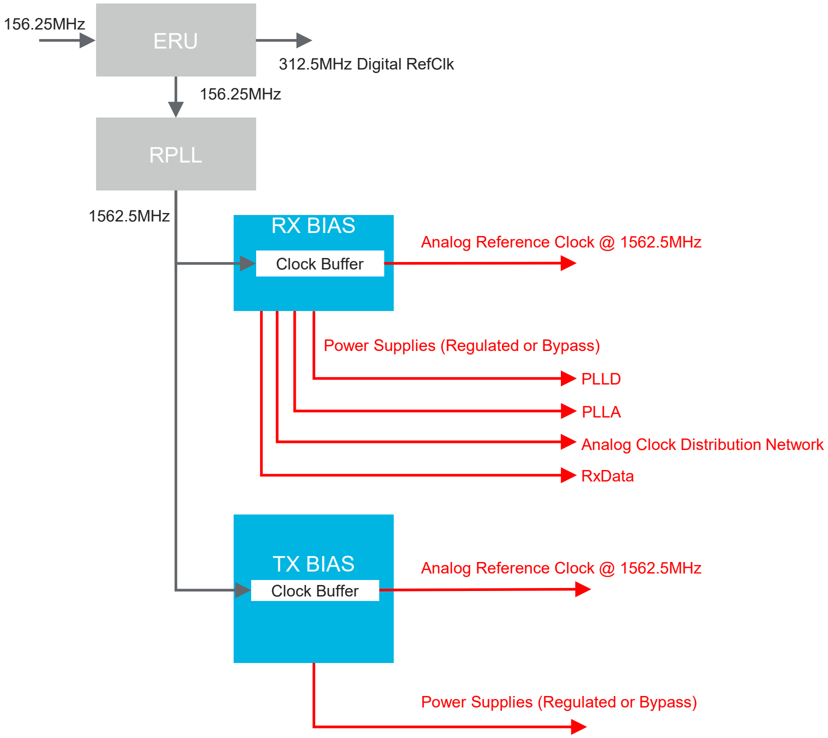
RX Overview – Bias/RefGen Blocks


156.25MHz
ERU
312.5MHz Digital RefClk
156.25MHz
RPLL
1562.5MHz
RX BIAS
Clock Buffer
Analog Reference Clock @ 1562.5MHz
Power Supplies (Regulated or Bypass)
PLLD
PLLA
Analog Clock Distribution Network
RxData
TX BIAS
Clock Buffer
Analog Reference Clock @ 1562.5MHz
Power Supplies (Regulated or Bypass)

- The BIAS blocks are responsible for:
  - Buffering the analog reference clock throughout the chip
  - Providing the individual supplies to different blocks of the chip
    - Each LDO can be regulated or pass-thru/bypassed
    - LDO = Low Dropout Regulator
- Bias/RefGen operates in bypass mode on Spica+
  - Workaround for low temperature h/w bug found on SpicaA (h/w bug fixed in Spica+)

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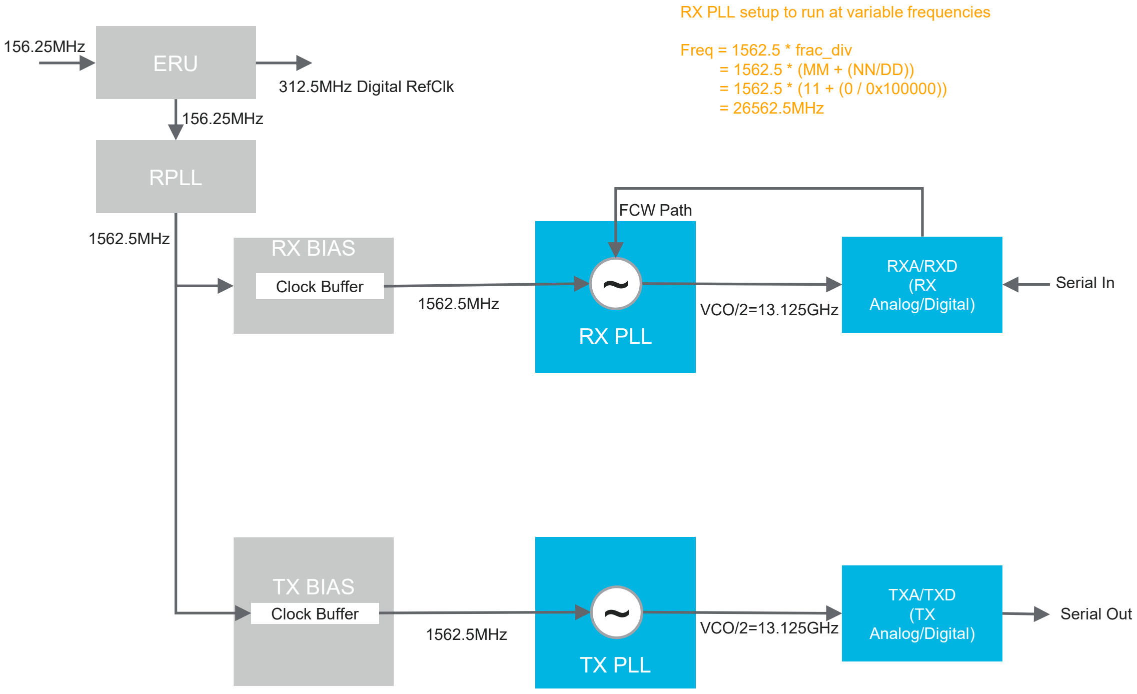
RX Diagram – SPLLs



- RX and TX SPLLs multiply the reference clock to the 28GBaud range and supply a divided down clock to the RXA/TXA blocks.
- The RXA and TXA sample on the rising/falling edge of the VCO clock from the SPLLs in order to RX/TX.
- RX has feedback path to speed up/slow down VCO to match recovered clock from serial data path

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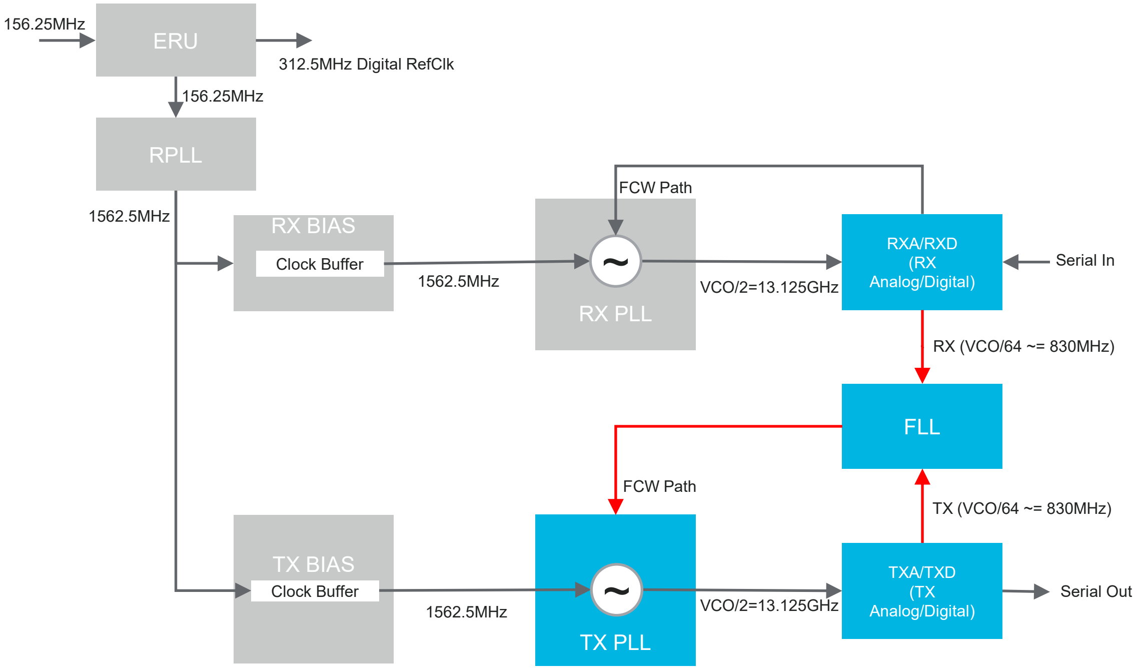
RX Diagram – FLL



- The FLL compares the recovered RX clock and the TX clock
- Uses feedback path to the TX PLL to speed up/slow down the TX VCO to match recovered RX clock

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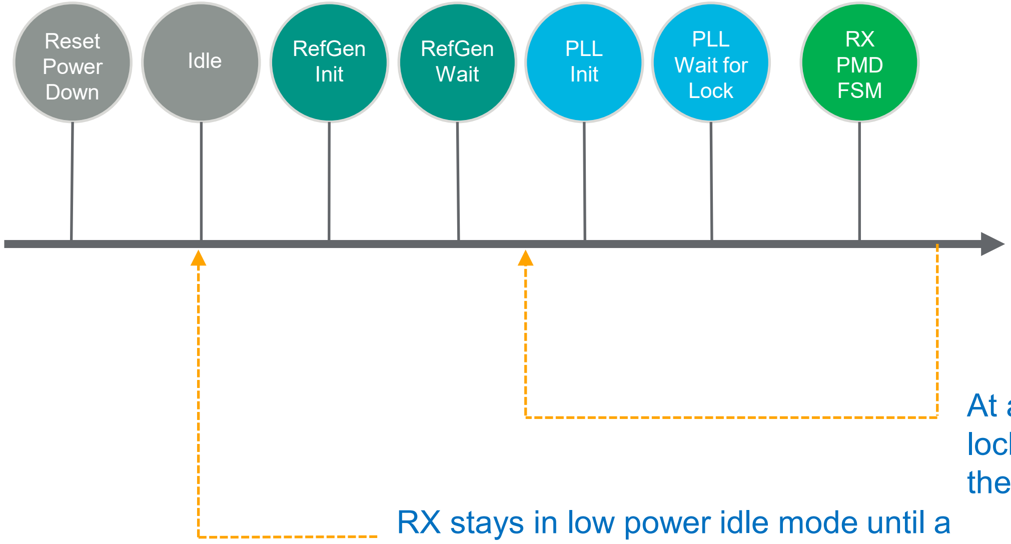
Top Level RX FSM



At any point if f/w detects loss of PLL lock it will jump back and re-configure the PLL

RX stays in low power idle mode until a request comes from the API to enable channel

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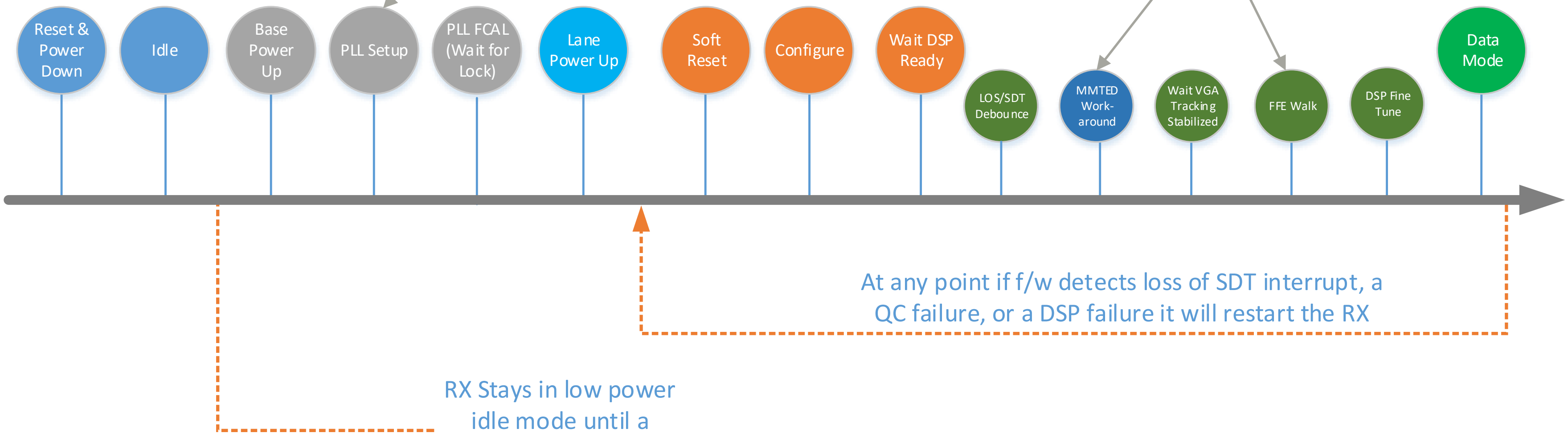
RX PMD FSM



Moving towards configuring this outside of PMD FSM

MMTED workaround only on CapellaB, Spica+, Mira

At any point if f/w detects loss of SDT interrupt, a QC failure, or a DSP failure it will restart the RX

RX Stays in low power idle mode until a request comes from the API

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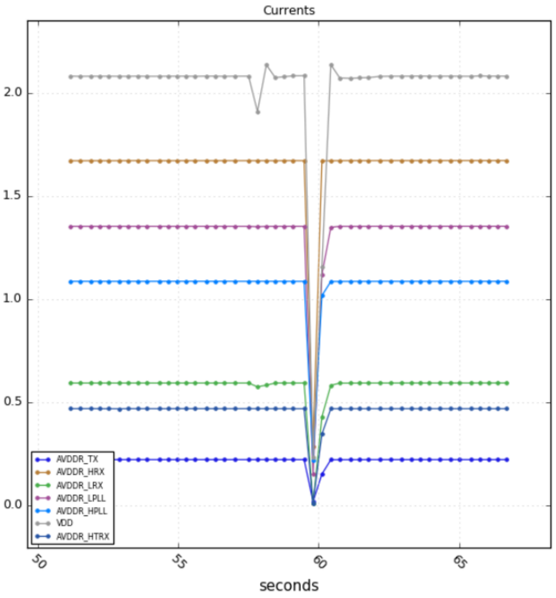
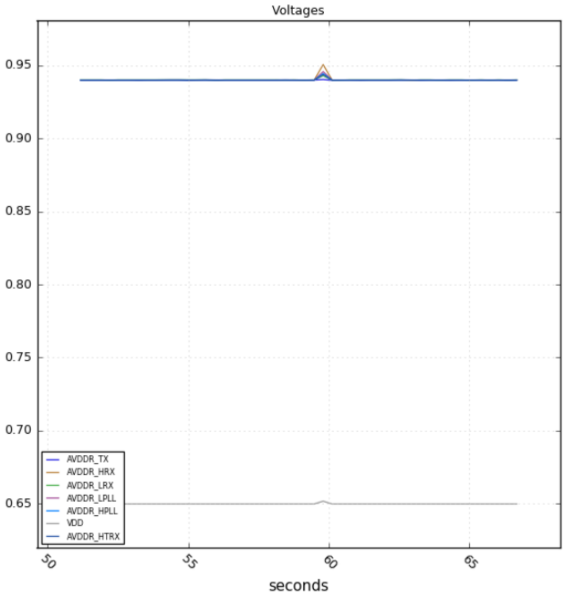
Flow works but not perfect

- The way we power things up on Spica+ is not perfect. There is a huge swing in power when configuring/re-configuring the device!





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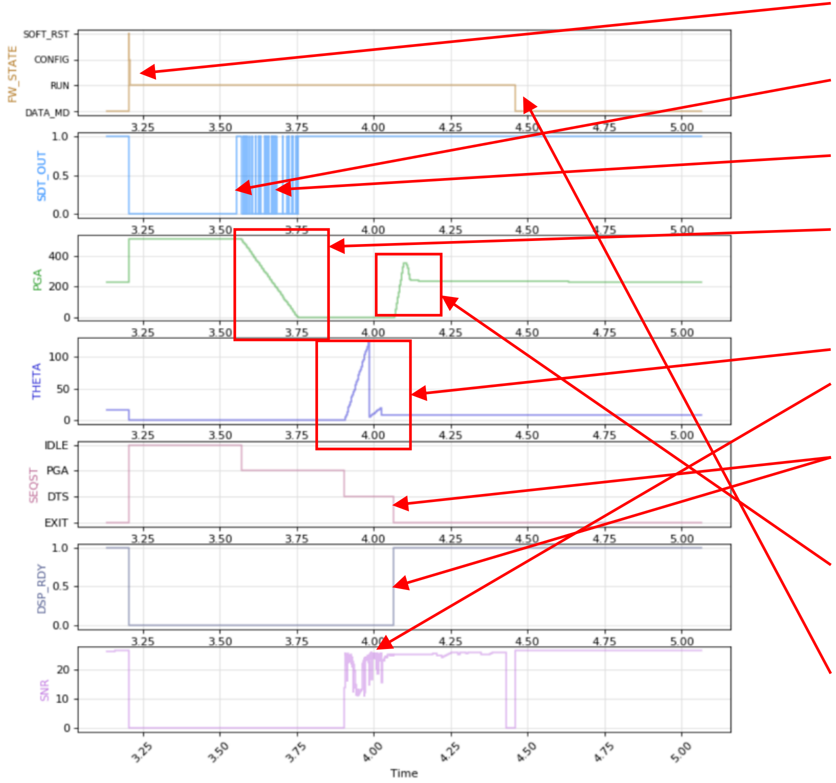
A Typical RX Flow (Animated)



Firmware soft resets the RX, re-configures, waits for SDT_OUT

Firmware waits for SDT_OUT and then starts h/w STM

SDT_OUT will toggle when the PGA FSM is running so it must be ignored.

PGA FSM – find optimal gain such that ADC samples use full swing

Theta Sweep – find the center of the eye by sweeping the phase and searching for the best SNR.

Hardware STM declares completion by asserting DSP_READY and moves to EXIT state. Still lots of stuff to do in f/w.

MMTED Fix - Use VGA tracking to restore ADC Envelope

Firmware does QC check and advances to Data Mode

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Important RX Registers

Register	Description
LANE_SEQUENCER_MANUAL_CFG.MAN_INIT_DONE	Holds the DSP clock while configuring the device
SIGNAL_DETECT_STATUS.SDT_OUT	Whether hardware has signal detect
STM_MIRROR_STATUS	Mirror of the STM status registers (accessible even when STM_ENABLE==1)
STM_MIRROR_STATUS.DSP_READY	The hardware STM has completed RX bringup
DSP_STM_ENABLE_CFG.DSP_STM_EN	Controls ownership of the hardware STM registers
DSP_STM_RESET_CFG	Controls the reset of the individual blocks in the DSP
RX_DSP_INTS/RX_DSP_INT	DSP alarms
RX_DSP_PGA_GAIN_STATUS.PGA_GAIN	The PGA Gain value (0 – 511 where 511 is highest gain)
DSP_STM_DTL_THETA_CFG.DTL_THETA	Theta Code (represents the phase)

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Software Status

Register	Description
RX_FW_STATUS	RX PMD Firmware Status (state, reset count, locked)
RX_FW_INT	Latch firmware interrupts
RX_SNR_VALUE	The RX SNR (still reported in MSE)
RX_QC_STATUS	Status of the RX QC
RX_FFE_WALK_STATUS	MMTED FFE Walk Status

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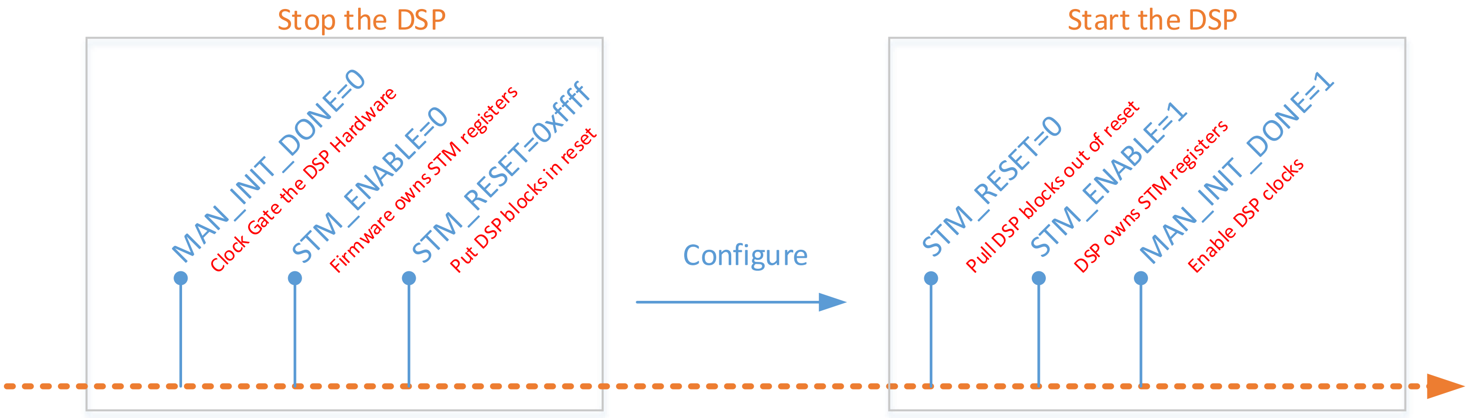
Starting the DSP – Order Matters



- If you set MAN_INIT_DONE=1 after STM_ENABLE=1 when starting the DSP the DSP will start but won't own the STM registers so it won't work!
- The DSP should own the STM registers until DSP_READY is asserted (or it fails)

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NRZ vs PAM

- Mode is configured in the PAMX_MODE field in the DSP_MODE_CONTROL_CFG register.
- In addition to setting PAMX_MODE the f/w configures one or more de-mapping registers that control bit ordering:
  - IEEE demap
    - In the original PAM devices we picked the wrong bit ordering when sending out the MSB/LSB.
  - Gray mapping (PAM only)
  - P/N inversion

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DSP Modes

- The hardware supports multiple DSP modes. The most important ones are:
  - SLC1 (Slicer)
  - SLC1_RC_SLC2 (Slicer + Reflection Canceller)
  - DFE1
  - DFE1_RC_DFE2
- The DSP mode is selected via the DSP_MODE_CONTROL register
- DFE modes not typically used on optics

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Advanced DSP Modes

- This modes are available but not often used
  - MPICan – Multi-path interference Canceller
  - LDEQ – Level Dependent Equalizer
  - OIM – Optical Interference Mitigation (Tunable notch filter)
  - MLSD/MLSE

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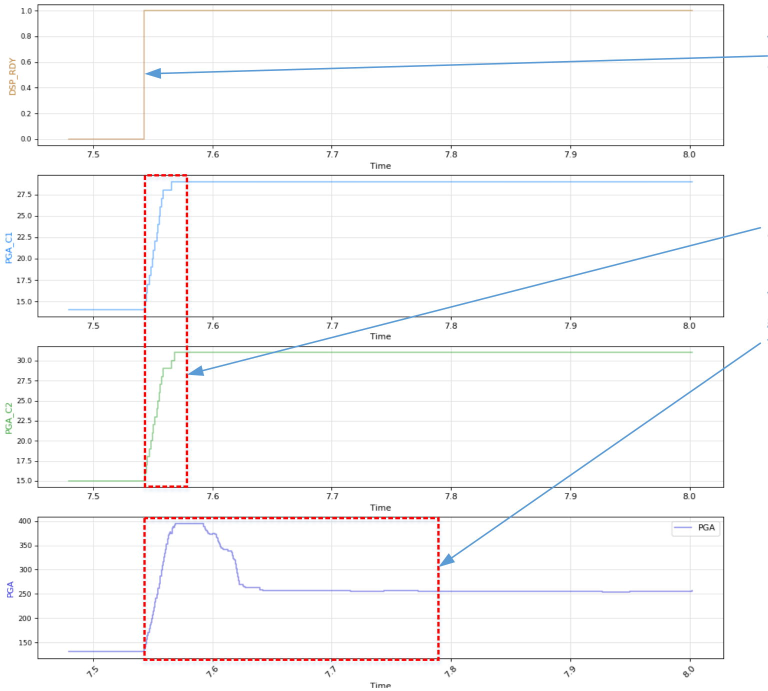
VGA Tracking

- VGA tracking is an additional state machine that starts after DSP_READY==1 that allows PGA to be adapted to track temperature variations
- Configured by DSP_STM_CFG.TRK_STM_EN



VGA tracking, when enabled, kicks in after h/w asserts DSP_READY

Firmware stepping up PGA CODE1/2 after MMTED workaround

VGA tracking loop adjusting the PGA gain after DSP_READY based on temperature + the adjustment of PGA codes

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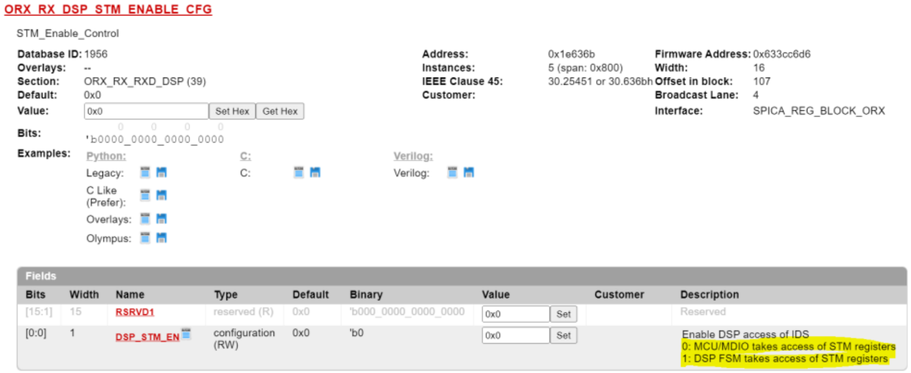
STM_ENABLE and STM Registers

- The STM register block requires special handling! These registers are controlled by the value of STM_ENABLE. If you set it wrong and try to access the registers in the f/w it will throw an exception!



ORX_RX_DSP_STM_ENABLE_CFG

STM_Enable_Control

Database ID: 1956
Overlays: --
Section: ORX_RX_RXD_DSP (39)
Default: 0x0
Value: 0x0 Set Hex Get Hex
Bits: 'b0000_0000_0000_0000

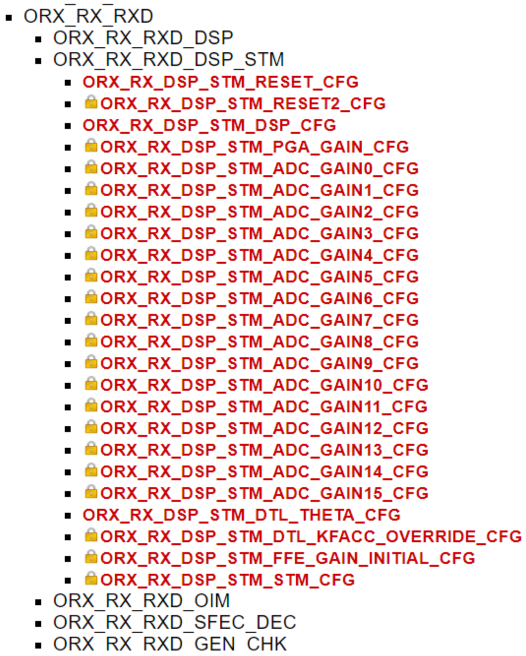
Address: 0x1e636b
Instances: 5 (span: 0x800)
IEEE Clause 45: 30.25451 or 30.636bh
Customer:

Firmware Address: 0x633cc6d6
Width: 16
Offset in block: 107
Broadcast Lane: 4
Interface: SPICA_REG_BLOCK_ORX

Examples: Python: Legacy: C Like (Prefer): Overlays: Olympus: C: C: Verilog: Verilog:

Fields

Bits	Width	Name	Type	Default	Binary	Value	Customer	Description
[15:1]	15	RSRVD1	reserved (R)	0x0	'b000_0000_0000_0000	0x0 Set		Reserved
[0:0]	1	DSP_STM_EN	configuration (RW)	0x0	'b0	0x0 Set		Enable DSP access of IDS 0: MCU/MDIO takes access of STM registers 1: DSP FSM takes access of STM registers



- ORX_RX_RXD
  - ORX_RX_RXD_DSP
  - ORX_RX_RXD_DSP_STM
    - ORX_RX_DSP_STM_RESET_CFG
    - 🔒ORX_RX_DSP_STM_RESET2_CFG
    - ORX_RX_DSP_STM_DSP_CFG
    - 🔒ORX_RX_DSP_STM_PGA_GAIN_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN0_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN1_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN2_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN3_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN4_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN5_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN6_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN7_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN8_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN9_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN10_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN11_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN12_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN13_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN14_CFG
    - 🔒ORX_RX_DSP_STM_ADC_GAIN15_CFG
    - ORX_RX_DSP_STM_DTL_THETA_CFG
    - 🔒ORX_RX_DSP_STM_DTL_KFACC_OVERRIDE_CFG
    - 🔒ORX_RX_DSP_STM_FFE_GAIN_INITIAL_CFG
    - 🔒ORX_RX_DSP_STM_STM_CFG
  - ORX_RX_RXD_OIM
  - ORX_RX_RXD_SFEC_DEC
  - ORX_RX_RXD_GEN_CHK

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Kp/Kf/Kvff

- Control variables for the CDR loop
  - Kp = gain or attenuation
  - Kf = low pass filter
  - Kvff = dampening factor
- Kp/Kf/Kvff control the loop filter which speeds up/slows down the PLL to match the receive clock.
- Setup to minimize jitter
- Kp/Kf/Kvff come from the hardware/validation team

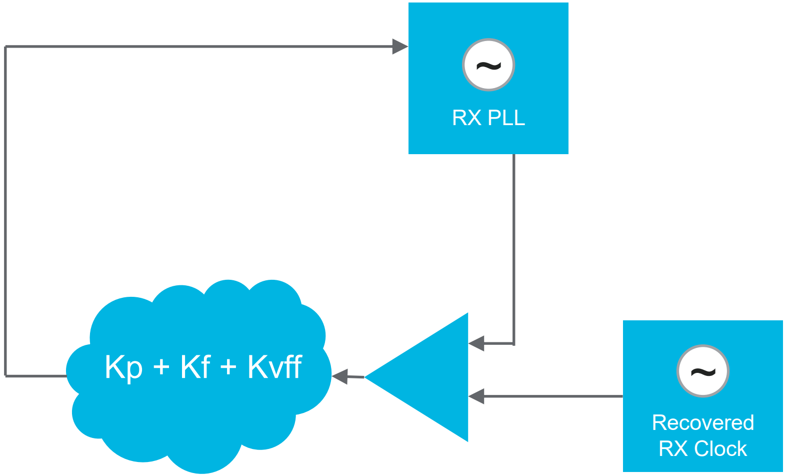
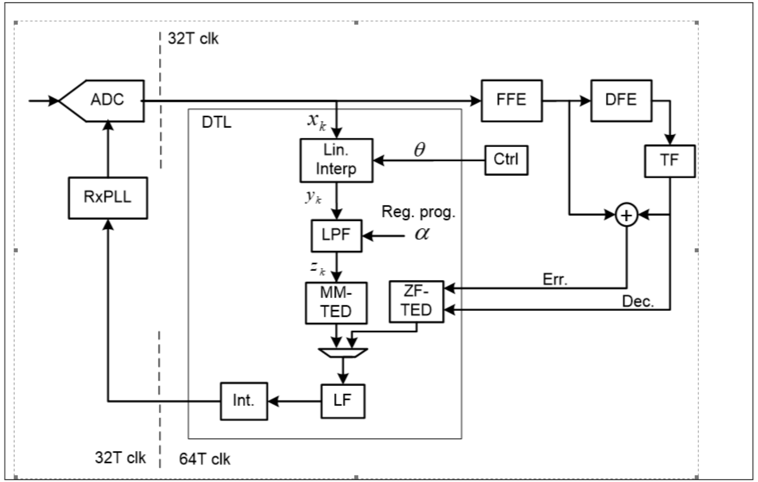


Figure 23 Digital Timing Loop Block Diagram



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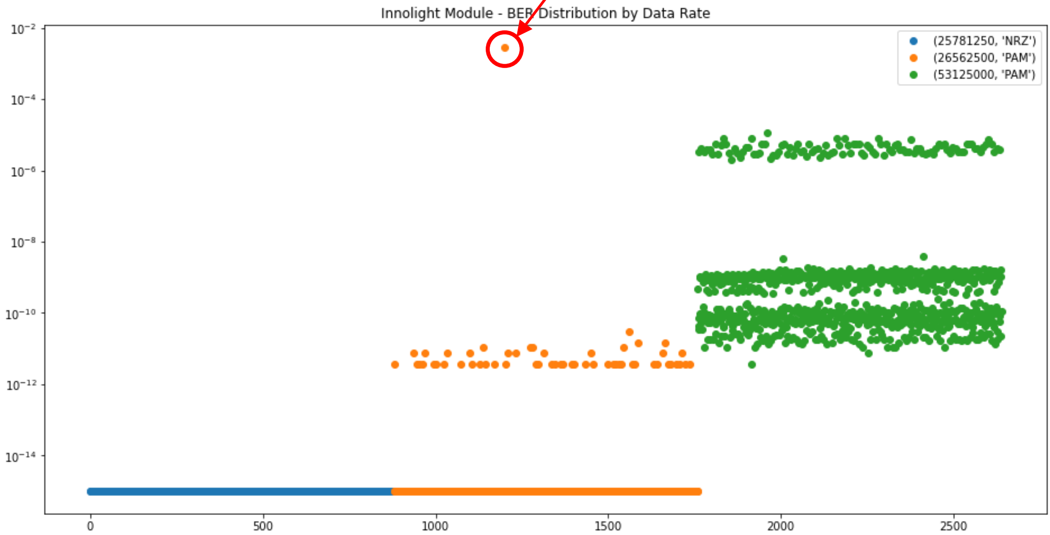
Why QC?

- QC stands for Quality Control
- The receiver hardware isn't perfect
  - Sometimes it may bring the RX up in sub-optimal state
  - QC there to try to catch this and restart the RX
  - Can't usually measure BER
- QC Types:
  - SNR (easiest)
  - Histogram
  - Slicer Thresholds

DSP started up in
bad state with high BER



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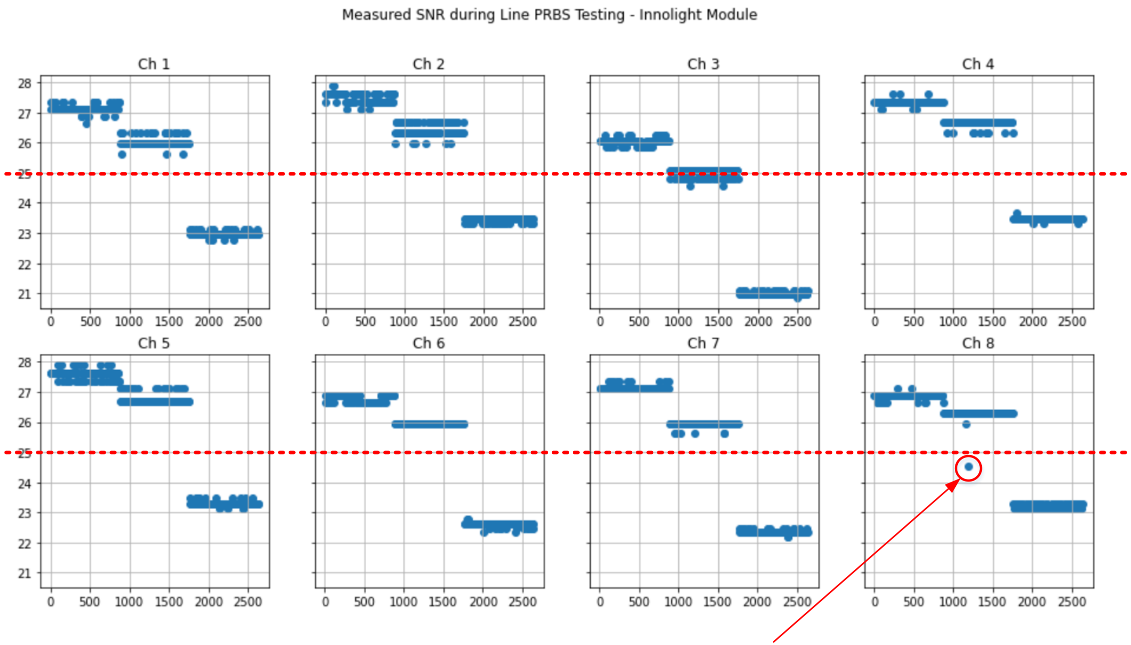
QC – SNR Check

- Monitor SNR before and after entering data mode and verify SNR > input threshold.



SNR below QC threshold

QC – Histogram and Slicer Checks

- https://sw.inphi-corp.local/bookstack/books/infrastructure/page/rx-quality-checks

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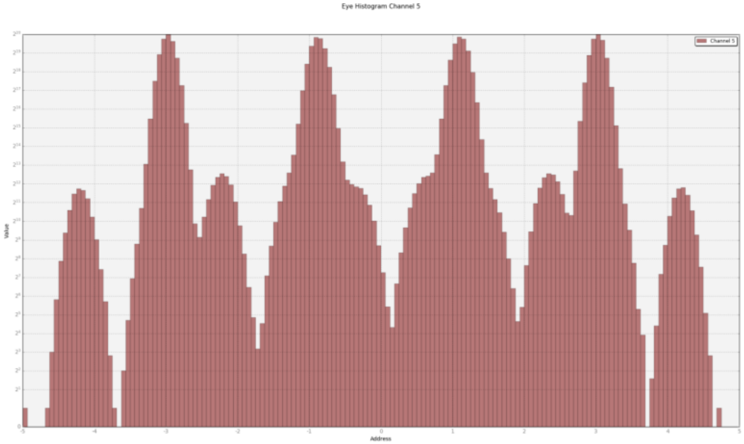
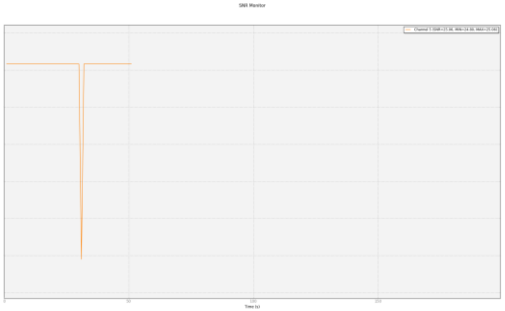
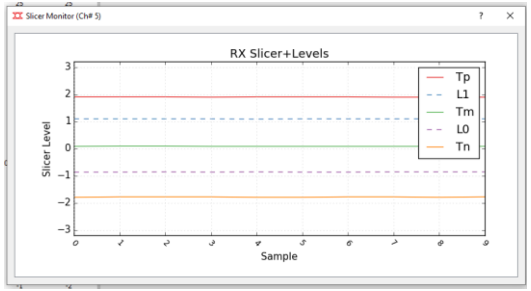
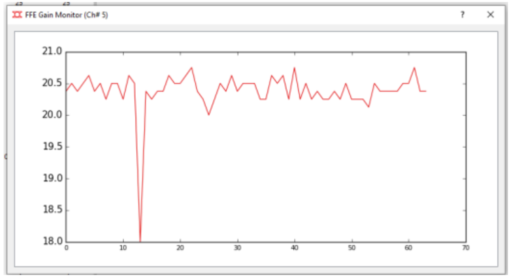
QC Limitations - Bad Histogram

- QC is not perfect. Here is an example that it doesn't catch.









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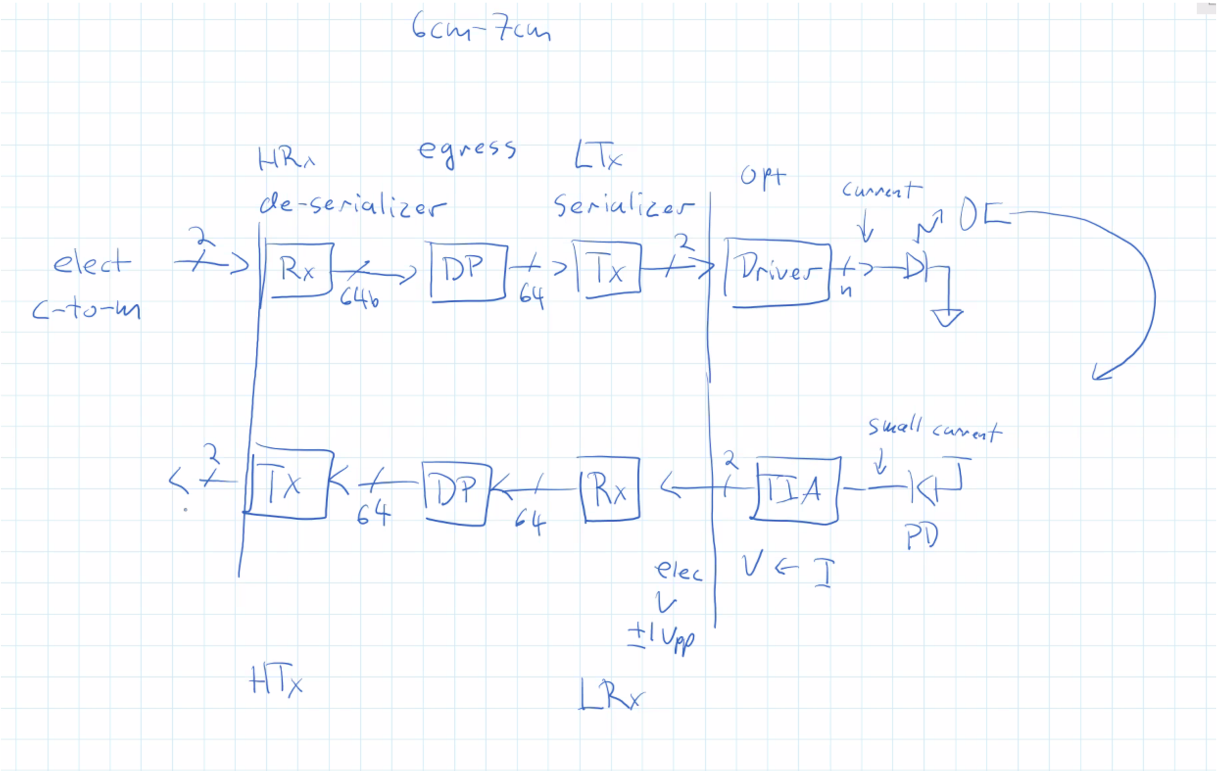
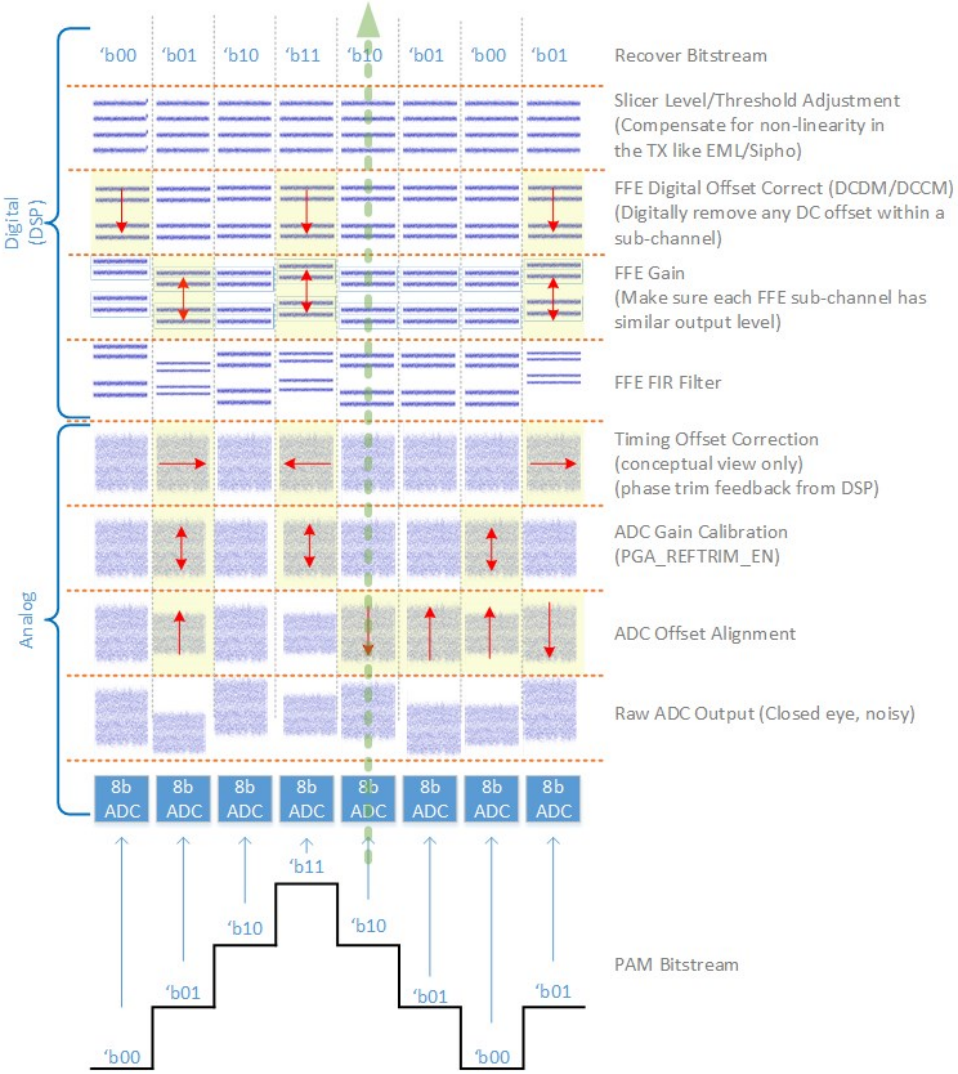
Devin’s Serializer/De-serializer Diagram

- PD=Photo Diode
- TIA = Transimpedance Amplifier (Convert photo-diode current into voltage)



What is Happening

- Conceptual View of what the RX is doing



Recover Bitstream

Slicer Level/Threshold Adjustment (Compensate for non-linearity in the TX like EML/Sipho)

FFE Digital Offset Correct (DCDM/DCCM) (Digitally remove any DC offset within a sub-channel)

FFE Gain (Make sure each FFE sub-channel has similar output level)

FFE FIR Filter

Timing Offset Correction (conceptual view only) (phase trim feedback from DSP)

ADC Gain Calibration (PGA_REFTRIM_EN)

ADC Offset Alignment

Raw ADC Output (Closed eye, noisy)

PAM Bitstream

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Hardware FSMs

- Sequencer or STM (State Machine)
  - This is the top-level state machine which controls the DSP bringup
- PGA FSM
  - The PGA FSM is used to optimize the PGA gain such that the ADC samples use the entire swing.
- DTS/DTL FSM
  - The DTS FSM is used to optimize the phase and recover the timing
- VGA Tracking FSM
  - Change the PGA gain after DSP_READY to compensate for temperature

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STM - Hardware Sequencer

1. Signal Detect
2. PGA FSM
3. DTL FSM
4. DSP_READY

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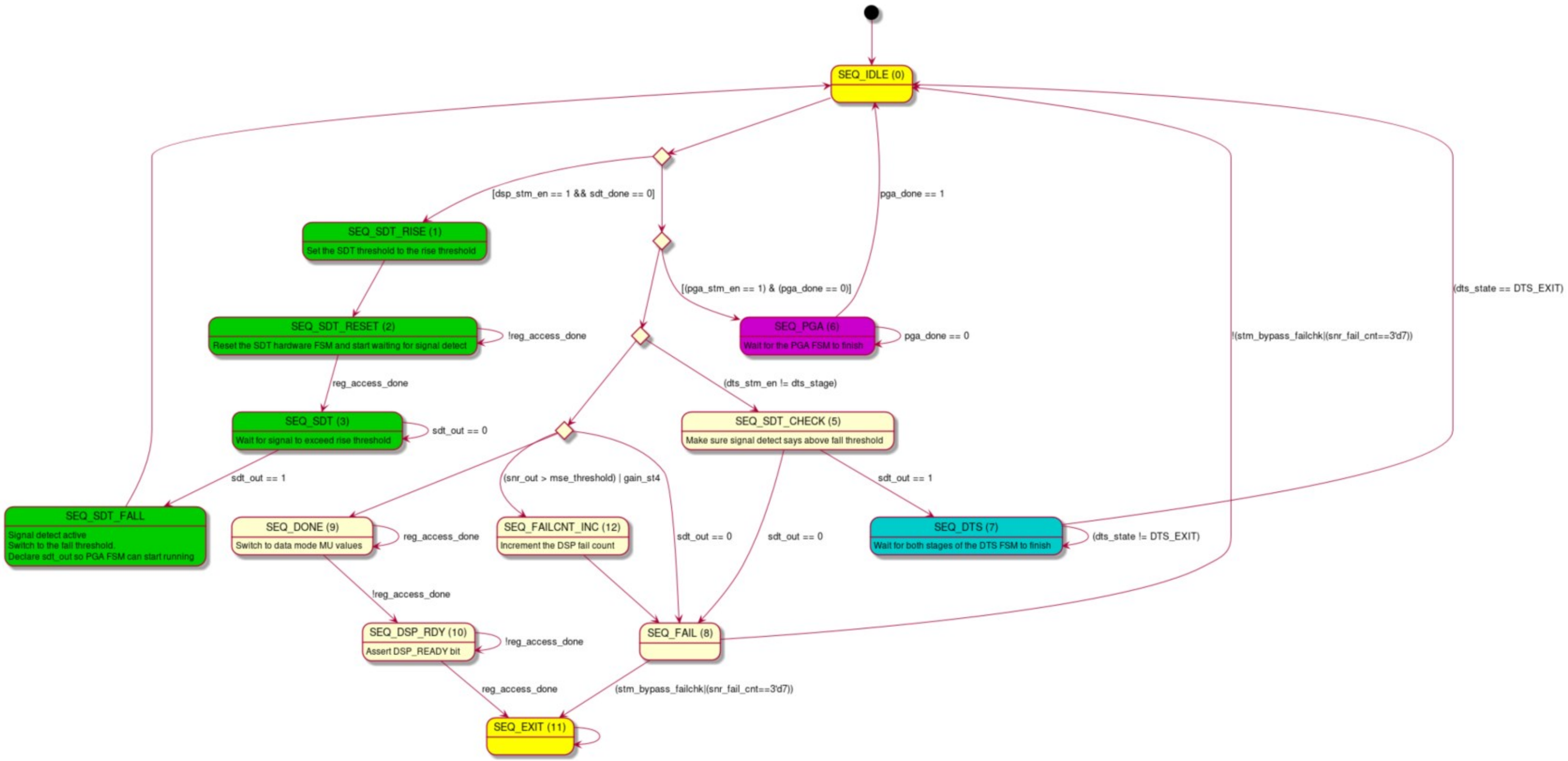
STM FSM


SEQ_IDLE (0)
[dsp_stm_en == 1 && sdt_done == 0]
pga_done == 1
SEQ_SDT_RISE (1)
Set the SDT threshold to the rise threshold
[(pga_stm_en == 1) & (pga_done == 0)]
(dts_state == DTS_EXIT)
SEQ_SDT_RESET (2)
Reset the SDT hardware FSM and start waiting for signal detect
!reg_access_done
SEQ_PGA (6)
Wait for the PGA FSM to finish
pga_done == 0
!(stm_bypass_failchk|(snr_fail_cnt==3'd7))
reg_access_done
(dts_stm_en != dts_stage)
SEQ_SDT (3)
Wait for signal to exceed rise threshold
sdt_out == 0
SEQ_SDT_CHECK (5)
Make sure signal detect says above fall threshold
sdt_out == 1
(snr_out > mse_threshold) | gain_st4
sdt_out == 1
SEQ_SDT_FALL
Signal detect active
Switch to the fall threshold.
Declare sdt_out so PGA FSM can start running
SEQ_DONE (9)
Switch to data mode MU values
reg_access_done
SEQ_FAILCNT_INC (12)
Increment the DSP fail count
sdt_out == 0
sdt_out == 0
SEQ_DTS (7)
Wait for both stages of the DTS FSM to finish
(dts_state != DTS_EXIT)
!reg_access_done
SEQ_DSP_RDY (10)
Assert DSP_READY bit
!reg_access_done
SEQ_FAIL (8)
reg_access_done
(stm_bypass_failchk|(snr_fail_cnt==3'd7))
SEQ_EXIT (11)

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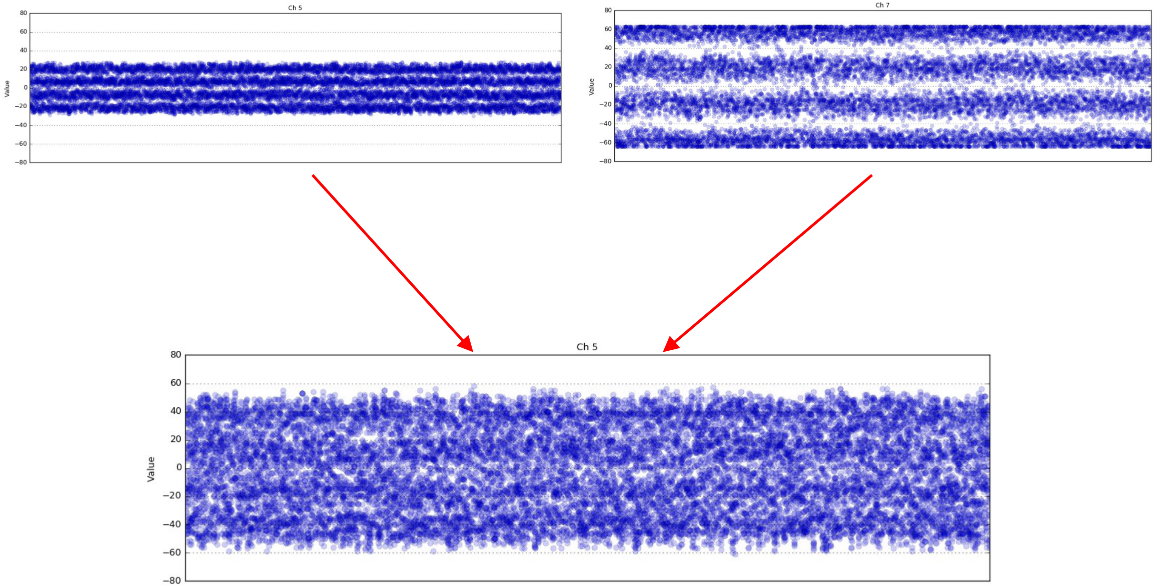
PGA FSM

- Optimizes the analog gain so that the ADC samples use the full ADC range (-63 to +63)



PGA Gain Optimized to use full ADC range without clipping

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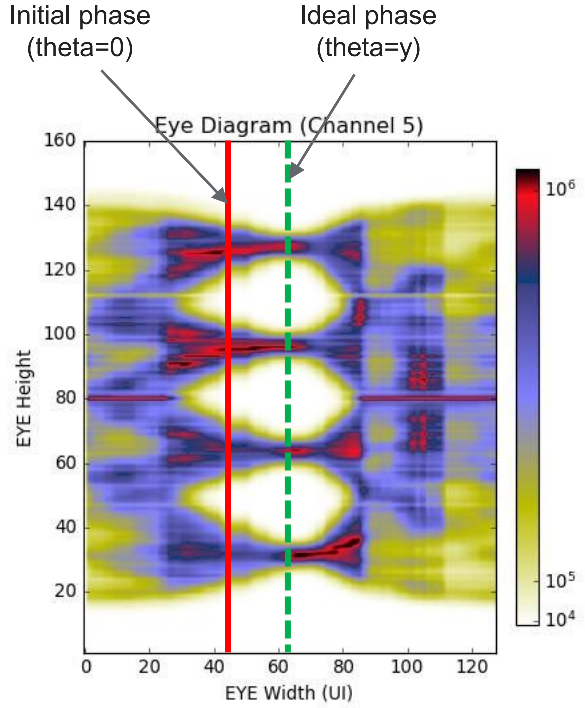
DTS/DTL FSM – Theta Sweep

- Theta represents the phase
- Goal of theta sweep is to find the horizontal center of the eye (the green dashed line in the diagram on the right)



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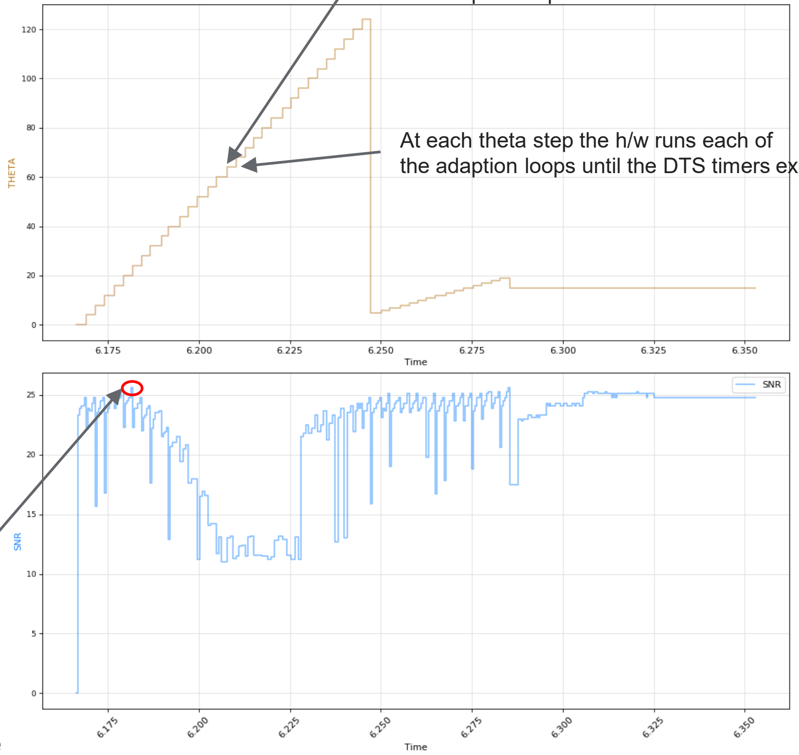
DTS/DTL FSM – Theta Sweep

- The hardware sweeps each theta/phase point looking for the highest SNR.
- There are two sweeps, a coarse sweep with larger steps, and a secondary fine sweep with smaller steps.
- At each step the h/w adapts each of the DSP loops like the FFE taps and FFEG ain.



Hardware increments theta in coarse steps and then measures the SNR at each theta (after the DTS timers expire) to determine optimum phase.

At each theta step the h/w runs each of the adaption loops until the DTS timers expire

Optimum theta/phase somewhere here

This plot shows the SNR values reported by the SNR monitor but the h/w only uses the peaks of each of these points when searching for the best SNR. This corresponds with the expiration of the DTS timers at each sample point.

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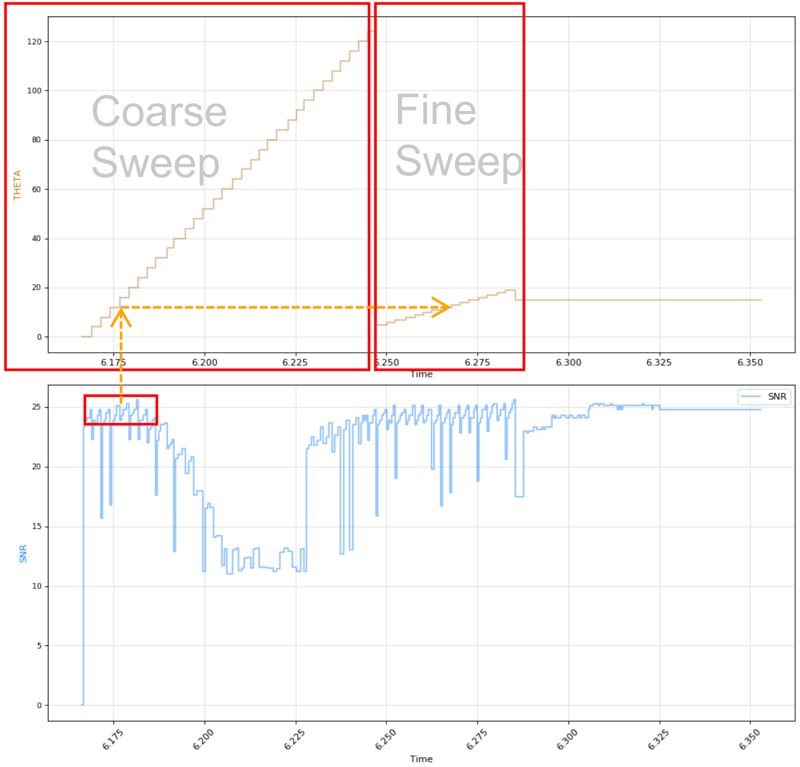
DTS/DTL FSM – Window Optimization

- When window optimization is enabled the h/w uses a sliding window instead of looking at a single point. It figures out which window has the highest average SNR.
- Enabled via THETA_OPT_WIN
- User must manually limit DTS range to avoid h/w bug.



This plot shows the SNR values reported by the SNR monitor but the h/w only uses the peaks of each of these points when searching for the best SNR.

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Hardware Breakpoints

The hardware supports breakpoints that can halt each of the state machines at a particular step.

Register	Description
STM_SEQ_STATE_OVERRIDE_CFG	Override or halt the top level sequencer or STM
STM_SEQ_STATE_STATUS	The current status of the top level sequencer or STM
STM_PGA_STATE_OVERRIDE_CFG	Override or halt the PGA FSM at a particular state
STM_PGA_STATE_STATUS	The current status of the PGA FSM
STM_DTS_STATE_OVERRIDE_CFG	Override or halt the DTS FSM at a particular state
STM_DTS_STATE_STATUS	The current status of the DTS FSM

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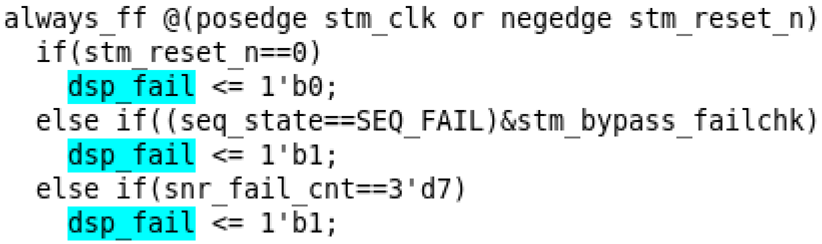
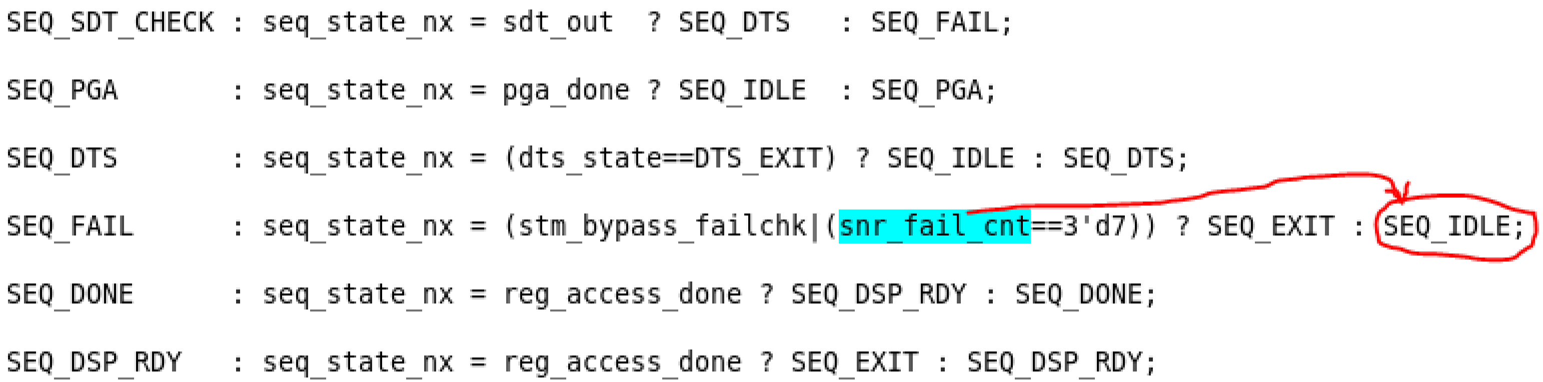
STM Automatic Retry on Failure

- When the STM detects a failure like an SNR drop it will attempt to automatically restart up to 7 times. Instead of exiting it attempts to restart automatically



```
always_ff @(posedge stm_clk or negedge stm_reset_n)
  if(stm_reset_n==0)
    dsp_fail <= 1'b0;
  else if((seq_state==SEQ_FAIL)&stm_bypass_failchk)
    dsp_fail <= 1'b1;
  else if(snr_fail_cnt==3'd7)
    dsp_fail <= 1'b1;
```



```
SEQ_SDT_CHECK : seq_state_nx = sdt_out  ? SEQ_DTS   : SEQ_FAIL;

SEQ_PGA       : seq_state_nx = pga_done ? SEQ_IDLE  : SEQ_PGA;

SEQ_DTS       : seq_state_nx = (dts_state==DTS_EXIT) ? SEQ_IDLE : SEQ_DTS;

SEQ_FAIL      : seq_state_nx = (stm_bypass_failchk|(snr_fail_cnt==3'd7)) ? SEQ_EXIT : SEQ_IDLE;

SEQ_DONE      : seq_state_nx = reg_access_done ? SEQ_DSP_RDY : SEQ_DONE;

SEQ_DSP_RDY   : seq_state_nx = reg_access_done ? SEQ_EXIT : SEQ_DSP_RDY;
```

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STM Automatic Retry on Failure

- Problem is the PGA and DTS registers are only reset in the PGA_INIT and DTS_INIT states
- If DSP automatically restarts one of the STM registers could be in the incorrect state! For example, AFE_TRIM could be wrong or the initial THETA_CFG could be incorrect.

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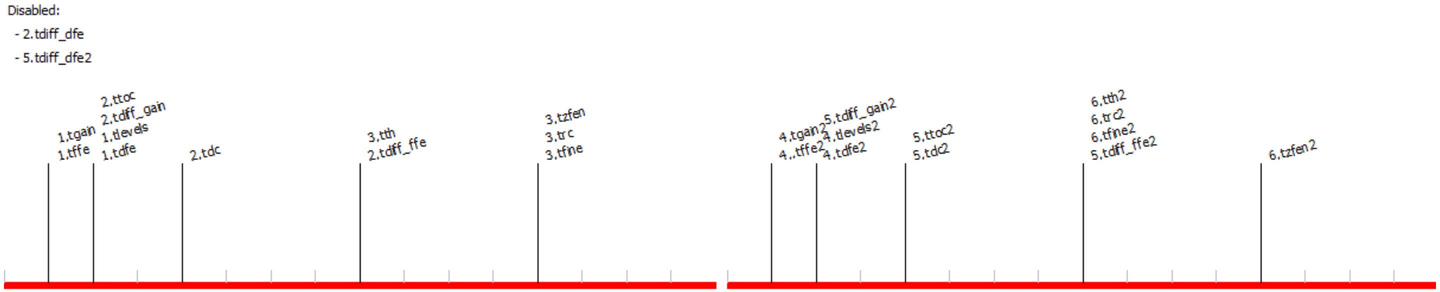
DTS/DTL FSM – DTS TIMERS

- As theta is stepped h/w runs individual adaptation loops.
- DTS timers control when each adaption step is run during the DTS FSM.
- Timers not used after DSP_READY asserted, switch to DSP MUs.



PI vs. FCW

- The 50G IPs like Syrma (and Polaris) use a phase interpolator
- The 100G IPs like Capella/Porrima/Mira/Spica+ have a feedback path to the PLL to allow the CDR to adjust the VCO frequency to match the recovered clock.
  - Disconnect PLL
    - ORX_RX_PLL_PLLD_CFG0.AFIFO_DOUT_OVERRIDE_EN=1
  - Connect PLL
    - ORX_RX_PLL_PLLD_CFG0.AFIFO_DOUT_OVERRIDE_EN=0

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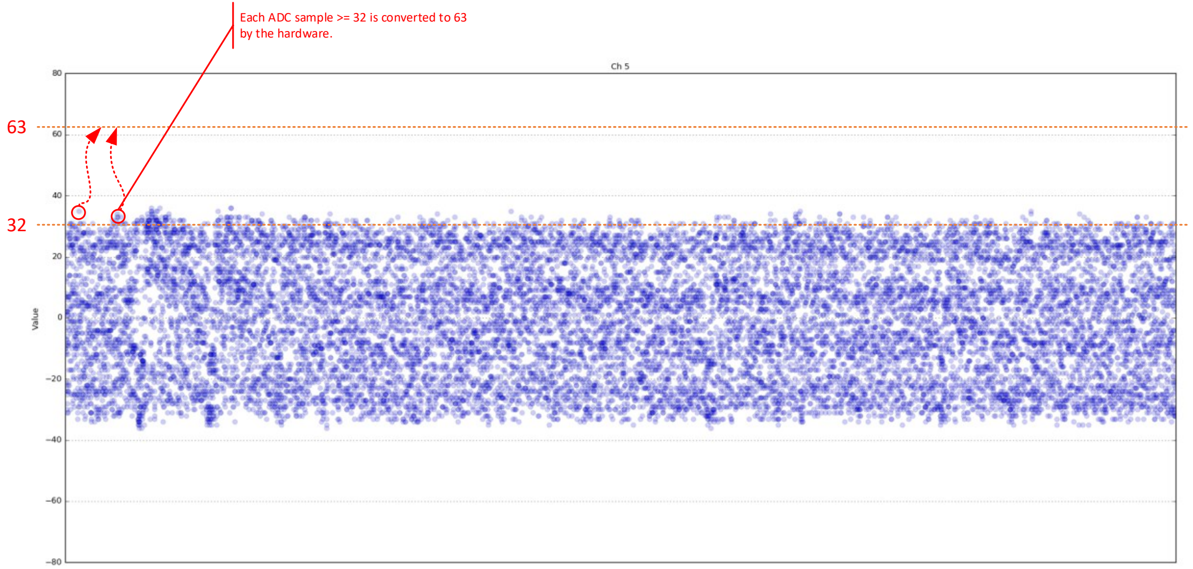
Delta Sigma Modulator

- TBD

MMTED Bug

- Only impacts the MMTED path (Mueller Muller Timing Error Detector)
- ADC samples are artificially saturated to the max code due to 7 to 6 bit conversion error in the MMTED path.



Each ADC sample >= 32 is converted to 63 by the hardware.

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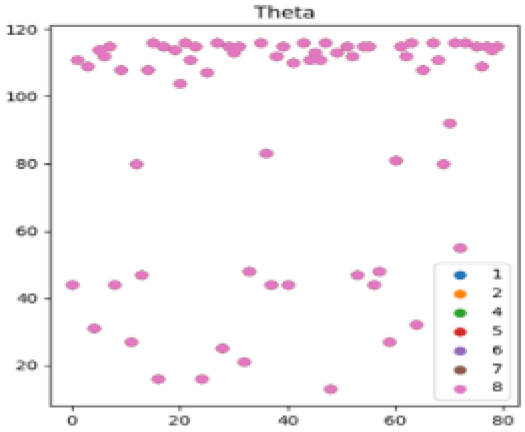
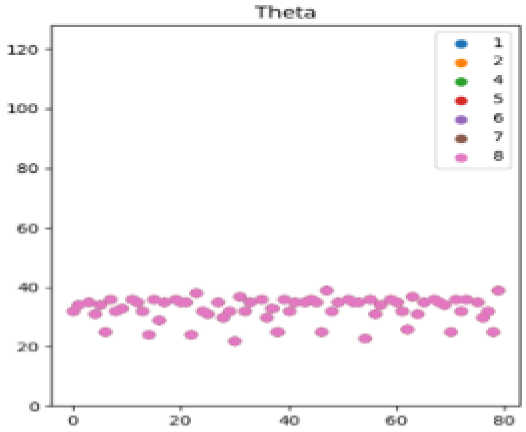
MMTED Bug - Consequence

- Primary issue is hardware has trouble picking theta

Without MMTED Workaround	With MMTED Workaround
	

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MMTED Bug - Workaround

- MMTED Workaround (
  - Limit ADC codes to -31 to +31 by halving PGA_CODE1+PGA_CODE2 to avoid saturation bug
  - Reduce analog gain by tweaking ADC parameters
  - Start DSP in MM mode
  - Wait for DSP to lock
  - Switch to ZF mode
  - Revert PGA_CODE1/CODE2, wait for VGA tracking to recover ADC envelope
  - Step FFE pre-cursor to compensate for phase variation
- See https://ewiki.marvell.com/display/ODSP/MMTED+Workaround

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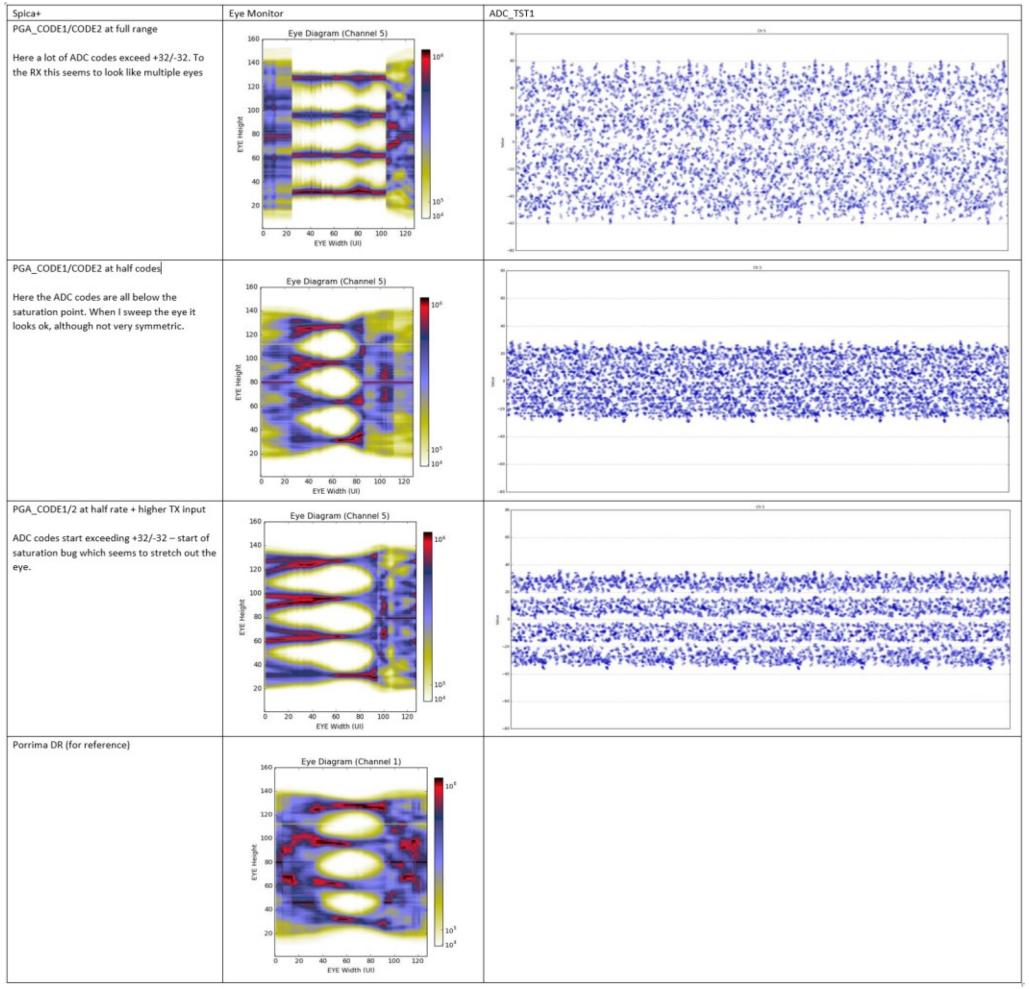
MMTED Bug

- Visualization of the MMTED bug using the eye monitor
- Top eye plot shows h/w having hard time scanning theta/phase.



Spica+	Eye Monitor	ADC_TST1
PGA_CODE1/CODE2 at full range Here a lot of ADC codes exceed +32/-32. To the RX this seems to look like multiple eyes		
PGA_CODE1/CODE2 at half codes Here the ADC codes are all below the saturation point. When I sweep the eye it looks ok, although not very symmetric.		
PGA_CODE1/2 at half rate + higher TX input ADC codes start exceeding +32/-32 – start of saturation bug which seems to stretch out the eye.		
Porrima DR (for reference)		

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Health Check of RX

- SNR
- Histogram
- FFE Taps
- PGA Gain and Debug Memory
- Slicer
- FFE Gain
- TOC Codes
- ADC Offsets
- Hardware FSM State Registers

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Health Check - SNR

- SNR should be stable and not drifting
- No large oscillations > 0.5dB

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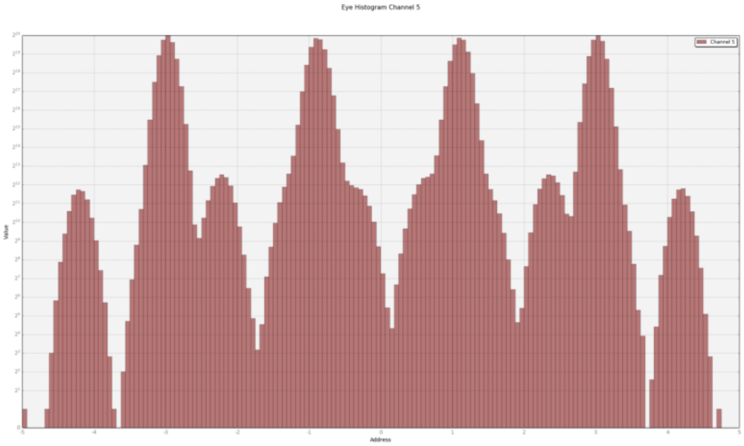
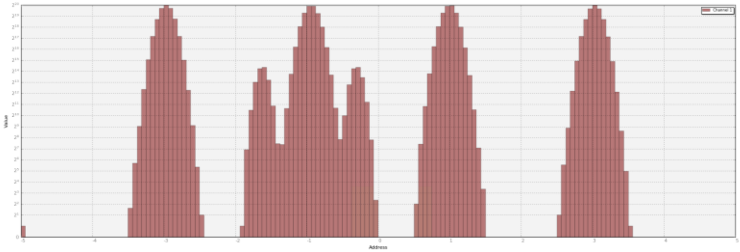
Health Check - Histogram

- The histogram should be clean with no extra lobes.





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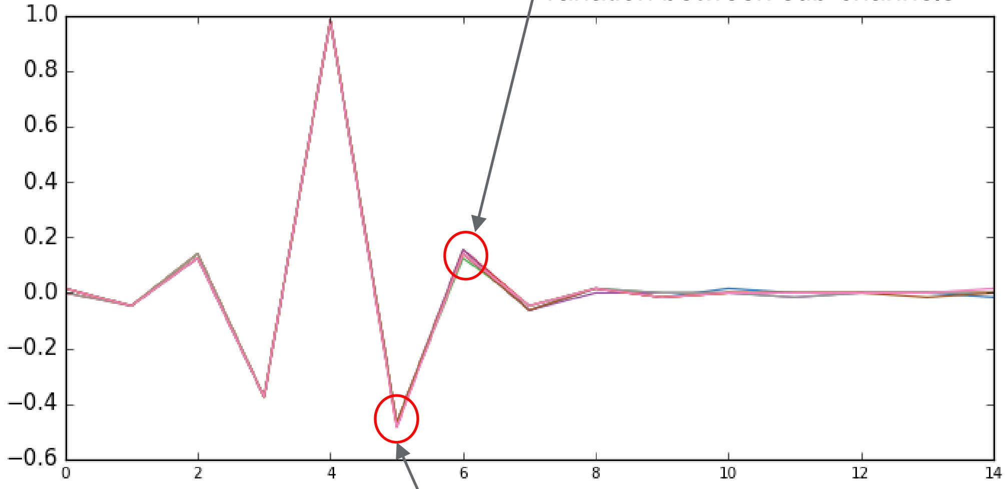
Health Check – FFE Taps

- If the pre-cursor taps look very flat we could run into FFE/DTL conflict
- If one or more taps are changing a lot/drifting then something is wrong
- If the sub-channels are different then there might be an issue with the timing correction.



Should be minimal variation between sub-channels

If you poll the FFE taps each tap shouldn’t be drifting up or down significantly

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Health Check – Sequencer Status

- RX_DSP_STM_SEQ_STATE_STATUS should report SEQ_EXIT state (11 on Spica+)
- RX_DSP_STM_PGA_STATE_STATUS should report PGA_EXIT state (20 on Spica+)
- DSP_STM_MIRROR_STATUS should report:
  - DSP_READY=1
  - PGA_DONE=1
  - DTS_DONE=1
  - DSP_FAIL=0

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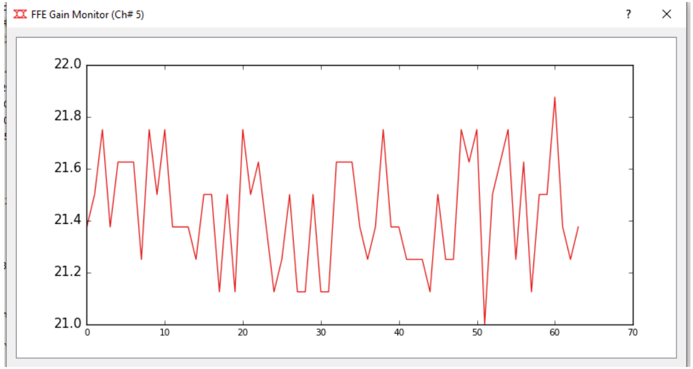
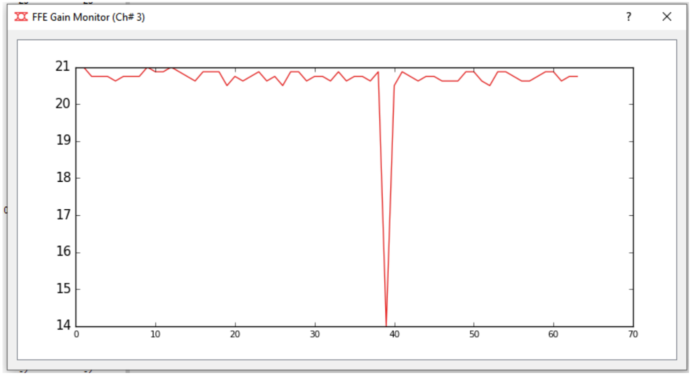
Health Check – FFE Gain

- FFE Gains across all sub-channels should have a similar value.

Good FFE Gain



Bad FFE Gain



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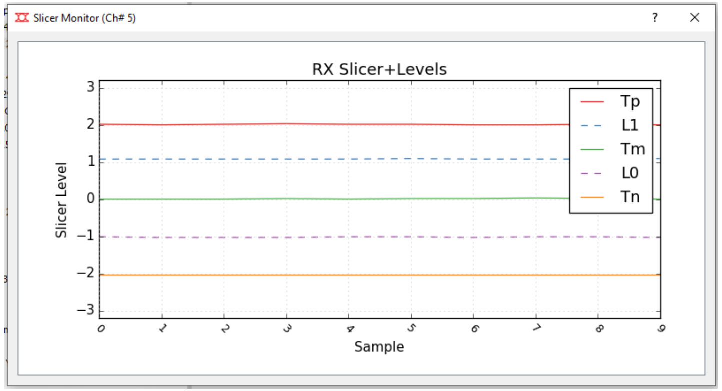
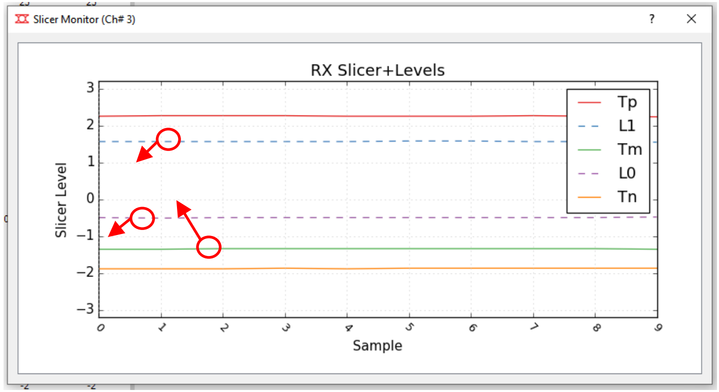
Health Check - Slicers

- +3 and -3 levels are fixed
- Inner slicer levels should be close to +1/-1.
- The slicer thresholds should be close to -2, 0, +2.

Good Slicers



Bad Slicers



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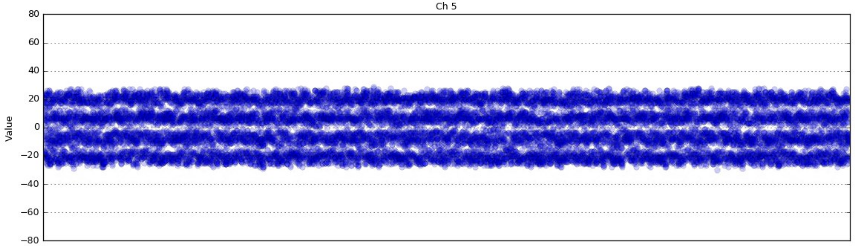
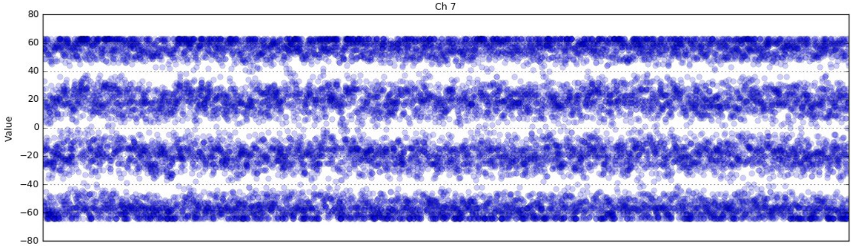
Health Check - PGA Gain

- ADC_TST1 should show the ADC samples between +/- 63 to avoid clipping or loss of precision

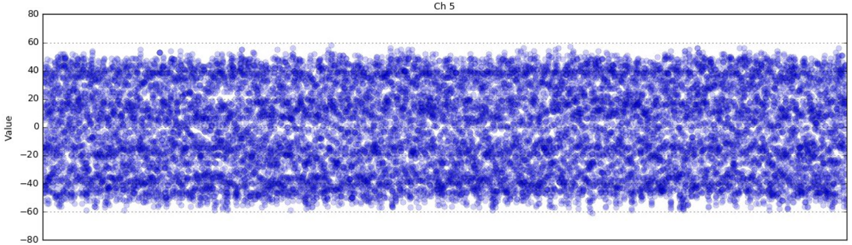
Gain too low – Only part of the ADC swing used – loss of precision



Gain too high – ADC clipping will cause problems for the DSP



PGA Gain Optimized to use full ADC range without clipping



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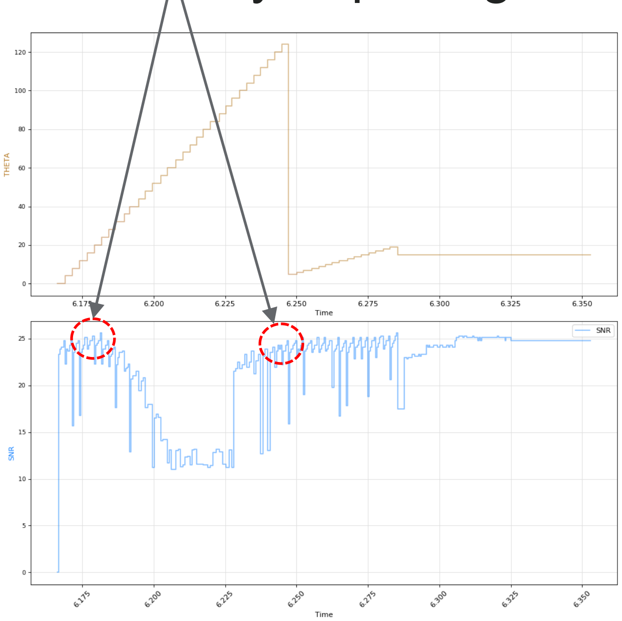
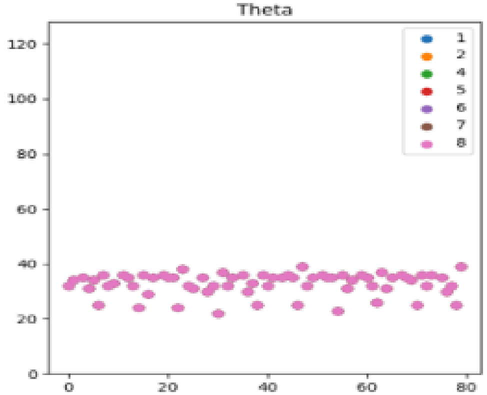
Health Check - Theta

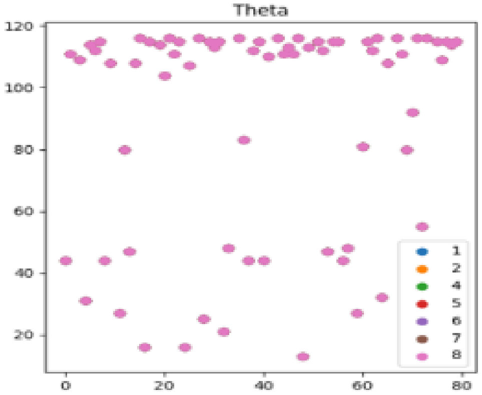
- The run to run distribution of theta should be in one or two relatively tight bands on either side of the vertical eye opening



Good Run to Run Theta Distribution



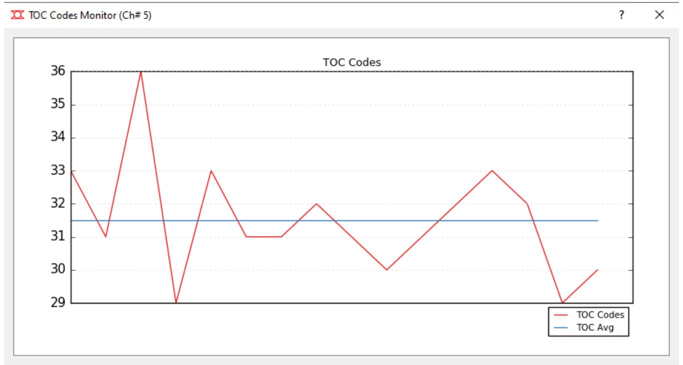
Bad Run to Run Theta Distribution



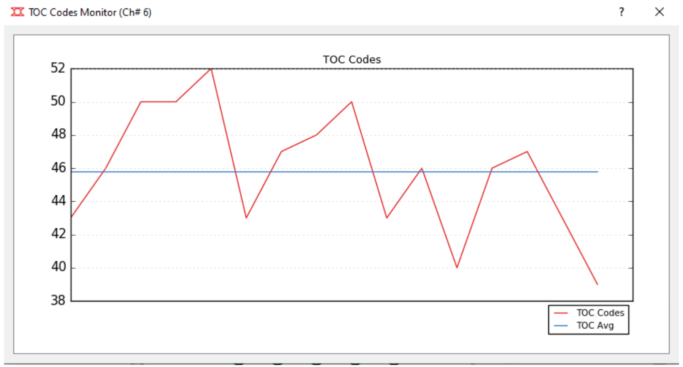
Health Check – TOC Codes

- TOC = Timing Offset Codes
- Corrects for time offsets between each of 64 ADC sub-channels
- Average of all TOC codes should be balanced around 31.5
- No individual code should be significantly different than another

Good TOC Codes



Bad TOC Codes = not balanced around 31.5



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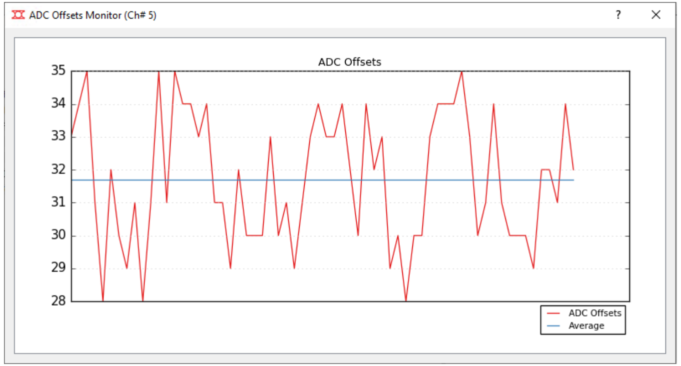
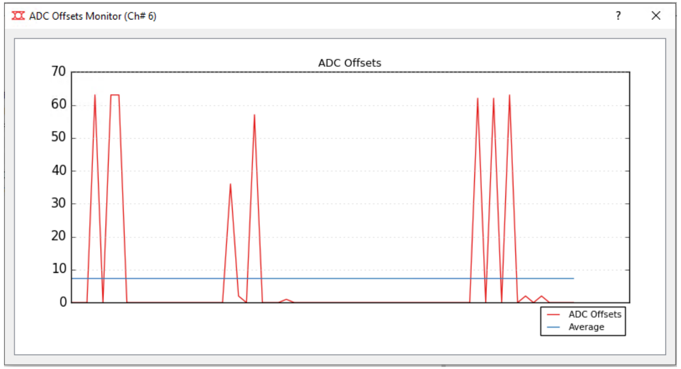
Health Check – ADC Offsets

- DC offset correction on each ADC sub-channel
- Average of all ADC offsets should be balanced around 31.5
- No individual ADC should be significantly different than another.

Good ADC Offsets



Bad ADC Offsets



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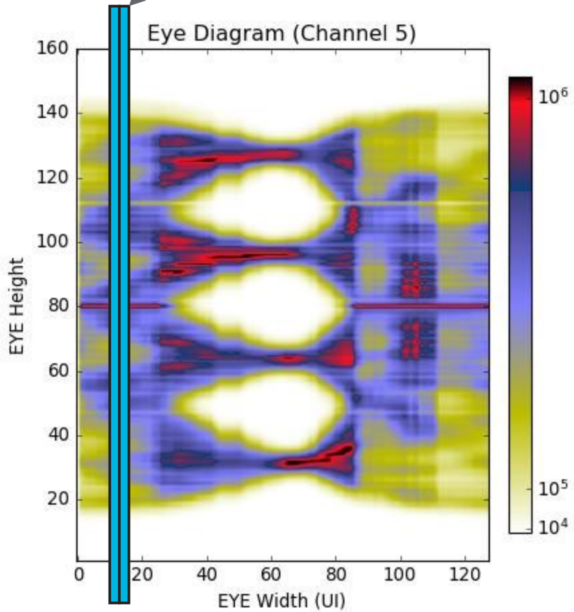
How the Eye Monitor Works

- Destructive in that it will disturb traffic flow
- Works by:
  - Put RX in MM mode to allow changing theta
  - Freeze DSP
  - Sweep theta from 0-126 and capture histogram at each theta point
  - Rotate the histogram and glue each histogram together to form vertical slices of the eye.

Individual histograms at each theta are rotated and glued together to form eye diagram.



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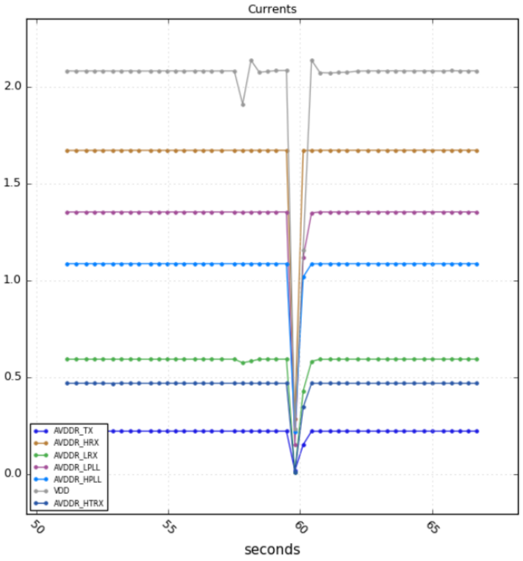
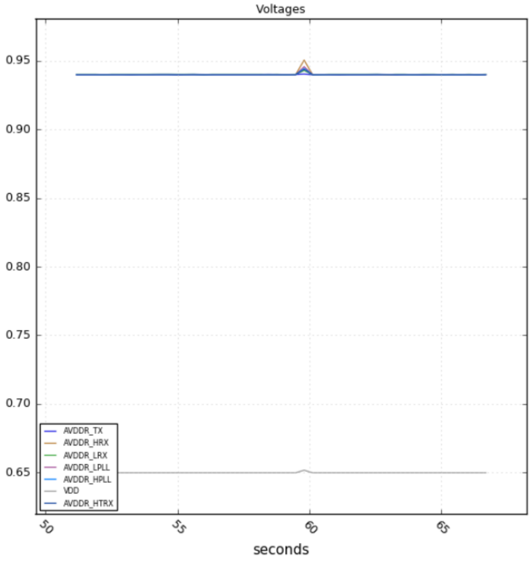
Power Swing

- This is a measure of the supplies from the EVB on Spica+ during configuration
- The amount of power swing when configuring the device is a concern.
- The external supplies are supposed to handle large current swing, but it could create noise or voltage droop which may impact the receiver or PLL locking.





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Slow Down Too Soon

– A common problem with the f/w is it slows down the DSP MUs too soon.

– Need to make sure that VGA tracking is not making large adjustments before freezing the DSP MUs.

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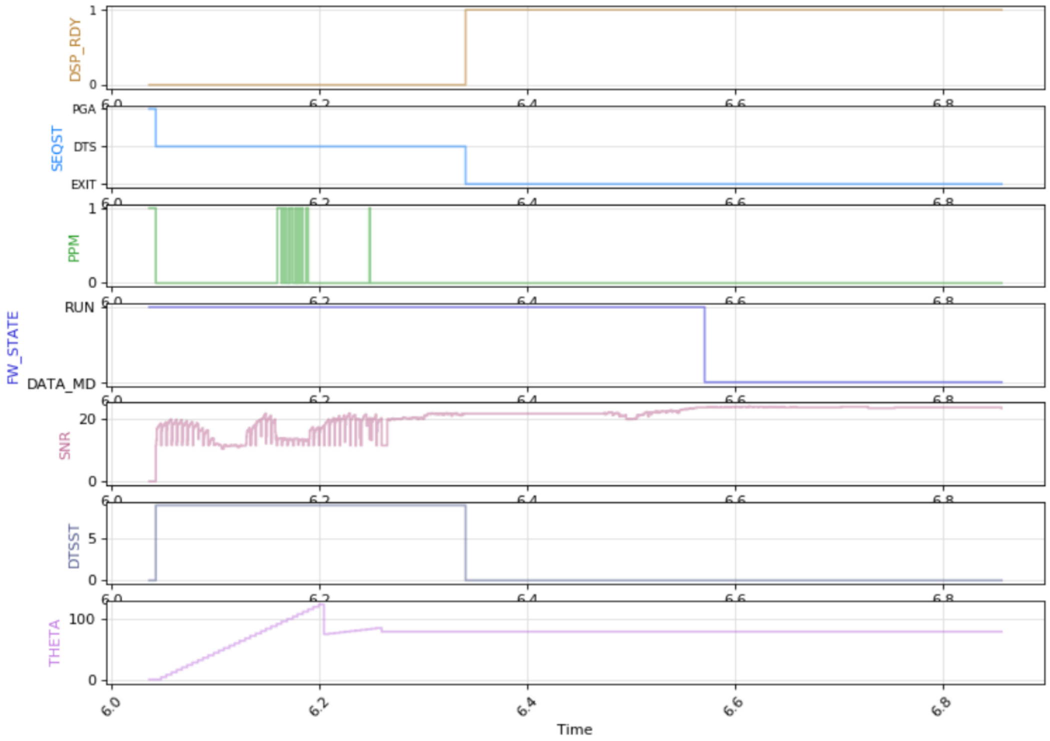
Problem – Half Rate Over-peaked Eye

- Here there is too much post peak in half-rate mode.
- This almost seems like the RX is seeing more than one UI



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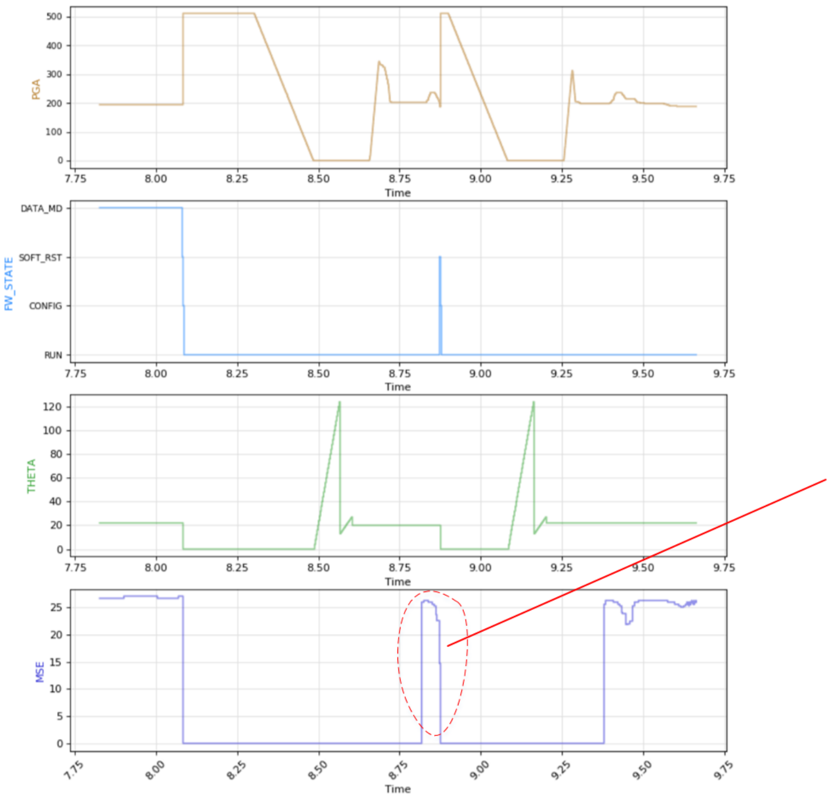
FFE Walk Problems – Eye Too Peaked



Due to the shape of the eye the FFE walk gets into trouble. It tries to walk the post cursor

ADC Offsets

- Remove any vertical offset between individual ADC sub-channels

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Timing Correction

- This removes any phase differences between individual ADC sub-channels

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DC Offset Correction

- DCCM = Common Mode DC Offset Correction
- DCDM = Differential Mode DC Offset Correction

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