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Spica5n FEC Monitoring Overview

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Agenda

- RS FEC Basics
- FEC Modes and Standards
- FEC Statistics
- Spica5n Block Diagram
- FEC Generation / Monitoring Simulation

RS FEC Basics

- Reed-Solomon FEC encoding involves taking *message* data, calculating *parity* and appending it to the message to form a *codeword*.
- When decoding a codeword, a *syndrome* is calculated. If the syndrome is 0, there are no errors. A non-zero syndrome means there are errors. If there are less that *T* errors, by mathematically solving an equation the errors can be corrected.

RS FEC Basics

- Data is compressed to compensate for the addition of parity through transcoding
- 4x66b converted to 257b
- Message is 20x257b (514 10b RS symbols)
- Two encoding supported.
  - KR: RS(528,514), 14 parity symbols, T=7
  - KP: RS(544,514), 30 parity symbols, T=15

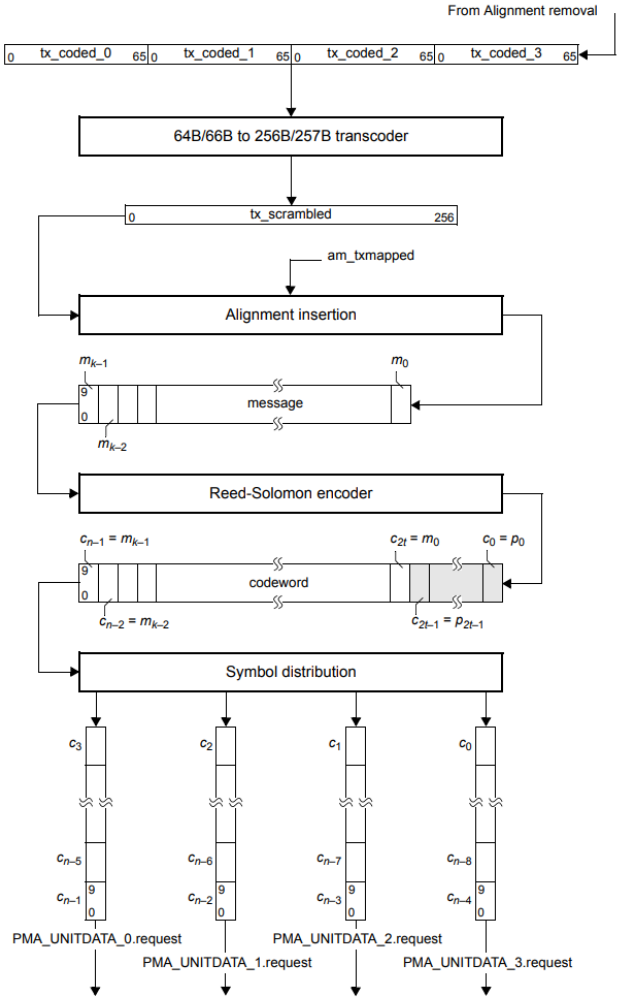


Figure 91–6—Transmit bit ordering

RS FEC Basics

- Before transcoding: 20 x 4 x 66 = 5280 bits
- After transcoding: 20 x 257 = 5140 bits (difference of 140 bits)
- KR adds 140 parity bits. Input and output rates match.
- KP adds 300 parity bits. Output is 544/528 times faster than the input.

RS FEC Basics

- RS symbols are distributed to FEC lanes.
- Every FEC lane has periodic alignment markers.
- Alignment markers have a common marker portion (to simplify detection) and a unique marker portion to identify the FEC lane.
- Alignment markers are used to deskew the FEC lanes and reorder them to reassemble codewords for decoding.
- FEC lanes can be bit interleaved (e.g four FEC lanes are interleaved for 100G PAM4)

RS FEC Basics

- T represents the number of errors that can be corrected.
- For KR, T = 7. A codeword with between 1 and 7 symbol errors can be corrected. An errored symbol can have between 1 and 10 bit errors. If there are 8 or more symbol errors the codeword is uncorrectable.
- For KP, T = 15. Codewords with 1 to 15 errors are correctable. Codewords with more than 15 errors are uncorrectable.
- Some modes have interleaved codewords. Two codewords are symbol interleaved before being transmitted to improve burst error tolerance.

RS Modes and Standards

Mode	# FEC Lanes	Interleaved Codewords	# Channels	Standard	Section
25G KR	1	No	8	IEEE 802.3by	Clause 108
50G KR and KP	2	No	8	IEEE 802.4	Clause 134
100G KR and KP	4	No	8	IEEE 802.3 published	Clause 91
100G CK	4	Yes	8	IEEE 802.3ck	Clause 161
200G KP	8	Yes	4	IEEE 802.3bs	Clause 119
400G KP	16	Yes	2	IEEE 802.3bs	Clause 119
800G KP	32	Yes	1	Ethernet Consortium	

RS Modes and Standards

- Standards available on:
  https://marvell.sharepoint.com/sites/hsc/engineering
- Standards for 400G and below are found in:
  Documents > Publications > Standards > IEEE (Ethernet 802.3)
- Standards for 800G:
  Documents > Publications > Standards > Ethernet Technology Consortium

FEC Statistics

- Processed codewords
- Corrected codewords
- Uncorrected codewords
- Bit errors
- Histogram (two variants for interleaved codewords)
- Symbol Errors (per FEC lane)

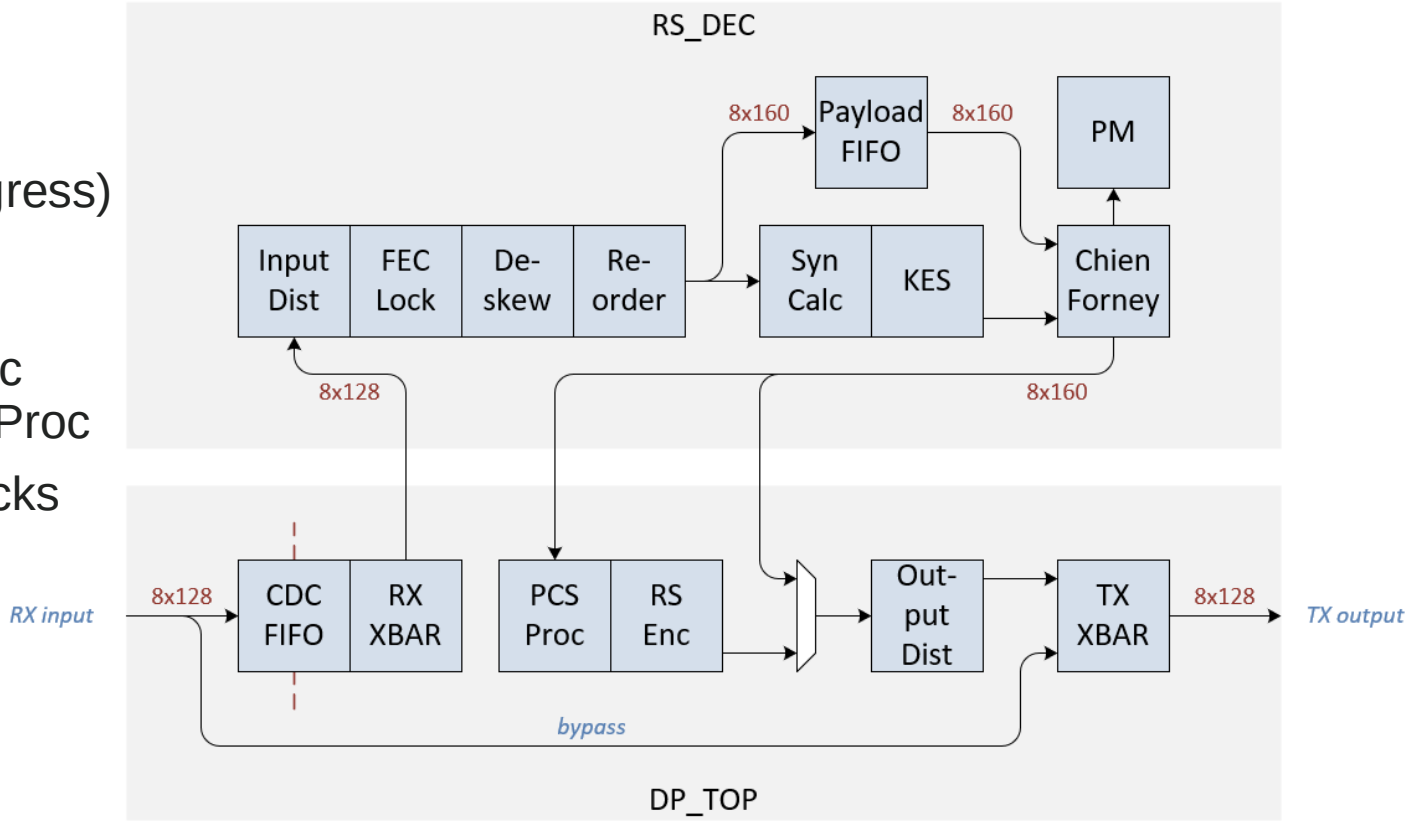
- Complete list in RSDEC_FEC_STATUS_CNT_ACCESS register description.

FEC Statistics

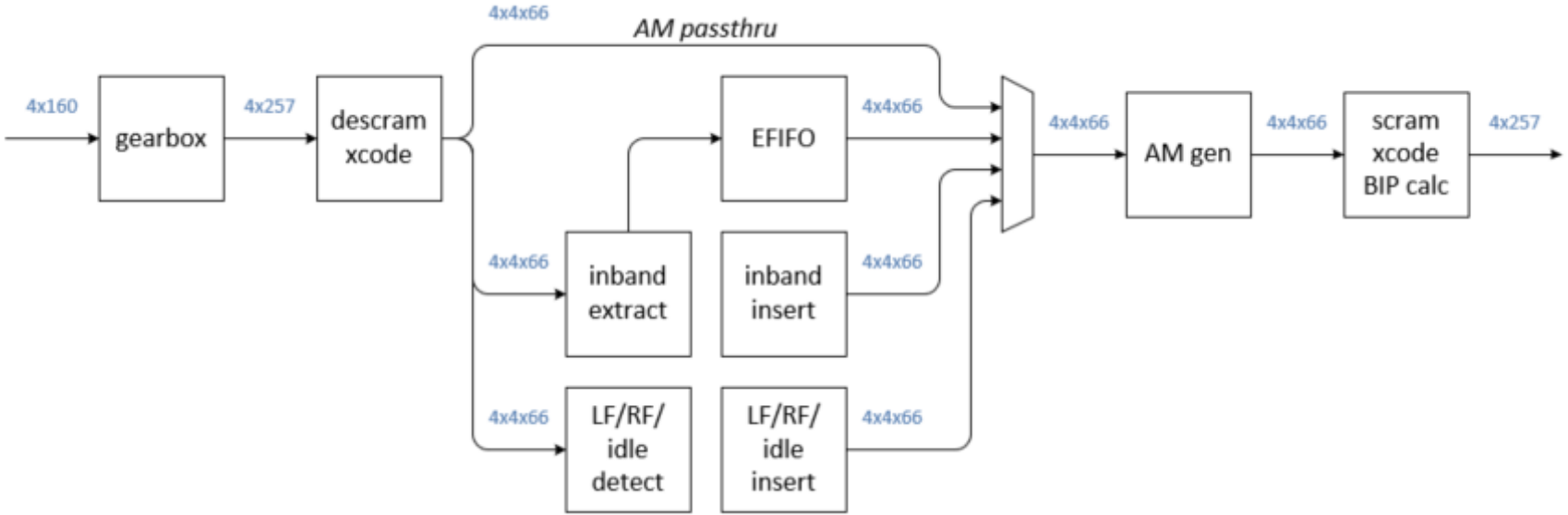
- Statistics are latched using a snapshot trigger. Three sources:
  - snapshot_en pin (controlled by chip level)
  - Local register (RSDEC_SNAPSHOT_CFG)
  - Timer (RSDEC_SNAPSHOT_TMR_CFG)
- A snapshot transfer active counts to latched counts and clears the active counts.
- Software accumulates the latched counts.

Spica5n FEC Block Diagram

- Two instances (ingress and egress)
- Datapaths:
  - Bypass
  - With PCS Proc
  - Without PCS Proc
- RX and TX blocks not shown

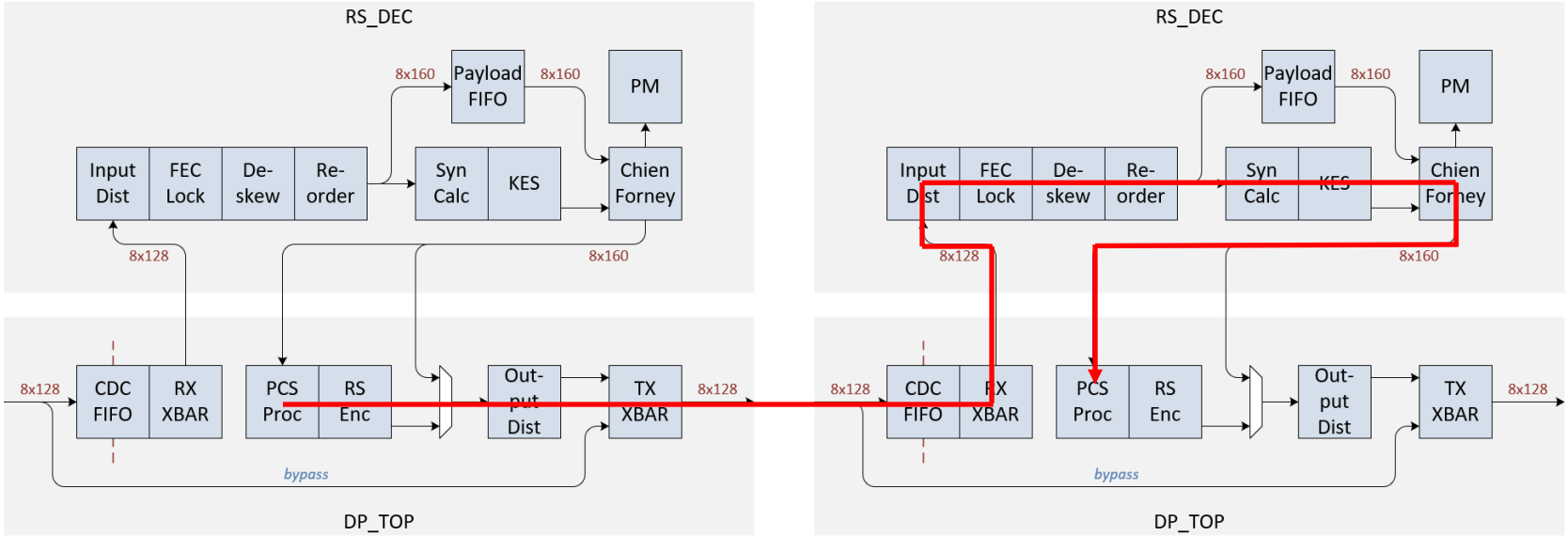


Spica5n PCS Processing Block Diagram



FEC Generation / Monitoring Simulation

- Two DUT instances, one for generation and one for monitoring.



FEC Generation / Monitoring Simulation

- Uses the pattern generator and pattern monitor in the inband block.
- The inband block can generate and monitor only one channel.
- The TX XBAR can be used to broadcast the channel.
- The testbench does not inject any FEC errors.

FEC Generation / Monitoring Simulation

- The testbench shows how to:
  - Configure the FEC monitor.
  - Configure the pattern generator.
  - Configure the pattern monitor.
  - Check lock status.
  - Check FEC statistics.
  - Check pattern monitor status.

FEC Generation / Monitoring Simulation

- Testbench checked in to SVN spica5n_A/trunk/frontend/modules/w_rs_dec/sim/pat_gen_mon
- To run a test:
  1. cd frontend/modules/w_rs_dec/sim/pat_gen_mon
  2. make *(builds testbench files)*
  3. make dump *(runs simulation and dumps waves)*
  4. make waves *(opens waveform viewer)*
- Edit the value of ‘mode’ for different FEC modes.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