APV21B - Performance Evaluation

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INTRODUCTION

The APV21B Real-time Video 16X Bicubic Super-resolution core is a soft IP core. It provides fully real-time 16X Bicubic interpolation video super-resolution, and its high performance design allows it to support video output resolutions in excess of 4K 60FPS.

The APV21B is compatibled with the AXI4-Stream Video protocol as described in the **Video IP: AXI Feature Adoption** section of the *Vivado AXI Reference Guide* (Xilinx Inc. UG1037) and **AXI4-Stream Signaling Interface** section of the *AXI4-Stream Video IP and System Design Guide* (Xilinx Inc. UG934).

This document is part of the IP user manual and is intended to describe the maximum achievable performance of this IP on several devices. Complete technical documentation can be found in the User's Manual for this IP.

1 Performance

The Real-time Video Bicubic Super-resolution IP is benchmarking by timing analysis tools in Vivado and Synopsys Synplify Premier. The parameters used in the benchmark test were configured as follows

- Input Video Width: 960
- Input Video Height: 540

Table 1 shows the results of the maximum frequencies benchmark.

FPGA Device Family	**Analysis Tool**	**Fmax (MHz)**
Xilinx Virtex UltraScale+	Synopsys Synplify Premier 2020.03[1]	628.6
Xilinx Kintex UltraScale+	Synopsys Synplify Premier 2020.03[1]	417.2
Xilinx Zynq UltraScale+	Vivado 2021.1[1][2]	428.4
	Synopsys Synplify Premier 2020.03[1]	394.1
Xilinx Kintex 7	Synopsys Synplify Premier 2020.03[3]	361.7
Xilinx Artix 7	Synopsys Synplify Premier 2020.03[3]	192.2
Intel Stratix 10	Synopsys Synplify Premier 2020.03[3]	260.7
Intel MAX 10	Synopsys Synplify Premier 2020.03[3]	220.5
Intel Arria V	Synopsys Synplify Premier 2020.03[3]	142.5

Table 1: Maximum Frequencies

2 Latency

Table 2 shows the Real-time Video Bicubic Super-resolution IP latency cycles measured on real-time video path. It does not include system dependent latency or throttling. Suppose the width of the input video frame is W.

Description	**Clocks**
Bicubic pipeline input to output	13
First pixel input to First pixel (group) output	$10 \cdot W + 28$
Last pixel input to last pixel (group) output	$13 \cdot W + 31$

Table 2: Latency

[1] Using DSP48E2 Macro.
[2] Using XPM Macro.
[3] Using pure Verilog inferring synthesis.

3 Throughput

Table 3 shows the Real-time Video Bicubic Super-resolution IP throughput measured for different input frame size.

Input Resolution	**Output Resolution**	**Throughput (FPS/MHz)**	**FPS @150MHz**
320 x 240	1280 x 960	3.23	484.7
480 x 270	1920 x 1080	1.92	287.6
640 x 360	2560 x 1440	1.08	162.1
960 x 540	3840 x 2160	0.48	72.1

Table 3: Throughput

4 Resource Utilization

Table 4 shows the Real-time Video Bicubic Super-resolution IP resource utilization on specified FPGA devices with specified settings for reference.

Resource utilization results of Xilinx Zynq UltraScale+ devices is evaluated under with Vivado synthesizer and using DSP48E2 and XPM Macros. The evaluation result of other devices are complete using Verilog automatically inferring, may different caused by the difference of data width of DSP module of each device. The Real-time Video Bicubic Super-resolution IP is specially optimized for DSP48E2 block of Xilinx UltraScale+ series devices. In order to maximum the resource utilization, it is recommended to use these devices for synthesis.

Device	**Configuration Parameters**		**Resource Utilization**			
	Input Resolution	**fCLK (MHz)**	**LUTs**	**FFs**	**DSPs**	**BRAMs**
XCZU15EG	960 x 540	300	431	694	49[1]	2.5[3]
XC7K325T	960 x 540	150	1979	2713	30[2]	2[3]

Table 4: Resource Utilization

[1] Xilinx UltraScale+ architecture DSP48E2 unit
[2] Xilinx 7 series FPGA DSP48E1 unit
[3] Xilinx FPGA Block RAM 36K unit

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