APV21B - Simulation & Verification Enviroment

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INTRODUCTION

The APV21B Real-time Video 16X Bicubic Super-resolution core is a soft IP core. It provides fully real-time 16X Bicubic interpolation video super-resolution, and its high performance design allows it to support video output resolutions in excess of 4K 60FPS.

The APV21B is compatibled with the AXI4-Stream Video protocol as described in the **Video IP: AXI Feature Adoption** section of the *Vivado AXI Reference Guide* (Xilinx Inc. UG1037) and **AXI4-Stream Signaling Interface** section of the *AXI4-Stream Video IP and System Design Guide* (Xilinx Inc. UG934).

The purpose of this document is to describe the construction, implementation and operation of the simulation and verification platform used in this IP, and to present the simulation results. Complete technical documentation can be found in the User Manual for this IP.

1 Verification Platform Overview

The APV21B Real-time Video 16X Bicubic Super-resolution IP is a dedicated IP for image processing, and a bottom-up layered verification and UVM-like verification platform is used to verify the correct functionality of the IP.

To improve the algorithm verification coverage and accuracy, a mixed random + extreme verification pattern is used for the verification of computation units. The *AXI-Stream Video Image VIP* is used for bus transaction driving and monitoring for the overall verification of the IP, and a mixed verification pattern of preset bitmaps and random bitmaps is used.

The verification of the underlying arithmetic unit is performed by the SystemVerilog non-synthesizable subset for reference arithmetic and comparison. The overall verification of the IP is done by the external C model reference program and the pixel comparison program.

The block diagram of the verification platform is shown in Figure 1 and Figure 2.

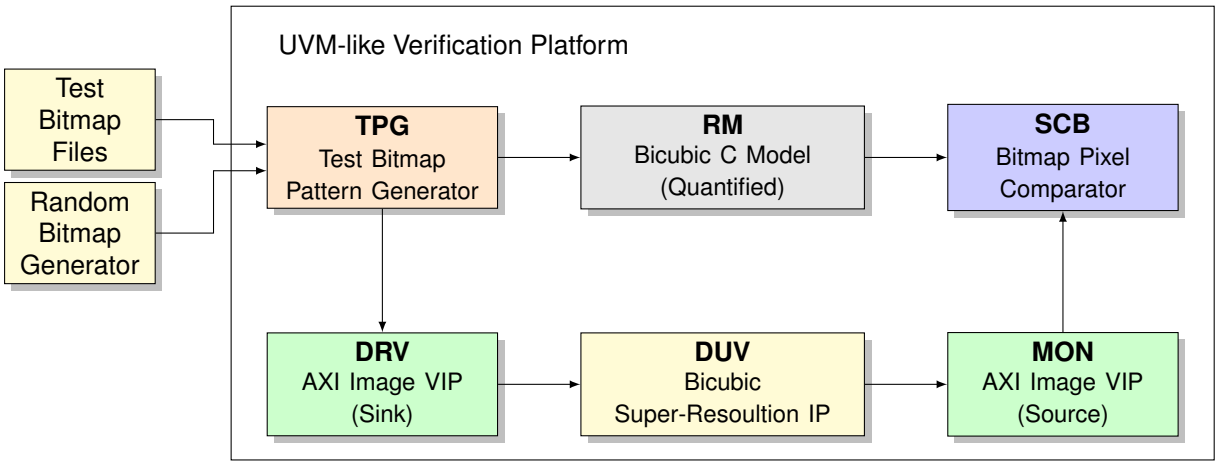

Figure 1: Diagram of UVM-like Verification Platform (Overall IP)

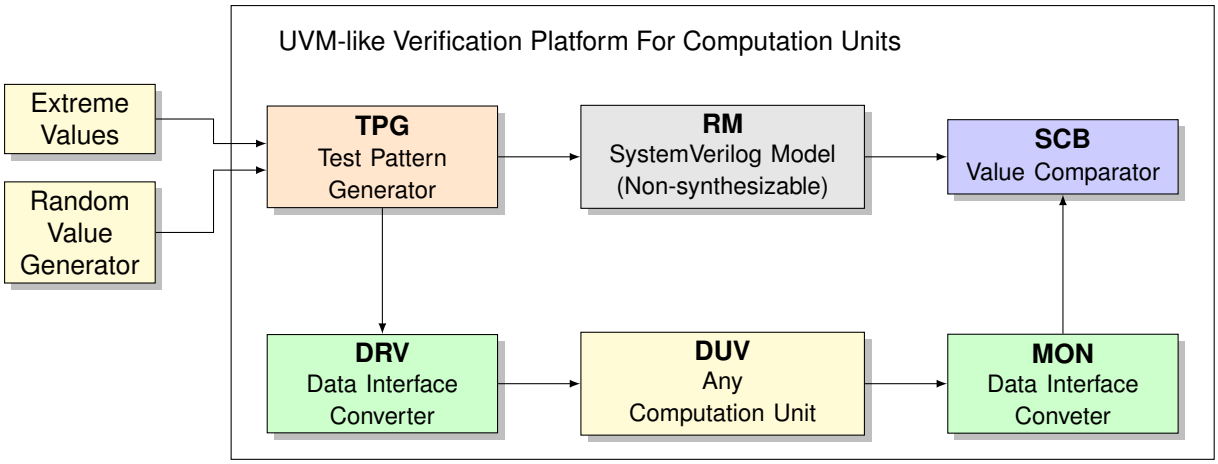

Figure 2: Diagram of UVM-like Verification Platform (Computation Units)

1.1 Software Platform

The detail information of the software platform used for IP verification is shown in Table 1.

Table 1: Software Verification Platform

Software Name	Mentor Modelsim
Version	2020.04
Referenced Libraries	Xilinx Secure IP, Xilinx XPM, Xilinx Unisims Verilog

1.2 Verification Methodology

The detail information of the verification methodology of this IP is shown in Table 2.

Table 2: Verification Methodology

Verification Language	System Verilog
Reference Model Language	System Verilog, C
Verification Platform	System Verilog Implemented, UVM-like
Test Patterns	Random Values, Extreme Values, Real-world Bitmaps

1.3 Verification Plan

The detail information of the verification plan of this IP is shown in Table 3.

Table 3: Verification Plan

Design Under Test	**Test Pattern**	**Count of Patterns**
Overall IP	Real-world Bitmap	60
	Random Bitmap	100
Multiplier Adder Unit	Extreme Values	1296
	Random Values	50000
8-input Add Unit	Extreme Values	104976
	Random Values	200000
Round Unit	Extreme Values	36
	Random Values	1000
Limit Unit	Extreme Values	3
	Random Values	1000
Overall Pipeline	Extreme Values	147456
	Random Values	200000

2 AXI-Stream Video Image VIP

The AXI-Stream Video Image VIP using the bitmap processing library which can read and write windows bitmap files (.BMP) into a bit array (virtural memory) by System Verilog for IP Verfication. The "axi_stream_video_image_in_vip" IP can read a bitmap file into the memory, and send it by a AXI-Stream Video Interface (Defined in Xilinx User Guide UG934). And the "axi_stream_video_image_out_vip" IP can monitor a AXI-Stream interface, obtain a frame which transmitting on the interface and save it to a bitmap file.

Please refer this GitHub Link (https://github.com/Aperture-Electronic/SystemVerilog-Bitmap-Library-AXI-Image-VIP) for detailed information of this important VIP in the verification platform.

The verifaction IP and the bitmap processing library were developed by the Nijigasaki IC Design Club.

3 Test Result

The detailed result report of the verification is shown in Table 4.

Table 4: Test Result

Design Under Test	**Test Pattern**	**Tested**	**Mismatched**	**Pass/Fail**
Overall IP	Real-world Bitmap	60	0	Pass
	Random Bitmap	100	0	Pass
Multiplier Adder Unit	Extreme Values	1296	0	Pass
	Random Values	50000	0	Pass
8-input Add Unit	Extreme Values	104976	0	Pass
	Random Values	200000	0	Pass
Round Unit	Extreme Values	36	0	Pass
	Random Values	1000	0	Pass
Limit Unit	Extreme Values	3	0	Pass
	Random Values	1000	0	Pass
Overall Pipeline	Extreme Values	147456	0	Pass
	Random Values	200000	0	Pass

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