RTS Measurement Progress Report

This report covers the progress made in measuring RTS for Skywater's DOE 1 test chip that utilizes an on-chip architecture, shown in figure 4, to access individual test cells. By designing an on-chip architecture to index specific devices, it is possible to exponentially increase the number of devices test during a given time frame. For this setup, the maximum number of devices characterized for their DC characteristics during a single test run is 3,072. The test run for these devices lasted approximately 11 hours and captured the source voltage at the device, which allowed for calculations of the gate source voltage, the transconductance, and the threshold voltage. A similar test is planned for RTS measurements but hasn't been completed yet due to the complex nature of the measurements.

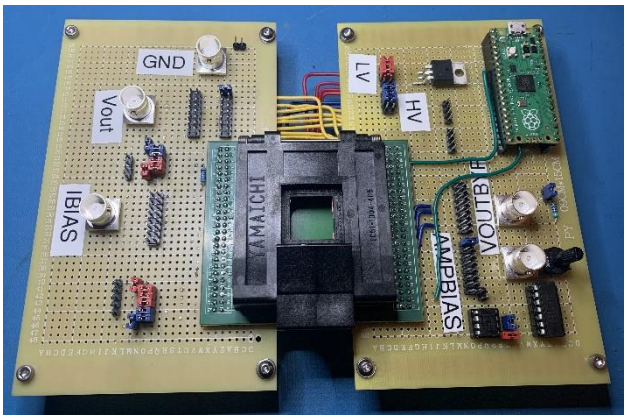

Figure 1: RTS measurement board V2

To test chiplet 3 on the DOE1 RTS measurement test chip, a board had to be created to house and power the chip as well as send signals to activate and deactivate the on-chip architecture. The signals that are generated and sent to the test chip come from a Raspberry Pi Pico with dual M4 cortex processors that is running at a default 133 MHz clock speed, which is connected to an LCC 100 pin socket via protoboard. Even though this setup is still in the prototype stage, it allows for DC characterizations of the on-chip components and preliminary RTS measurements.

To turn the DOE1 RTS test chip on, there are two voltage levels that must be applied to the power pins on the chip. These voltage levels are 1.2 volts for the low voltage and 3.3 volts for the high voltage. Each voltage level has four input pins on the chip and it is possible to verify their functionality by applying the respective voltage to one of the pins and measure the voltage available on the remaining pins. For chip 6p 3, when a 3.2572v is applied to the high voltage power pins we record 3.2524 volts on the remaining pins which shows a functioning device. Applying 1.1961 volts to the low voltage power rail, we measure 1.1961 volts which also indicates a functioning device. Although this step may seem trivial it was crucial making progress to making further characterizations and RTS measurements.

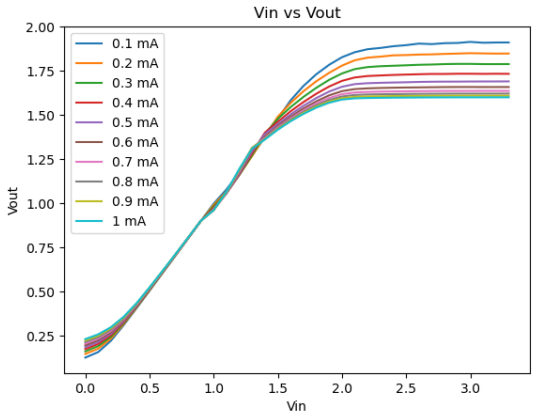

Figure 2: Op Amp characterization

The eight on-chip operational amplifiers (OP Amps) are used to amplify the output voltage that is measured from the source terminal of the device under test (DUT). To characterize the op amps, there is a bias current applied to the amp bias pin, the shift registers are held in the reset position, and the output bypass pin on the chip is activated. By activating the bypass pin, it is possible to sweep different voltages through the op amp and measure the output on the other side. With the op amp connected in a unity gain configuration, the voltage sweep that was used varied from 0 to 3.3 volts in 0.1-volt increments. To better characterize the op amps, the current being applied to the amp bias was swept from 0 amps to 1 milliamp in 0.1 amp increments while sweeping the voltage for each increment. Figure 2 shows the results of the characterizations and that the on chip operational amplifiers provide a linear region of operation between 0.3 V and 1.8 V. While this region is slightly less than necessary to reach a 1:1 input/output for the higher voltage levels on the chip, it is an excellent device for the lower voltage levels. The characterizations also show that the amp bias currents have an almost negligent effect on the op amps gain while the bias current is high enough for the amp to be powered on.

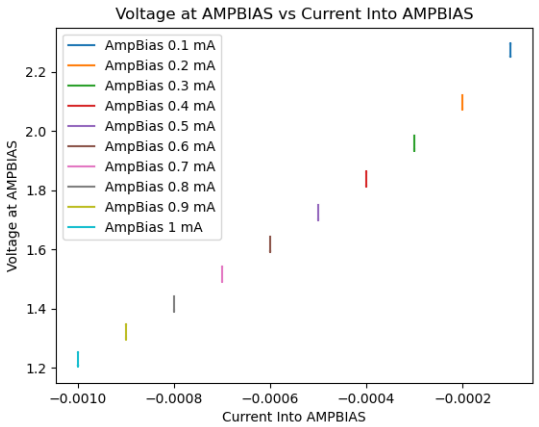

Figure 3: Voltage change in the op amp for different values of current.

When configured for normal operation, the op amps positive input pin is connected to the source terminal of the device under test and the negative input is connected to the output so that the device is configured for unity gain feedback. To select a device from the array, two shift registers have to be sent instruction sets by clocking the data through their independent input pins. Once a device is selected by row and column we are able to characterize the on chip current sources by sweeping the bias current and monitoring the output through the op amp that is biased with 0.5 mA. The current sweep ranges from 100pA to 50uA, which creates a voltage drop that appears on the source terminal of the voltage follower. The recorded voltage drop is then used to characterize the current source by calculating Vgs, Vth and the transconductance (Gm). This process is repeated for each device in the bank (96 rows X 32 columns) that the measurement board is configured to test. Containing 16 different types of transistors, each bank varies in widths and lengths and are configured as source followers that can be tested and characterized through the on-chip architecture. Figure 5 below shows that the device is functioning as intended because the measured data and simulation data match closely. As

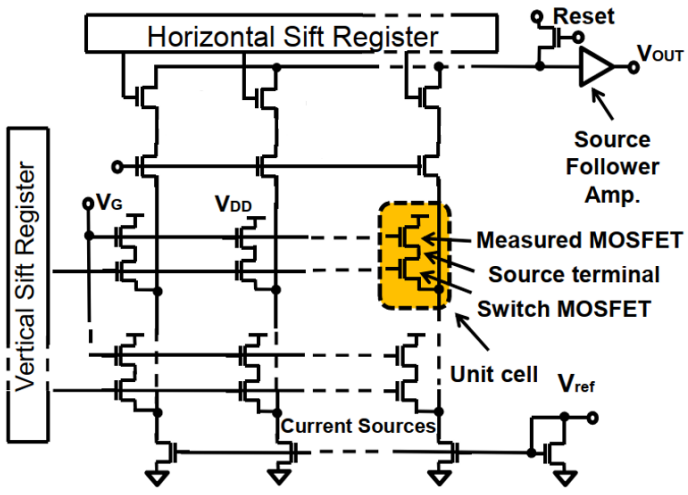

Figure 4: On chip test architecture

mentioned above, the banks are grouped into 16 different transistor types by width and lengths. These groupings are done by columns, meaning that the types change every two columns. So, for all the rows in column 0 and 1 the devices have the same widths and lengths. This is beneficial because it will allow for characterizations of process variability when the data is superimposed into one graph as shown in Figure 6.

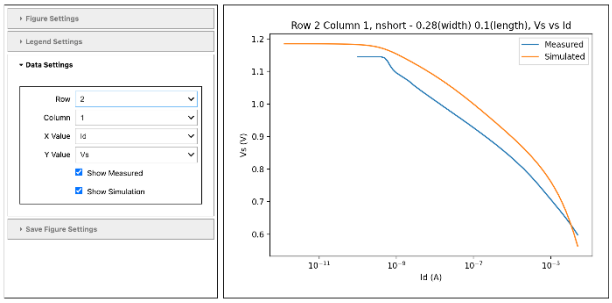

Figure 5: Simulated and measured data of Id vs Vs Characterization for a transistor with W/L of 0.28/0.1.

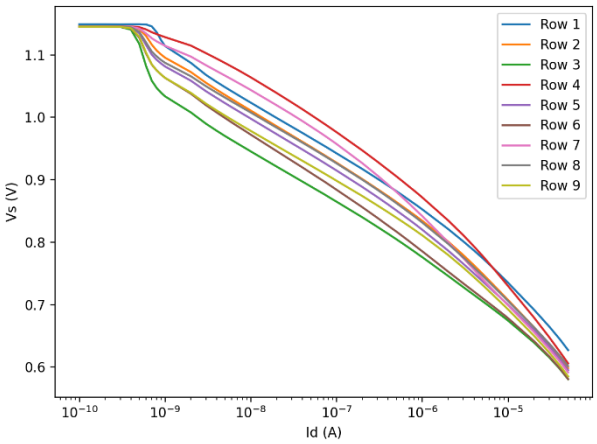

Figure 6: Superimposed graphs of transistors with the same widths and lengths.