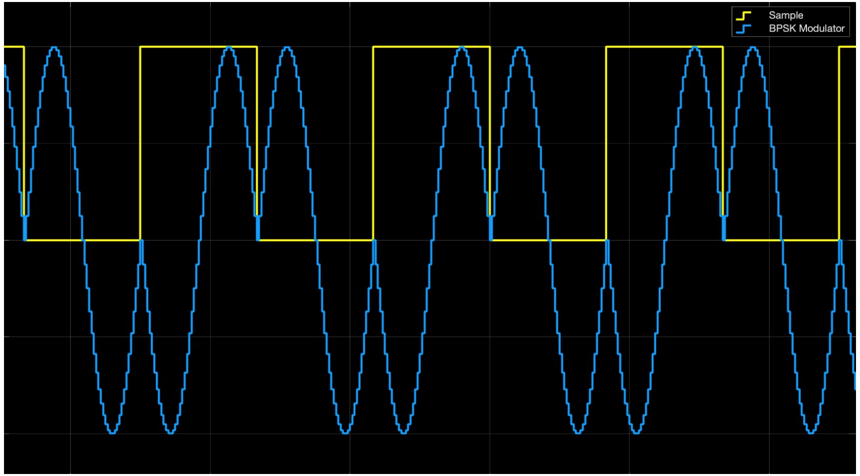

End-to-end System Modeling

Analog Digital Communication

December 14, 2020

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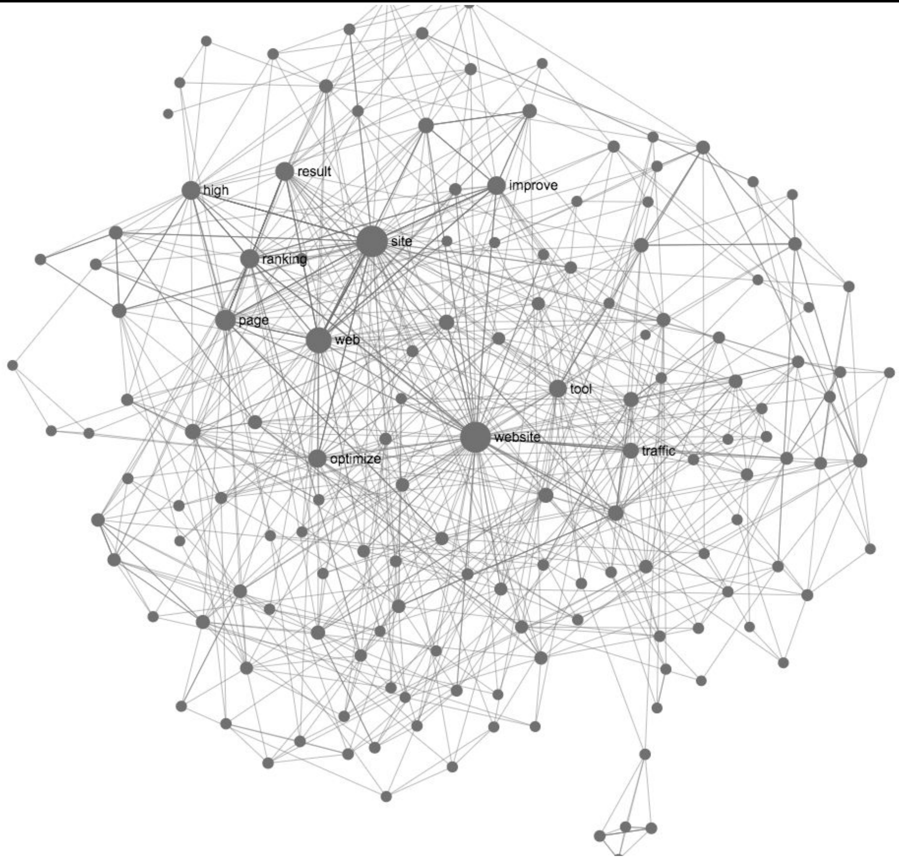
Goals

Gain **practical experience** in designing a **complete** communications system.

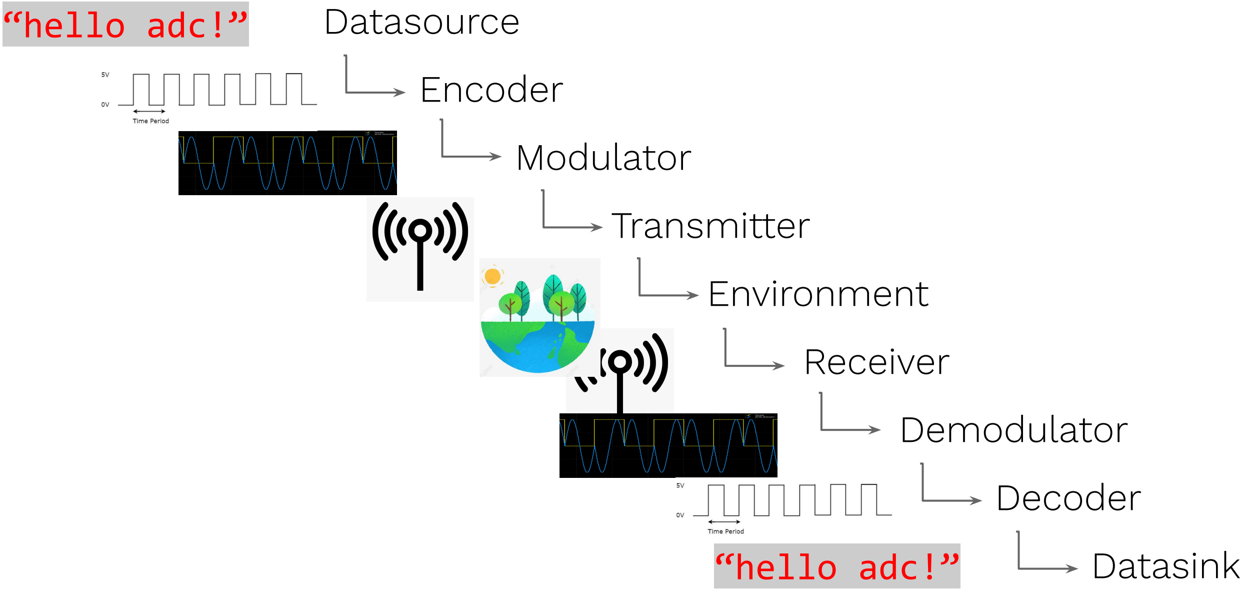
Understand the **practical** and **physical** considerations of implementing a **hardware** communications system.

Learn more about digital communication protocols at the **MAC layer**, including packet **encoding** and **error correction**.

Design a BPSK system in Simulink



System Design: Overview



Datasource

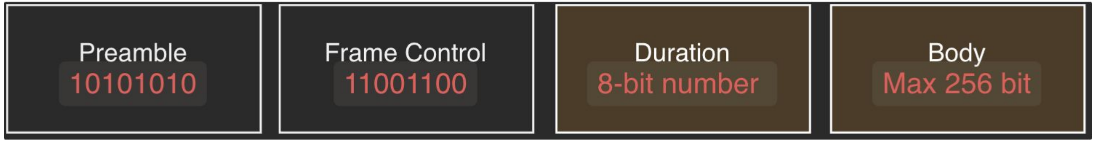
- Payload data is converted to a binary format and stored into a collection of registers.
- We used the “Timetable” Simulink data load option to mimic a microntronoller’s buffer and queue

- Data is pre-encoded using Hamming codes.
- MAC layer is implemented at the queue level.

```
Fc = 2.4e9;
Tb = 1/Fc;
wperiod = 50;
SampSin = Tb/wperiod;
tau = 1/(2*pi*(Fc+1e9));
loss = Fc*1000;

% Create Packet For Sending
random_additions = 'asdf';
bitlist = get_bits('HELLO');
encoded = hammingEncode(bitlist);
packet = createPacket(encoded, random_additions);
bits = createTimetable(Tb, packet);
```

Encoder

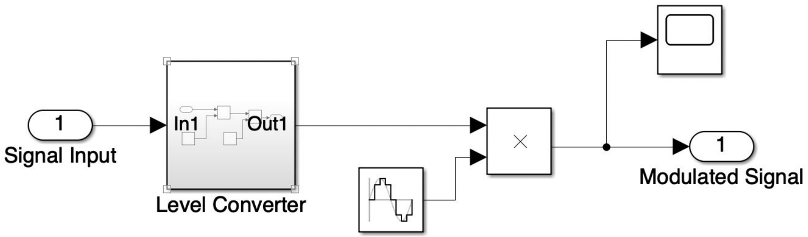
- Used a very simple layout for packet construction.
- **Preamble**: the “syncword” for receivers to listen for and synchronize to.
- **Frame** control: the “API version” of the packet layout for receivers to understand if they can parse the packet.
- **Duration**: 8-bit (padded) hamming encoded body length.
- **Body**: variable-length, hamming encoded packet body.

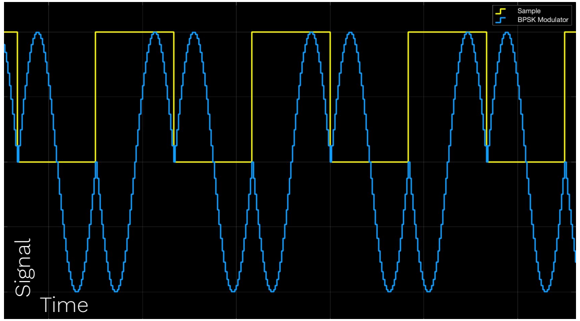



```
function packet = createPacket(bitstring, random_additions)

% bits: list of bits for the data section of the packet
% Build a packet as shown in the paper.

preamble = [1, 0, 1, 0, 1, 0, 1, 0]';
frame_control = [1, 1, 0, 0, 1, 1, 0, 0]';

calculated_length = length(bitstring);
len = pad(dec2bin( calculated_length ), 8, 'left', '0');
duration = str2num(reshape(len.', [], 1));

body = bitstring;
ending_error = get_bits(random_additions);
packet = vertcat(preamble, frame_control, duration, body, ending_error);
```

Modulator

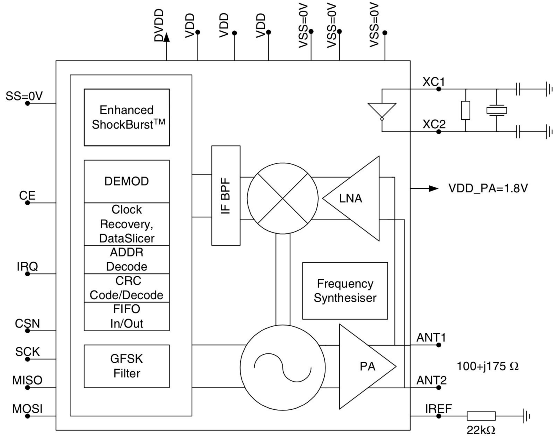
- Implements a Binary Phase Shift Keying (BPSK) modulation scheme.
- **Upsampler**: locks and holds digital signal to the specified bit rate
- **Level Converter**: converts 1/0 signal into 1/-1
- **Mixer**: combines level-converted digital signal with 2.4 GHz carrier wave
- Carrier wave is phase aligned with the bit period.





Transmitter

- Selected a **nRF24L01** 2.4 GHz transceiver as the real-world hardware implementation.
- Used for transmitter characteristics in Simulink, Represented as transfer function P(f).



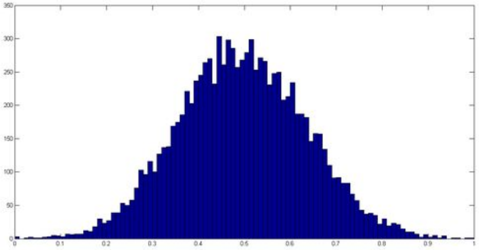
	General RF conditions					
f_{OP}	Operating frequency	2	2400		2525	MHz
f_{XTAL}	Crystal frequency			16		MHz
Δf_{1M}	Frequency deviation @ 1000kbps			±160		kHz
Δf_{2M}	Frequency deviation @ 2000kbps			±320		kHz
R_{GFSK}	Data rate ShockBurst™		>0		2000	kbps
$F_{CHANNEL}$	Channel spacing @ 1000kbps			1		MHz
$F_{CHANNEL}$	Channel spacing @ 2000kbps			2		MHz
	Transmitter operation					
P_{RF}	Maximum Output Power	3		0	+4	dBm
P_{RFC}	RF Power Control Range		16	18	20	dB
P_{RFCR}	RF Power Accuracy				±4	dB
P_{BW}	20dB Bandwidth for Modulated Carrier (2000kbps)			1800	2000	kHz
P_{RF1}	1st Adjacent Channel Transmit Power 2MHz				-20	dBm
P_{RF2}	2nd Adjacent Channel Transmit Power 4MHz				-50	dBm
I_{VDD}	Supply current @ 0dBm output power	4		11.3		mA
I_{VDD}	Supply current @ -18dBm output power			7.0		mA
I_{VDD}	Average Supply current @ -6dBm output power, Enhanced ShockBurst™	5		0.05		mA
I_{VDD}	Supply current in Standby-I mode	6		32		µA
I_{VDD}	Supply current in power down			900		nA

Environment

- A combination of free space power loss:

$$FSPL = 20\log_{10}(d) + 20\log_{10}(f) + 20\log_{10}\left(\frac{4\pi}{c}\right) - G_t - G_r$$

- Also includes Gaussian white noise with PSD of 2e-20 Watts/Hz



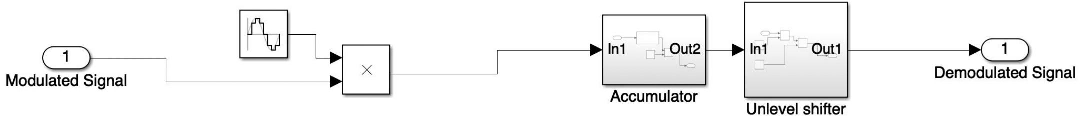
Receiver

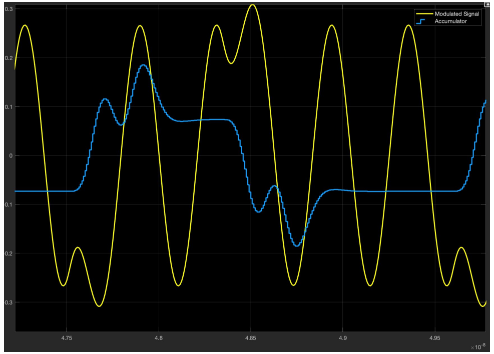
- Represented as a transfer function with coefficients derived from the nRF24L01.

	Receiver operation					
I_{VDD}	Supply current one channel 2000kbps			12.3		mA
I_{VDD}	Supply current one channel 1000kbps			11.8		mA
RX_{SENS}	Sensitivity at 0.1%BER (@2000kbps)			-82		dBm
RX_{SENS}	Sensitivity at 0.1%BER (@1000kbps)			-85		dBm
C/I_{CO}	C/I Co-channel (@2000kbps)	7		7[8]/11[9]		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 2MHz			1/4		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 4MHz			-21/-20		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 6MHz			-27/-27		dB
C/I_{CO}	C/I Co-channel (@1000kbps)	10		9[11]/12[12]		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 1MHz			8/8		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 2MHz			-22/-21		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 3MHz			-30/-30		dB

Demodulator

- Uses the thresholded windowed-integrator method for decoding BPSK signal data from the receiver.
- Rounding is used to threshold the values to +1/-1
- A zero-order-hold then samples the integrated signal at the bit rate.
- Decoding is triggered by a thresholded match filter using Simulink callbacks.





Demo! 🎉

Thanks!

Hardware exploration

- Selected a 2.4 GHz Large Duck Antenna
- 5dBi, Reverse Polarized.
- 50 ohm impedance.
- nRF24L01 2.4 GHz transceiver IC.