FD2203

250V Half-bridge gate driver

Outline

FD2203 It is a half-bridge gate drive circuit chip,

Designed for high voltage, high speed driving N Power MOSFET

with IGBT It can be up to + 250V Work under voltage.

FD2203 Built-in undervoltage (UVLO)Protective function,

Preventing the power transistor operates at low voltage and improve efficiency.

FD2203 Built-in filtering the input signal, the input noise preventing

Sound interference.

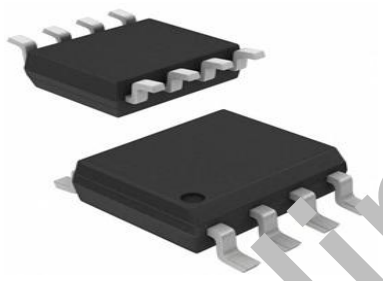
FD2203 Built-in pass-through to prevent and dead time, preventing

Power tube through occurs, the effective protection of the power device.

Features

- Suspension absolute voltage + 250V
- Output current + 1.6A / -2.3A
- 3.3V / 5V Input logic compatible
- VCC / VBS Undervoltage protection (UVLO)
- High-end and high-end output in phase with the input
- Low-side and low-side input inverter output
- Built-in pass-through prevention function
- Internal 250ns Dead time
- Channel matching high and low end

Package



SOIC-8

application

Motor drive

DC-DC converter

Ordering Information

Product Name	Package Ordering	
FD2203	SOIC-8	FD2203

1. Absolute Maximum Ratings (Unless otherwise noted, all pins are COM As a reference point)

parameter		symbol	range	unit
A high side floating absolute voltage		V_B	-0.3 ~ 275	V
A high side floating offset voltage		V_S	V_B- 25 ~ V_B + 0.3	V
High-side output voltage		V_{HO}	V_S- 0.3 ~ V_B + 0.3	V
The low side supply voltage		V_{CC}	-0.3 ~ 25	V
Low-side output voltage		V_{LO}	-0.3 ~ V_{CC} + 0.3	V
Logic input voltage (HIN, LIN *)		V_{IN}	-0.3 ~ V_{CC} + 0.3	V
Offset voltage slew rate range		dVs / dt	≤ 50	V / ns
Power Dissipation @ T_A ≤25 • C	SOIC-8	P_D	≤ 0.625	W
Thermal resistance junction on the environment	SOIC-8	R_{thJA}	≤ 200	• C / W
Junction Temperature Range		T_j	≤ 150	• C
Storage temperature		T_{stg}	- 55 ~ 150	• C

Note 1 : In any case, do not exceed P_D . Note 2 : Voltage exceeds the absolute maximum ratings may damage the chip.

2. Recommended Operating Conditions (All voltages are COM As a reference point)

parameter	symbol	Minimum	Maximum	unit
A high side floating absolute voltage	V_B	V_S +	V_S + 20	V
A high side floating offset voltage	V_S		250	V
High-side output voltage	V_{HO}	V_S	V_B	V
The low side supply voltage	V_{CC}	8	20	V
Low-side output voltage	V_{LO}	0	V_{CC}	V
Logic input voltage (HIN, LIN *)	V_{IN}	0	V_{CC}	V
Ambient temperature	T_A	- 40	125	• C

Note 1 : V_S for(COM-2V) To 250V Time, H normal V V_S fo OM-2V) To (COM-V_{BS})Time, HO Logic state remains. Note 2 : V_S for(COM-50V),width 50ns The negative voltage transient, HO normal work. Note 3 : Chip long-term work outside recom nded operating conditions may affect its reliability, the chip is not recommended for long-term work outside the recommended operating condition

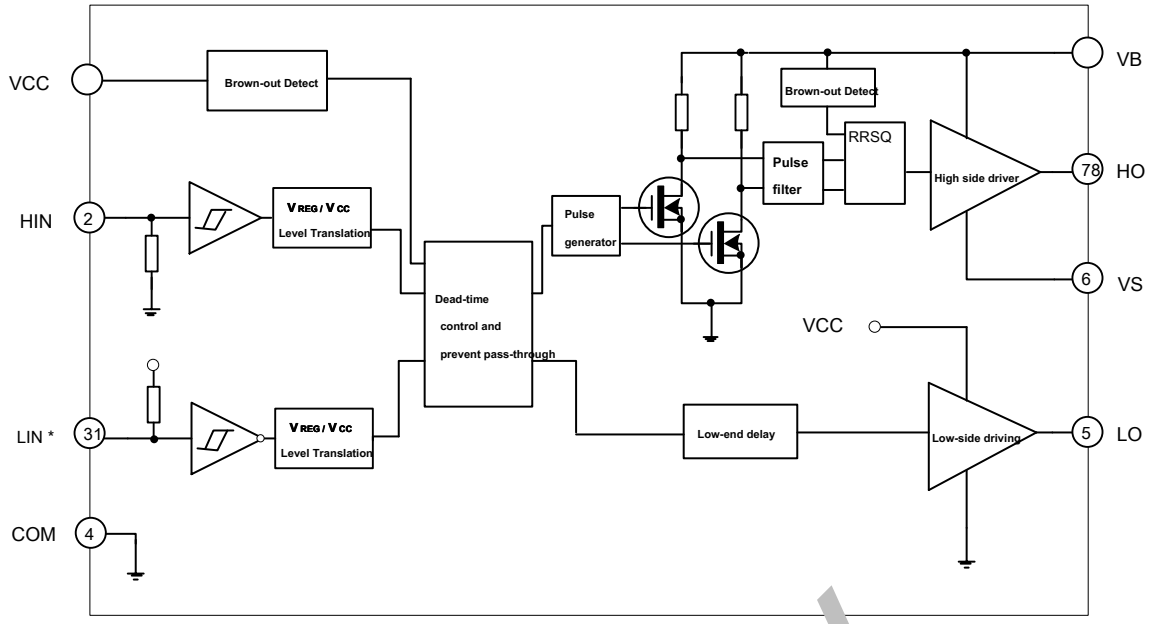
3. static electrical parameters (Unless otherwise specified, T_A = 25 • C , V_{CC} - V_{BS} = 15V , V_S - COM)

parameter	symbol	Test Conditions	Min	Typ	Max	Units
High level input threshold voltage	V_{IH}		2.4	--	--	V
Low level input threshold voltage	V_{IL}		--	--	0.8	V
V_{CC} Undervoltage protection voltage trip	V_{CCUV+}		6.3	6.9	7.5	V
V_{CC} Reset voltage undervoltage protection	V_{CCUV-}		5.9	6.5	7.1	V
V_{CC} Hysteresis voltage undervoltage protection	V_{CCUVH}		0.2	0.4	--	V
V_{BS} Undervoltage protection voltage trip	V_{BSUV+}		6.3	6.9	7.5	V
V_{BS} Reset voltage undervoltage protection	V_{BSUV-}		5.9	6.5	7.1	V
V_{BS} Hysteresis voltage undervoltage protection	V_{BSUVH}		0.2	0.4	--	V
Floating power supply leakage current	I_{LK}	V_B = V_S = 250V	--	1.0	10.0	µA
V_{BS} Quiescent Current	I_{QBS}	V_{IN} = 0V or 5V	--	140	250	µA
V_{BS} Dynamic current	I_{PBS}	f_{HIN} = 20kHz	--	140	250	µA
V_{CC} Quiescent Current	I_{QCC}	V_{IN} = 0V or 5V	---	460	700	uA
V_{CC} Dynamic current	I_{PCC}	f_{IN} = 20kHz	---	460	700	µA
LIN * High input bias current	I_{LIN+}	V_{LIN*} = 0V	---	20	40	µA
LIN * Low input bias current	I_{LIN-}	V_{LIN*} = 5V	--	2		µA
HIN High input bias current	I_{HIN+}	V_{HIN} = 5V	---	20	40	µA
HIN Low input bias current	I_{HIN-}	V_{HIN} = 0V	--	--	2	µA
High-level output voltage	V_{OH}	I_O = 20mA	--	0.09	0.16	V
Low Output Voltage	V_{OL}	I_O = 20mA	--	0.03	0.06	V
High short circuit output current pulse	I_{OH}	V_O = 0V , PW≤10µs	1.1	1.6	--	A
Low short circuit output current pulse	I_{OL}	V_O = 15V , PWD≤10µs	1.6	2.3	--	A
V_S Static negative pressure	V_{SN}		--	-6.0	--	V

4. Dynamic electrical parameters (Unless otherwise specified, T_A = 25 • C , V_{CC} - V_{BS} = 15V , C_L = 1000pF , V_S - COM)

parameter	symbol	Test Conditions	Min	Typ	Max	Units
The rising edge transit time	t_{on}	C_L = 1000pF	---	350	520	ns
Falling output transmission time	t_{off}	C_L = 1000pF	---	100	150	ns
Output Rise Time	t_r	C_L = 1000pF	---	12	--	ns
Output Fall Time	t_f	C_L = 1000pF	--	8	--	ns
Dead time	DT		--	250	370	ns
Delay matching the high and low side	MT		--		---	50 ns

The block circuit diagram



6. chip pin configuration

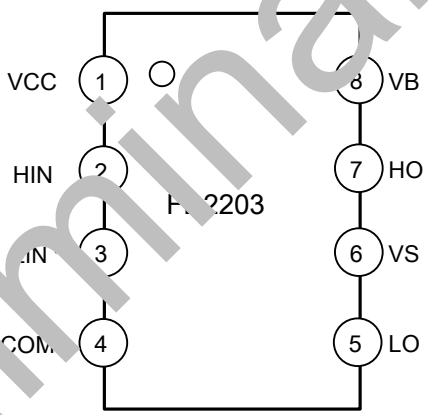
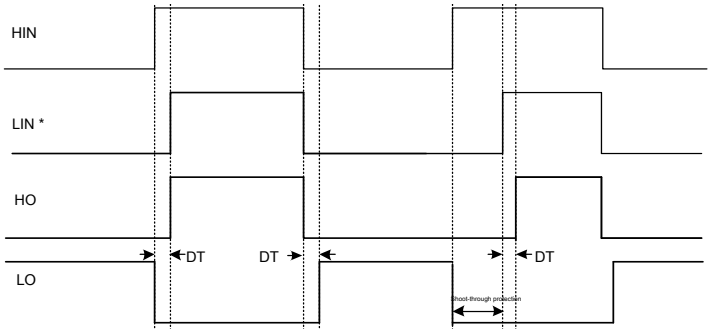


FIG package pins 6-1 of FIG.

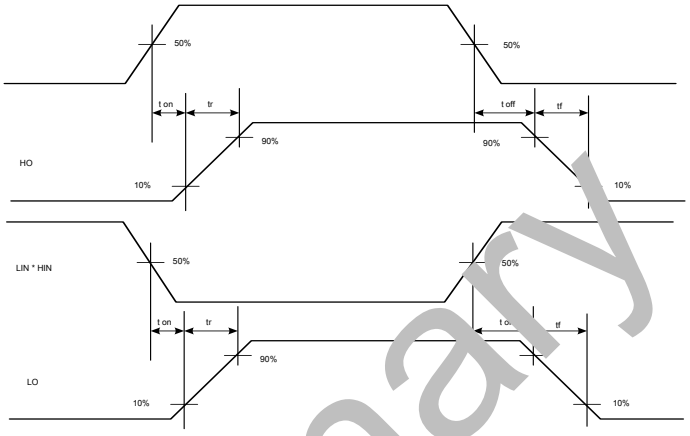
Table 6-1 Pin Description

Number	Name	Pin Description
1	VCC	The low side supply voltage
2	HIN	A high side
3	LIN *	Low-side input
4	COM	Ground
5	LO	Low-side output
6	VS	A high side floating offset voltage
7	HO	High-side output
8	VB	A high side floating absolute voltage

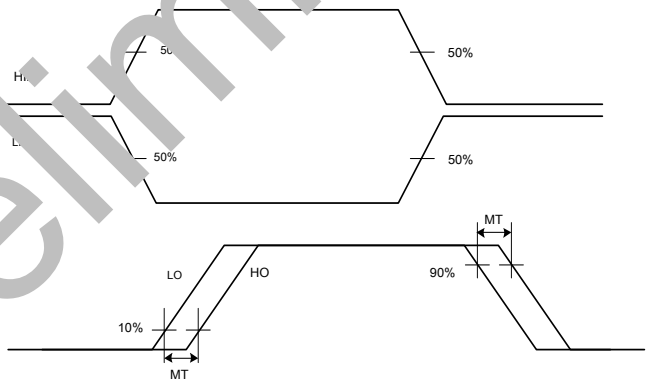
7. FIG logic timing



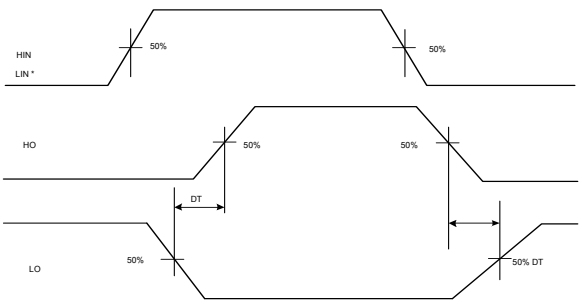
8. Switching Time Test Standard



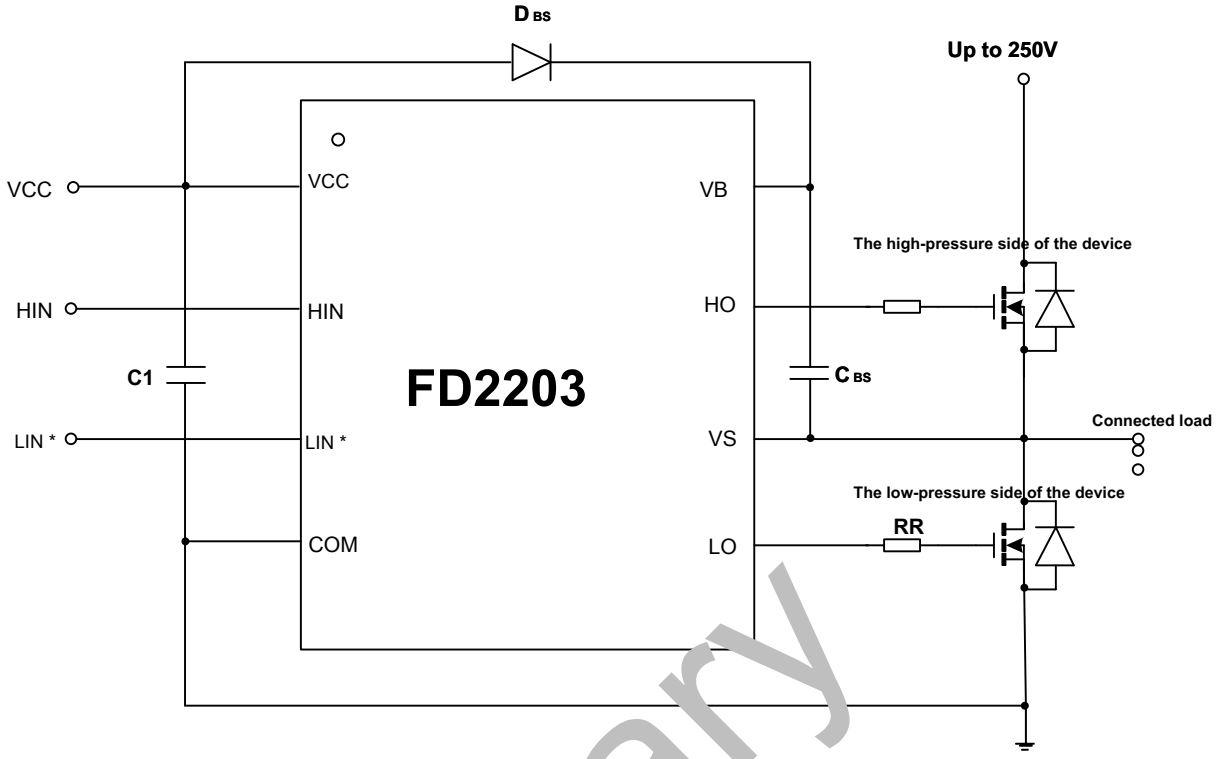
9. The transmission time matching test standard



10. The dead time testing standards



11. A typical application circuit



C1 : Power supply filter capacitor circuit according to the case optionally 0.1μF ~ 10μF .

R : Gate drive resistor, the resistance depends on the driven element.

Dbs : Bootstrap diode should be selected high reverse breakdown voltage (> 2[illegible] V), The diode recovery time as short as possible.

Cbs : Bootstrap capacitor should be chosen ceramic or tantalum, the minimum capacitance value calculated according to the following equation:

$$C_{bs} \geq \frac{[2 \cdot Q_g + Q_{period} + I_{bs(static)} \cdot \text{period} + I_{bs(leak)} \cdot \text{period}]}{V_{cc} - V_F - V_{ds(L)}}$$

among them: Q_g A gate charge of the high-side power device;

Q_{period} Required per cycle charge level converting circuit electrically, about 10nC ;

$I_{bs(static)}$ Quiescent current driving circuit is a high side;

$I_{bs(leak)}$ Bootstrap capacitor leakage current;

[illegible] operating frequency for the circuit;

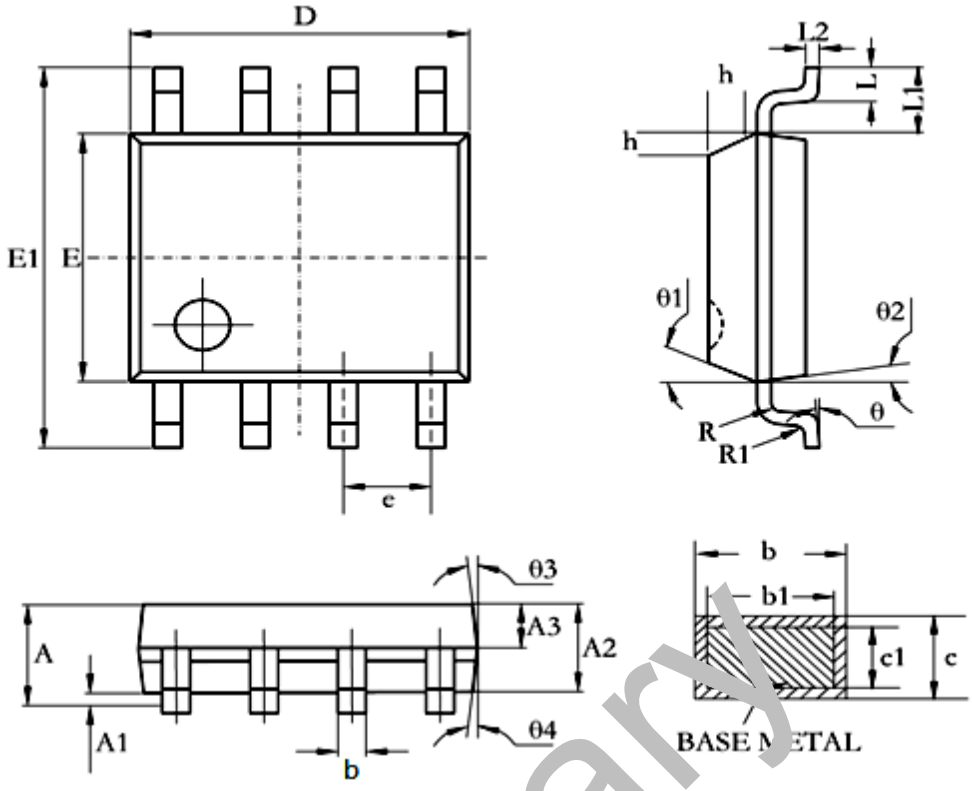
V_{CC} A low side supply voltage;

V_F Bootstrap diode forward voltage drop;

$V_{ds(L)}$ Voltage drop for the low-side power device.

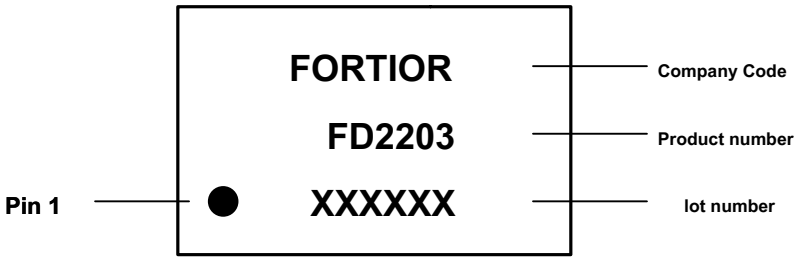
Note: The circuit parameters are for reference and actual application circuit setting parameters according to the measured results.

12. The package size (SOIC-8)



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	1.36	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	1.25	1.40	1.65	0.049	0.055	0.065
A3	0.50	0.65	0.70	0.020	0.024	0.028
b	0.31	-	0.51	0.015	-	0.020
b1	0.37	0.42	0.47	0.015	0.017	0.019
c	0.17	-	0.25	0.007	-	0.010
c1	0.17	0.20	0.23	0.007	0.008	0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	5.80	6.00	6.20	0.228	0.236	0.244
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27BSC					
L	0.45	0.60	0.80	0.018	0.024	0.031
L1	1.04REF					
L2	0.25BSC					
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
h	0.30	0.40	0.50	0.012	0.016	0.020
θ	0 °	-	8 °	0 °	-	8 °
θ1	15 °	17 °	19 °	15 °	17 °	19 °
θ2	11 °	13 °	15 °	11 °	13 °	15 °
θ3	15 °	17 °	19 °	15 °	17 °	19 °
θ4	11 °	13 °	15 °	11 °	13 °	15 °

13. The top screen in the form of FIG.



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