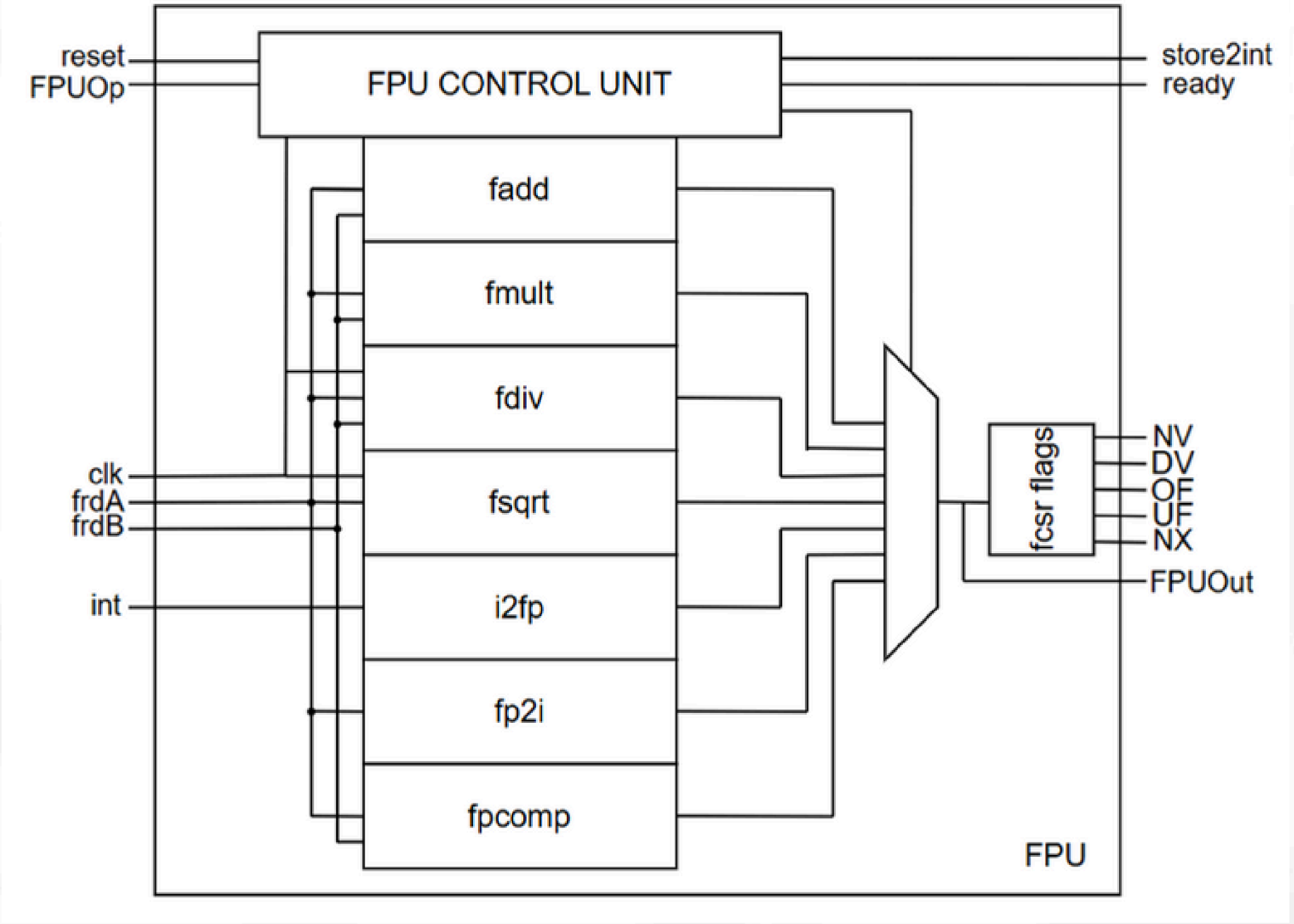
ECE338 - PARALLEL COMPUTER ARCHITECTURE

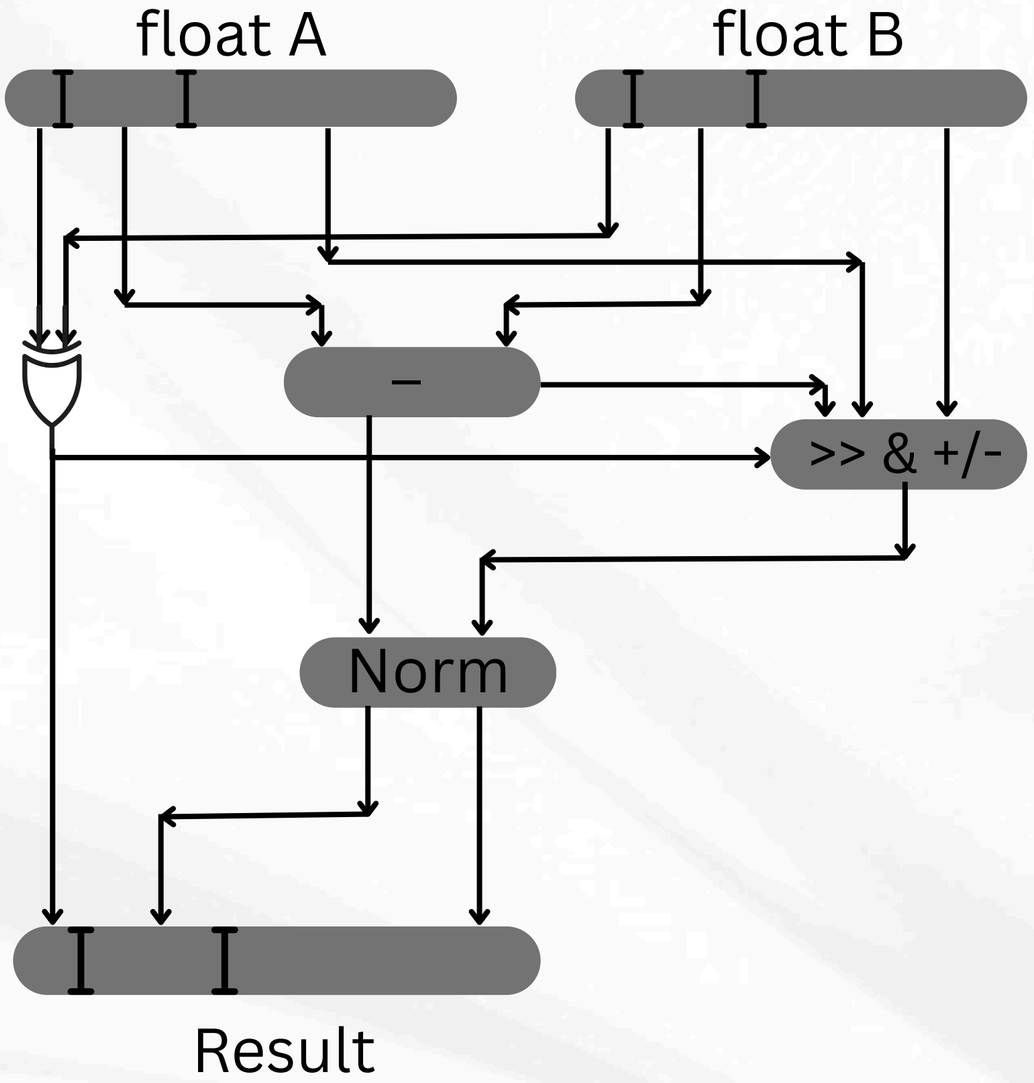
FINAL PRESENTATION

CHRISTOS KARAGIANNIS - IOANNIS KALLERGIS

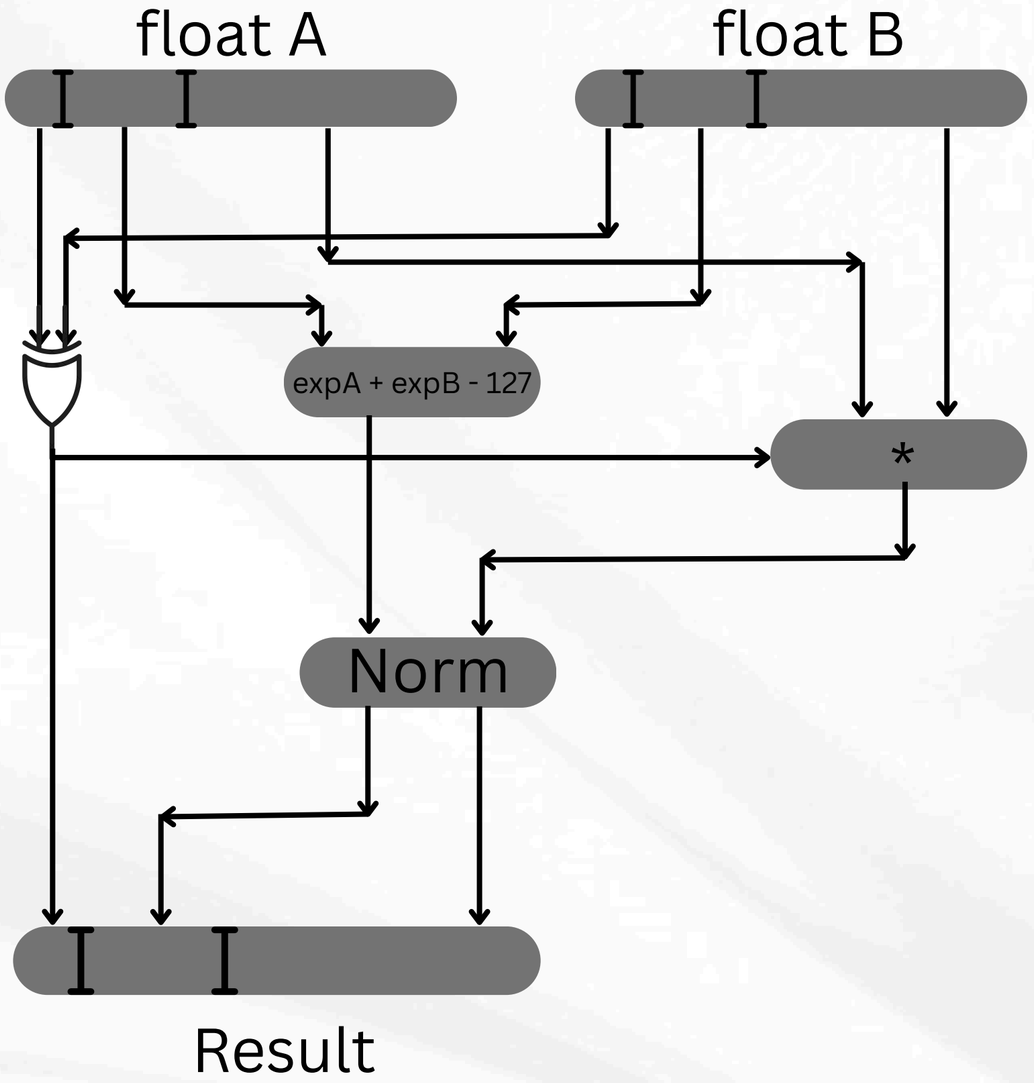
FPU DATAFLOW



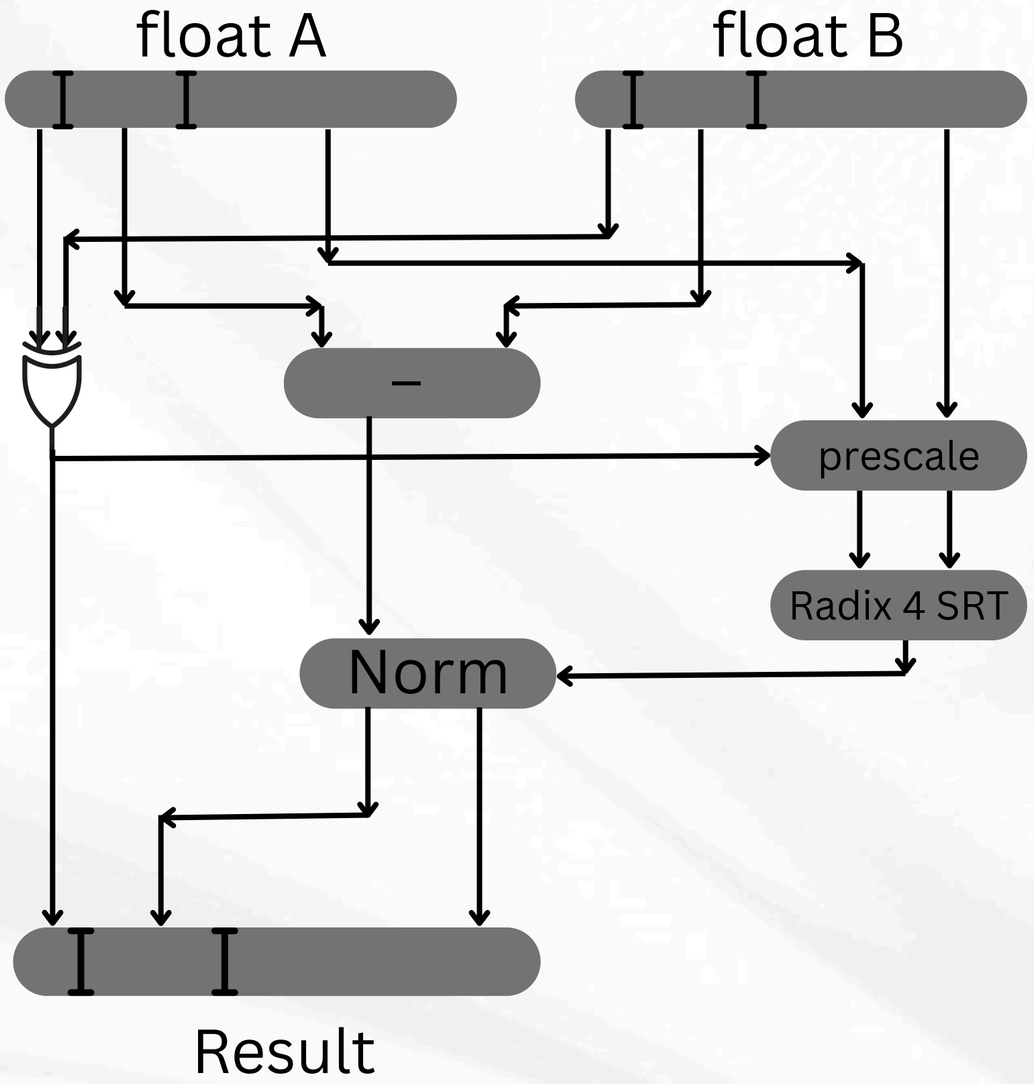
IEEE 754 ADDER



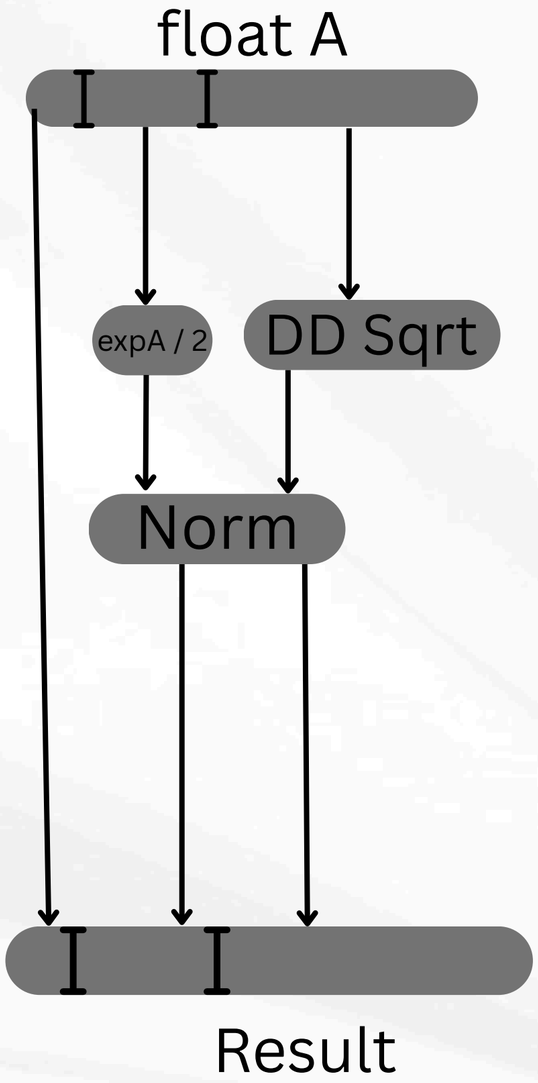
IEEE 754 MULTIPLIER



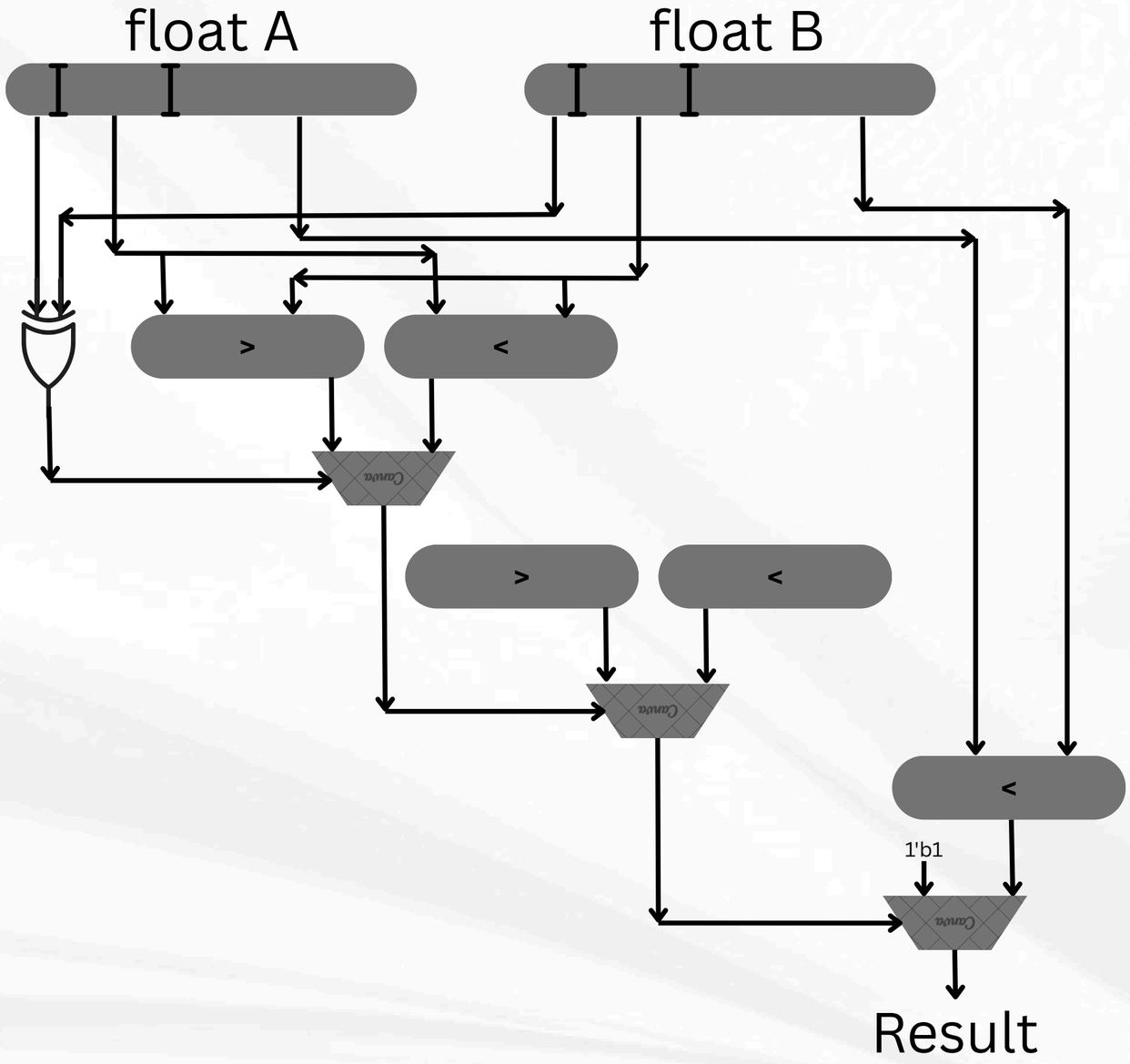
IEEE 754 DIVIDER



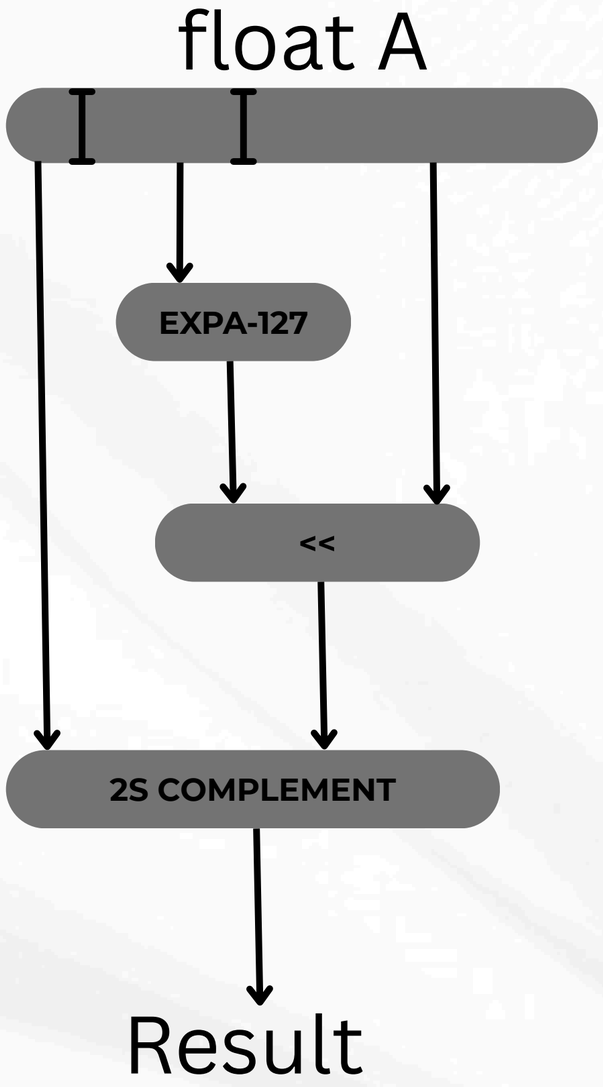
IEEE 754 SQUARE ROOT



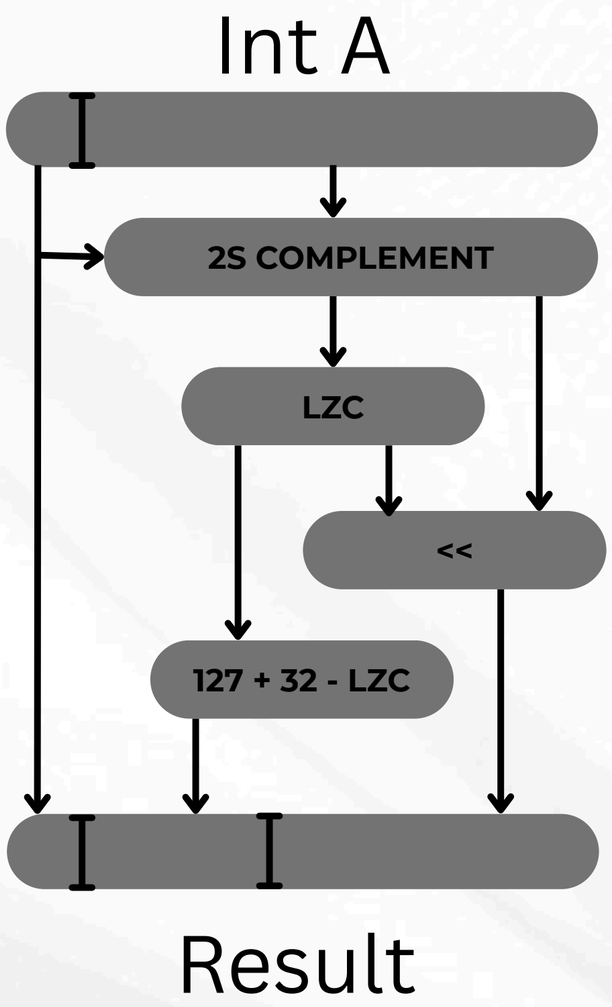
IEEE 754 COMPARATOR



IEEE 754 TO INTEGER



INTEGER TO IEEE 754



THANKS FOR WATCHING