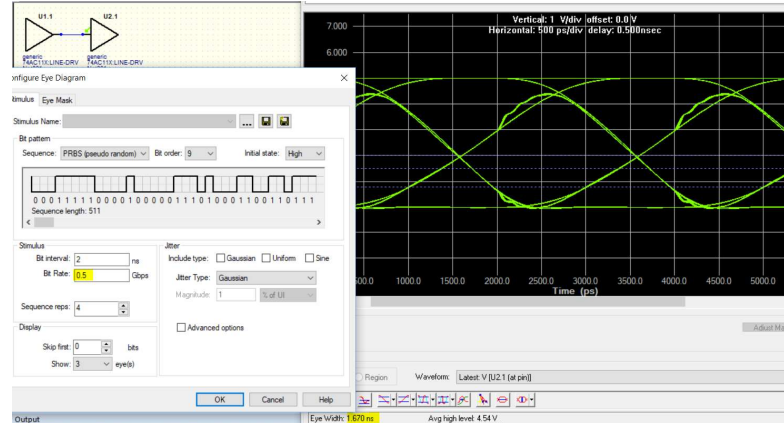**Goal:** The goal of this lab is to get a hands-on experience to evaluate different routing topologies including Branched and Daisy Chain and analyse the same with and without termination components. Also, tabulate the observations and provide proper reasoning for the findings. Tool used is Hyperlynx.
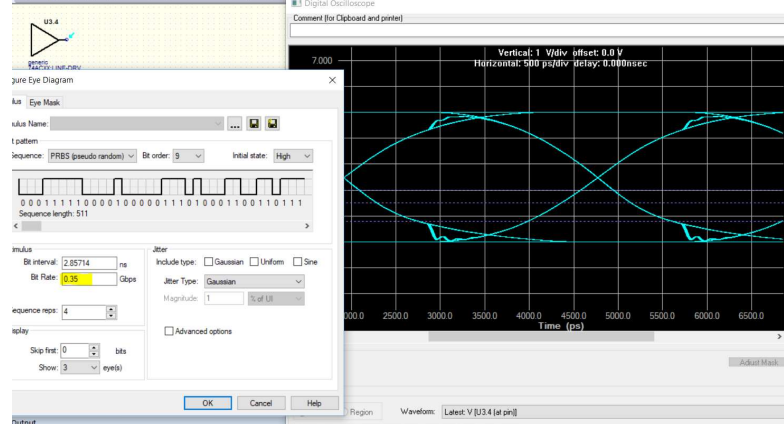
Plan: The plan is to theoretically anticipate the problems in Branched and Daisy Chain routing and also understand the effects of stub resonance. The same needs to be verified in Hyperlynx.

Note: The driver model used is **74AC11-LINE DRV. PRBS** sequence is considered in the eye diagram to get the maximum Data Rate

1. **Select a Driver model. What's the data rate for TX directly connected to RX ?**

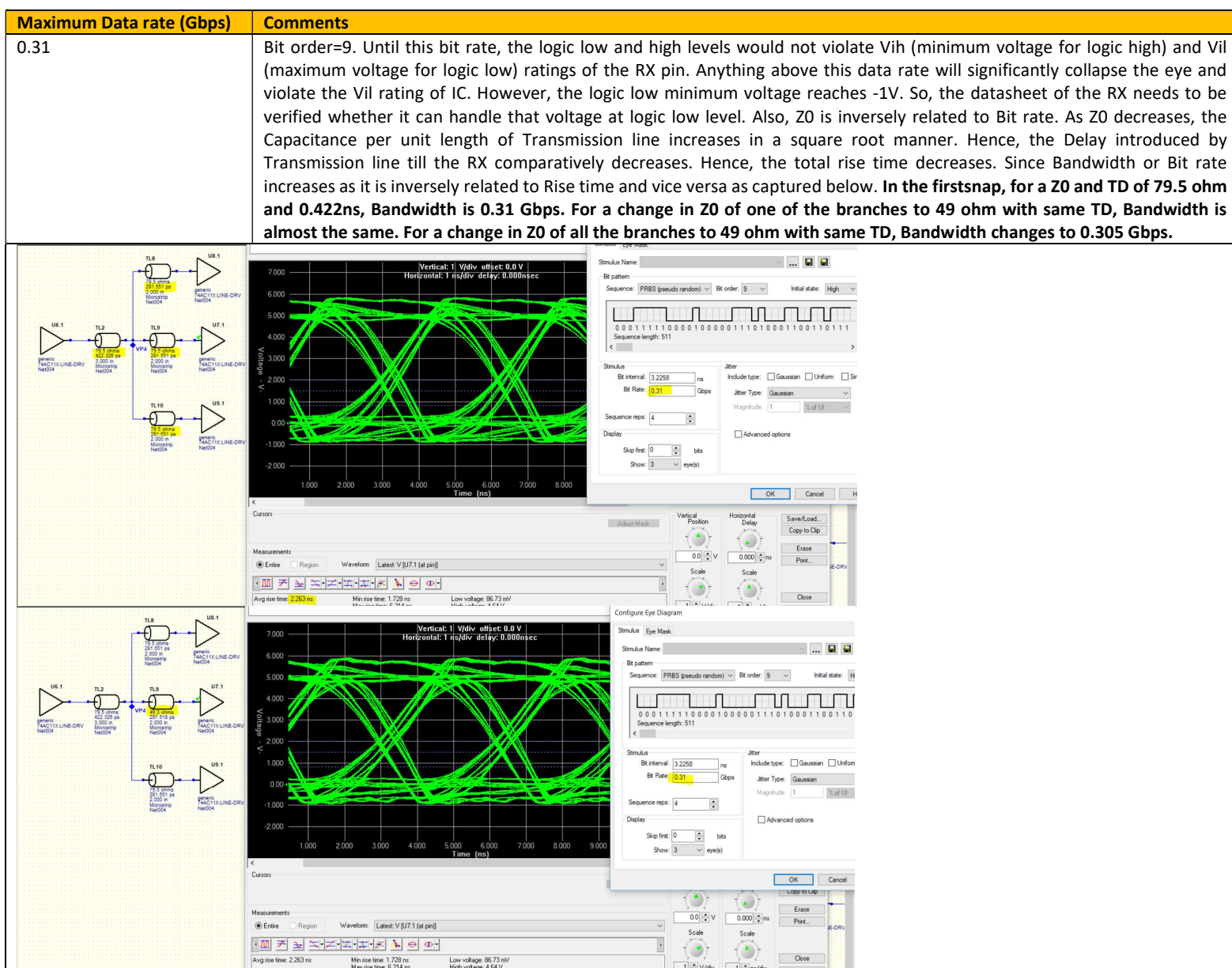| Maximum Data rate (Gbps)	Comments
0.5	Bit order=9. Until this bit rate, the logic low and high levels would not violate Vih (minimum voltage for logic high) and Vil (maximum voltage for logic low) ratings of the RX pin. Anything above this data rate will significantly make the eye to reach more than Vil for 50% of UI and violate the Vil rating of IC. For other driver with a lower rise time, the band width increases (Rise time = 0.35/Bandwidth) and vice versa.

2. **What's the data rate if RX replaced by open?**

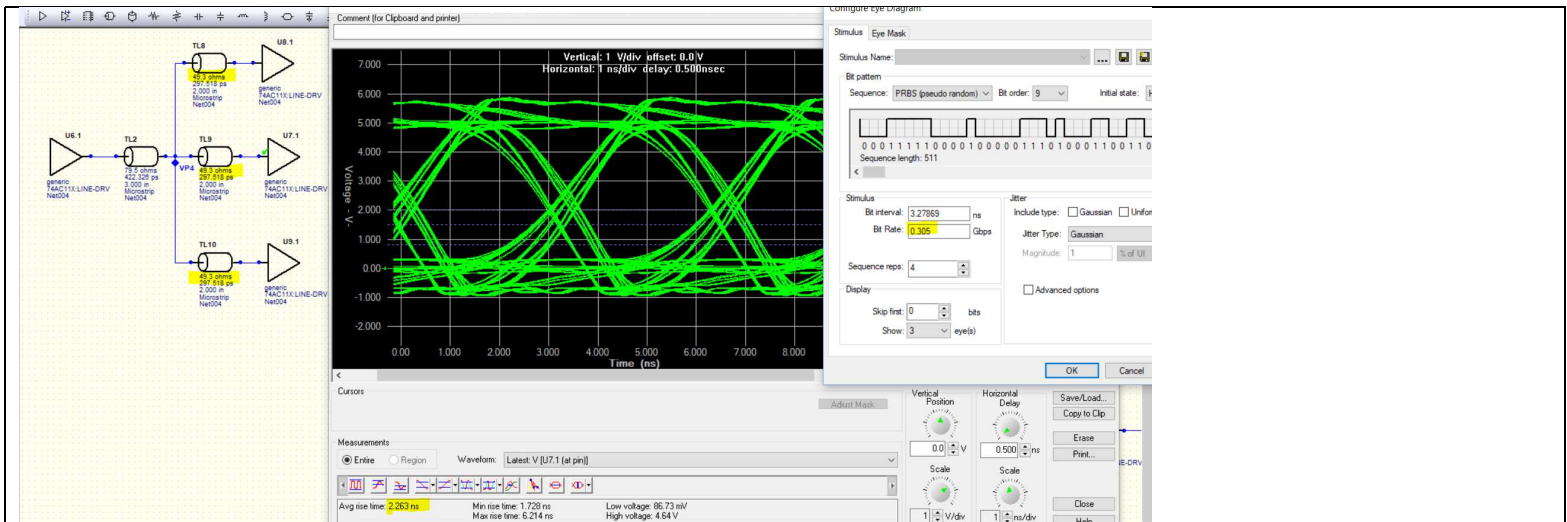| Maximum Data rate (Gbps)	Comments
0.35	Bit order=9. Until this bit rate, the logic low and high levels would not violate Vih (minimum voltage for logic high) and Vil (maximum voltage for logic low) ratings of the RX pin. Anything above this data rate will significantly make the eye to reach more than Vil for 50% of UI and violate the Vil rating of IC. For other driver with a lower rise time, the band width increases (Rise time = 0.35/Bandwidth) and vice versa.

3. **What's the data rate if interconnect is 3 inch long and not terminated ?**

| Maximum Data rate (Gbps)	Comments
0.48	Bit order=9. Until this bit rate, the logic low and high levels would not violate Vih (minimum voltage for logic high) and Vil (maximum voltage for logic low) ratings of the RX pin. Anything above this data rate will significantly collapse the eye and violate the Vil rating of IC. However, the logic low minimum voltage reaches -1V. So, the datasheet of the RX needs to be verified whether it can handle that voltage at logic low level. Also, Z0 is inversely related to Bit rate. As Z0 decreases, the Capacitance per unit length of Transmission line increases in a square root manner. Hence, the Delay introduced by Transmission line till the RX comparatively decreases. Hence, the total rise time decreases. Since Bandwidth or Bit rate increases as it is inversely related to Rise time and vice versa as captured below. **In the left snap, for a Z0 and TD of 79.5 ohm and 0.422ps, Bandwidth is 0.48 Gbps. For a Z0 of 54.2 ohm with same TD, Bandwidth is 0.55 Gbps.**
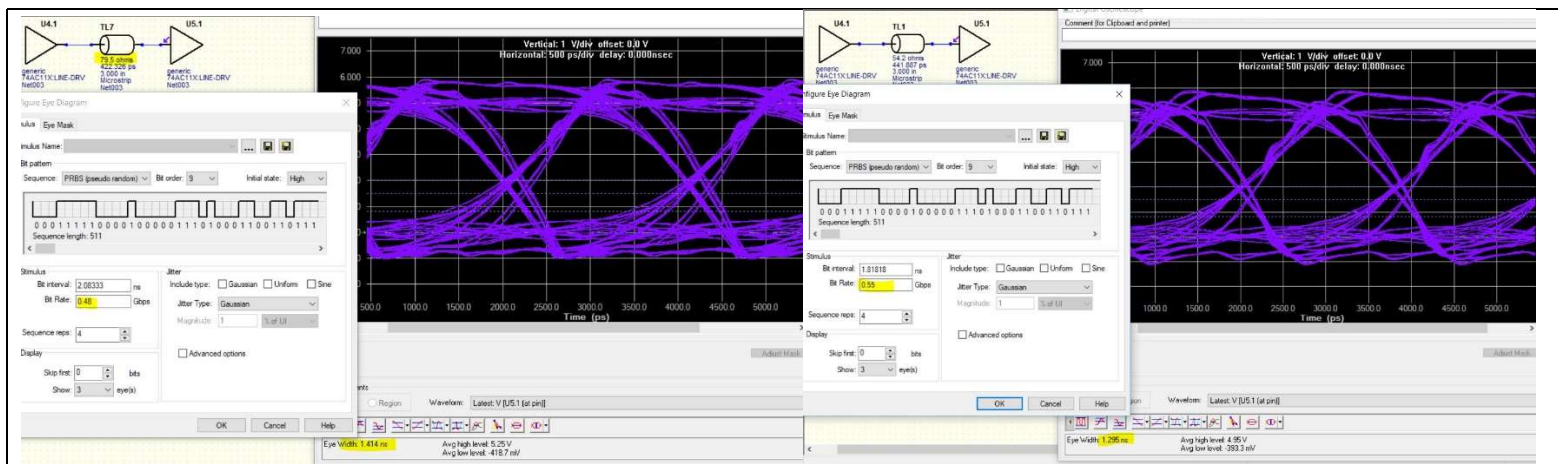
4. **Suppose there is a 3 inch trunk and 3, 2inch branches. What is the max data rate?**

Maximum Data rate (Gbps)	Comments
0.31	Bit order=9. Until this bit rate, the logic low and high levels would not violate Vih (minimum voltage for logic high) and Vil (maximum voltage for logic low) ratings of the RX pin. Anything above this data rate will significantly collapse the eye and violate the Vil rating of IC. However, the logic low minimum voltage reaches -1V. So, the datasheet of the RX needs to be verified whether it can handle that voltage at logic low level. Also, Z0 is inversely related to Bit rate. As Z0 decreases, the Capacitance per unit length of Transmission line increases in a square root manner. Hence, the Delay introduced by Transmission line till the RX comparatively decreases. Hence, the total rise time decreases. Since Bandwidth or Bit rate increases as it is inversely related to Rise time and vice versa as captured below. **In the firstsnap, for a Z0 and TD of 79.5 ohm and 0.422ns, Bandwidth is 0.31 Gbps. For a change in Z0 of one of the branches to 49 ohm with same TD, Bandwidth is almost the same. For a change in Z0 of all the branches to 49 ohm with same TD, Bandwidth changes to 0.305 Gbps.**

5. **What is the max data rate for a 3 drop linear route with 1/4inch stub and flyby termination?**

Maximum Data rate (Gbps)	Comments
0.42	Bit order=9. Zo throughout is 50 ohm. Until this bit rate, the logic low and high levels would not violate Vih (minimum voltage for logic high) and Vil (maximum voltage for logic low) ratings of the RX pin. Anything above this data rate will significantly collapse the eye and violate the Vil rating of IC. However, the logic low minimum voltage reaches -1V. So, the datasheet of the RX needs to be verified whether it can handle that voltage at logic low level. Also, Z0 is inversely related to Bit rate. As Z0 decreases, the Capacitance per unit length of Transmission line increases in a square root manner. Hence, the Delay introduced by Transmission line till the RX comparatively decreases. Hence, the total rise time decreases. Since Bandwidth or Bit rate increases as it is inversely related to Rise time and vice versa as captured below. **In the first snap, for a Z0 and TD of 50 ohm and 0.44ns, Bandwidth is 0.42 Gbps. For a change in Z0 of all the branches to 25 ohm with same TD, Bandwidth changes to 0.305 Gbps.**
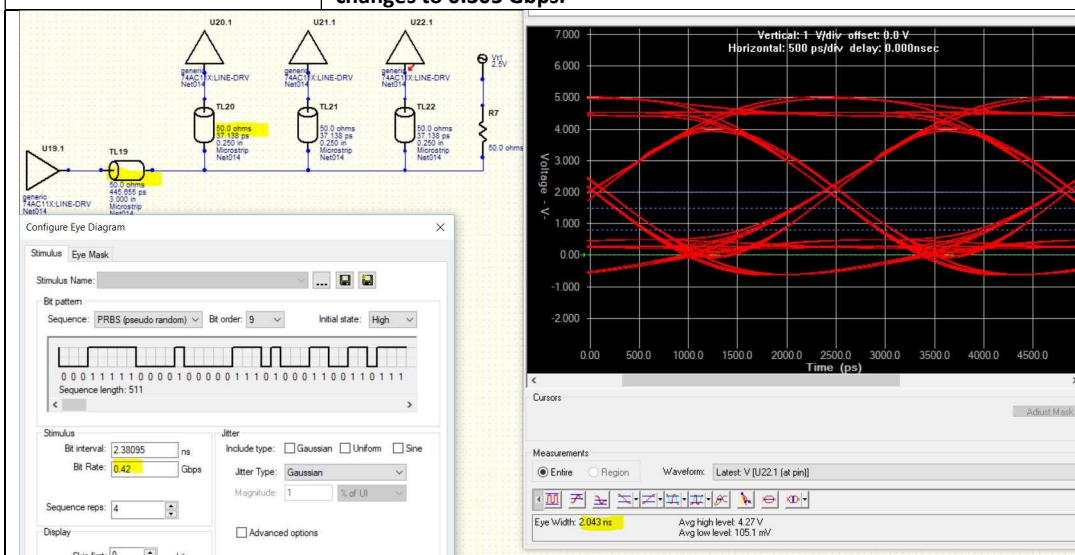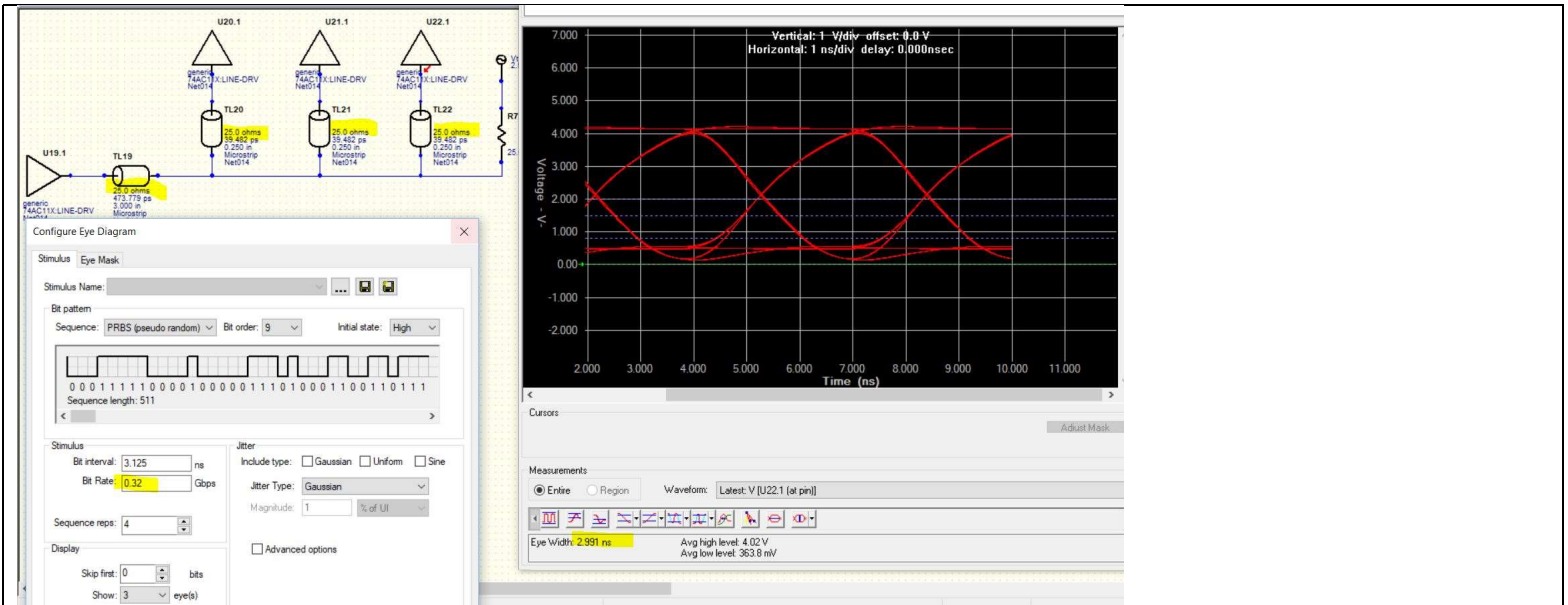
Conclusions / Lessons Learnt:

1. The maximum data rate depends on the type of termination and also on the routing topology
2. Flyby termination has higher data rate than Source termination as the current to RX is more in Flyby due to which capacitor at RX charges quickly.So, rise time decreases and Date rate increases.
3. For data rates lesser than 2Gbps, a branched topology can be used by thorough analysis
4. For data rates more than 2Gbps, linear routing is the only major topology
5. As Zo of the Transmission line decreases, Capacitance per unit length varies inversely to the square root of Z0, so the overall rise time increases at RX pin due to which, the Max data rate decreases and vice versa.