**Goal:** The goal of this lab is to get a hands-on experience to characterize Drivers based on Rise and fall times, Source Impedance, Open circuit voltage and apply all the major termination strategies and tabulate their respective advantages and disadvantages. Also, tabulate the power dissipation. Tool used is Hyperlynx.

**Plan:** The plan is to theoretically anticipate the source impedance and to theoretically apply the termination strategies to Transmission and predict the best approach considering the power, extra components and so on. The same needs to be verified in Hyperlynx.

**Characterize two driver models: 74AC11, TDR, IDT 74FCT**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Driver** | **Rise Time (ns) (10%-90%)** | **Fall Time(ns) (10%-90%)** | **Source Impedance (ohm)** | **Open Circuit Voltage (V)** | **Comments** |
| 74ACT11 | 1.75 | 1.347 | 17 | 5 | The fall time < rise time as expected since Rise Time is governed by PMOSFET whose switching time is comparatively higher than NMOSFET which governs the fall time. As per simulation, for a termination of 50 ohm at the driver, the voltage across resistor is 3.96V. So, applying Voltage Divider equation, 3.96 = 5 \*50/(Rs+50). Rs turns out to be 17 ohm. When the 50 ohm termination is replaced with 17 ohm, the voltage across resistor is 2.5V. |
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| 74ALSXX | 3.017 | 2.074 | 25 | 3.58 | The fall time < rise time as expected since Rise Time is governed by PMOSFET whose switching time is comparatively higher than NMOSFET which governs the fall time. As per simulation, for a termination of 50 ohm at the driver, the voltage across resistor is 2.48V. So, applying Voltage Divider equation, 2.48 = 3.58 \*50/(Rs+50). Rs turns out to be 25 ohm. When the 50 ohm termination is replaced with 25 ohm, the voltage across resistor is 1.79V. |
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**Pick one of the drivers: Build a transmission line circuit. How long can it be without termination?**

|  |  |  |
| --- | --- | --- |
| **Driver** | **Maximum Transmission Line length without termination (in)** | **Comments** |
| 74ACT11 | 3.2 | The Receiver is a TDR model. For Transmission Line length in inch lesser than rise time in ns, there should absolutely no distortion in the received signal as per the thumb rule. For length greater than 3 inch, the Monotonicity at the logic low level will be affected with further increase of trace length due to excess ringing. However, the logic low level goes till -0.8V and is neglected. The rise time being 1.74 ns, the quality of the signal when it travels a length of 1.74 inch cannot be guaranteed as it heavily depends on the Receiver input characteristics like Gate capacitance. |
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|  | | |
| **Engineer the five different termination schemes and optimize each one. Do some have advantages?** | | |

**Note:** The transmission line considered is a simple, 50-ohm, 5 ns delay type. The Receiver is a TDR model.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Termination Type** | **Resistor added (ohm)** | **Vlow**  **(V)** | **Vhi**  **(V)** | **Acceptable**  **?** | **Comments** | |
| **Source Series** | 33 | -0.639 | 5 | Yes | The Driver source resistance being 17 ohm, if a series resistor of 33 ohm is added near to driver in series to equate to transmission line impedance of 50 ohm, the signal sees a uniform impedance of 50 ohm throughout. Although the Logic high level is more than 5V and logic low level is less than 0, they are acceptable. Without the series resistor, there are very high ringing due to impedance mismatch. The same is observed in the below simulation. | |
| C:\Users\nagar\AppData\Local\Microsoft\Windows\INetCache\Content.Word\Q3_1.jpgC:\Users\nagar\AppData\Local\Microsoft\Windows\INetCache\Content.Word\Q3_2.jpg | | | | | | |
| **Far End Shunt to Vss** | 33 | -0.639 | 4 | Yes | The Driver source resistance being 17 ohm, if a shunt resistor of 68.4 ohm is added near to RX to equate to transmission line impedance of 50 ohm, the signal sees a uniform impedance of 8.4 ohm throughout. Although the Logic logic low level is less than 0, its are acceptable. Without the shunt resistor, there are very high ringing due to impedance mismatch. The same is observed in the below simulation. | |
| C:\Users\nagar\AppData\Local\Microsoft\Windows\INetCache\Content.Word\Q3_2_1.jpg | | | | | |  |
| **Far End RC** | 68.4 ; C= 100 nF | -0.639 | 4 | Yes |  | |
| C:\Users\nagar\AppData\Local\Microsoft\Windows\INetCache\Content.Word\Q3_3.jpg | | | | | |  |
| **Far End Thevenin** | R1=100; R2=100 | 0.2 | 4.5 | Yes | The far end Thevenin network should be such be such that the Vcc should be equal to the signal voltage from the driver and the equivalent parallel value of the resistors be equal to Z0 of transmission line. This ensures proper termination as there would be uniform impedance throughout the path. The same is observed in the below simulation. | |
| C:\Users\nagar\AppData\Local\Microsoft\Windows\INetCache\Content.Word\Q3_4.jpg | | | | | |  |
| **Far End Shunt to Vtt** | 50 | 0.4 | 4.5 | Yes | The Driver source resistance being 17 ohm, if a shunt resistor of 68.4 ohm is added near to RX to equate to transmission line impedance of 50 ohm, the signal sees a uniform impedance of 8.4 ohm throughout. Although the Logic logic low level is less than 0, its are acceptable. Without the shunt resistor, there are very high ringing due to impedance mismatch. The same is observed in the below simulation. | |
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**Calculate the average power dissipation in each approach, assuming driver output resistance is 0.**

|  |  |  |  |
| --- | --- | --- | --- |
| **Termination Type** | **Power Dissipation Formula** | **Power Dissipation (W)** | **Comment** |
| **Source Series** | 0.5\*(0)/50 | 0 | The Voltage across the Resistor is negligible as the other end is a very high impedance (RX) |
| **Far End Shunt Vss** | 0.5\*(52)/50 | 0.25 |  |
| **Far End RC** | 0.5\*(0.5\*5)2/50+0.5\*(0.5\*5)2/50 | 0.125 |  |
| **Far End Thevenin** | 0.5\*(52)/100+0.5\*(52)/100 | 0.25 |  |
| **Far End Shunt to Vtt** | 0.5\*(0.5\*5)2/50+0.5\*(0.5\*5)2/50 | 0.125 |  |