Lab 2: Schematic Design and Spectre Simulation

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CMPE 640
Custom VLSI Design
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Schematic Creation and Simulation Procedure

The Virtuoso software is a powerful suite of tools that allows for constructing circuits and simulating them using Spectre. Each gate and simulation requires it to be its own cell. Once a cell is created, Schematic XL can be used to construct the circuit. For simulating circuits, the ADE L tool is used. The ADE L tool must first be configured with the correct setting, and most importantly be set up to use Spectre as the simulator. Once ADE L is set up, a netlist can be created and a simulation run. When the simulation is complete, a waveform of the inputs and outputs will appear, which allows for analysis.

In these experiments, the transient measuring tool was used to obtain the rise and fall times for each experiment. Additionally, the horizontal flag tool was used to mark the time when the voltage was at 50%. Subtracting the difference between the output and input at 50% allowed for the simple calculation of the fall and rise delays.

Minimum Inverter (INVx1) Simulation Results

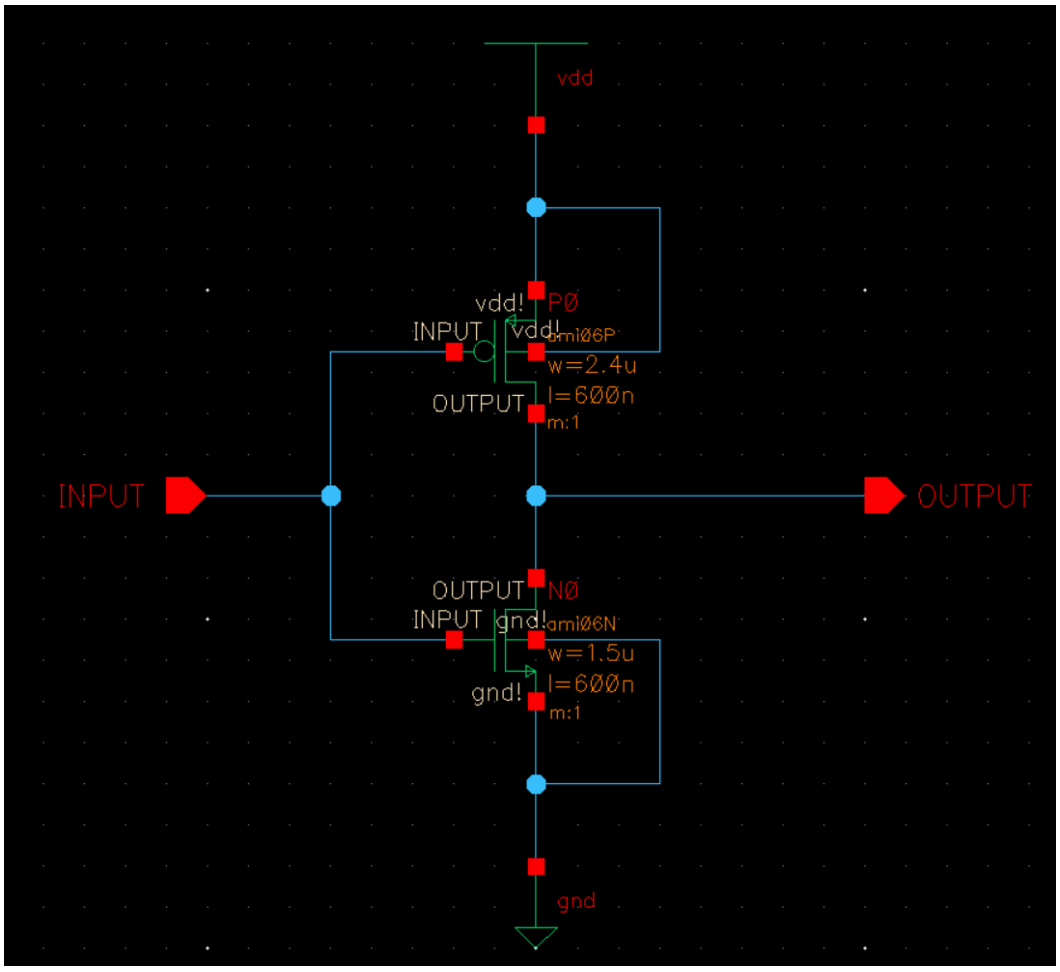

Figure 1: Schematic of the minimum sized inverter with length of 600 nM and width of 1.5 uM. INVx2 and INVx4 use this same design but with larger widths.

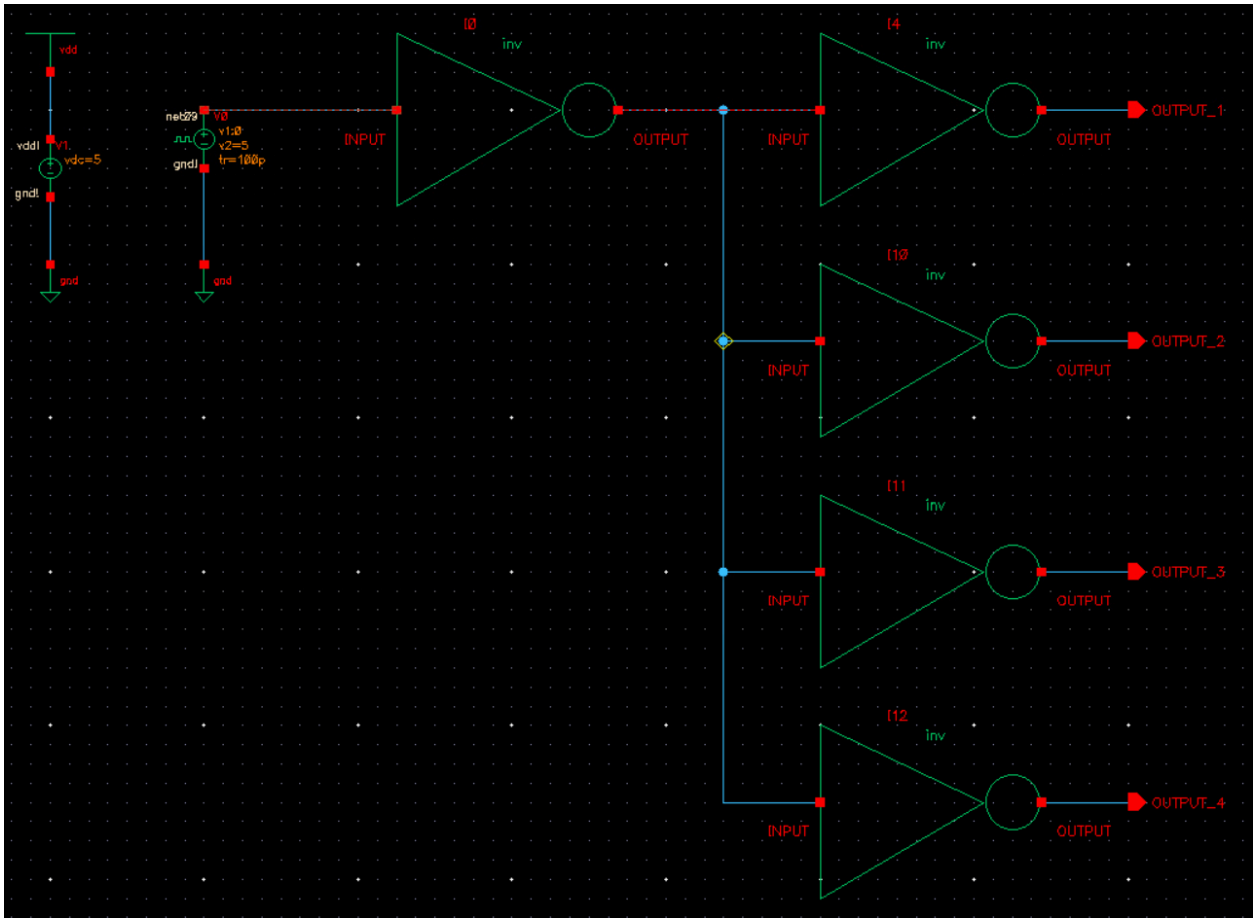

Figure 2: Schematic of “testbench” used for simulation for a load of 4 inverters. This style of simulation was used to retrieve the results in Table 1, Table 2 and Table 3.

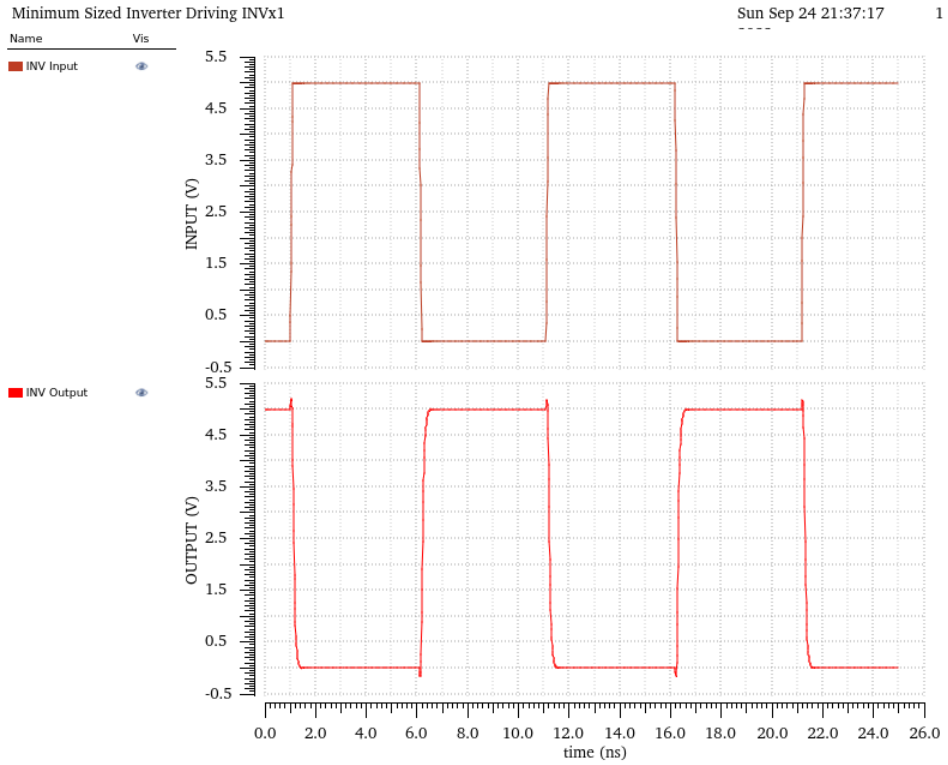

Figure 3: Input and output results of the minimum sized inverter with a load of one inverter.

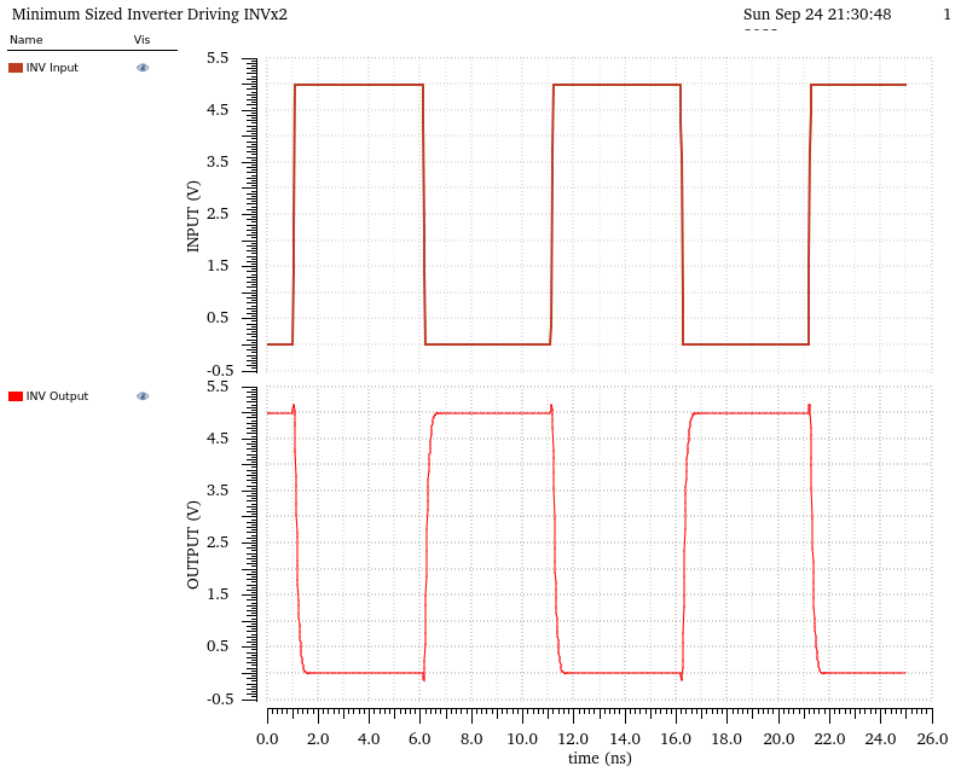

Figure 4: Input and output results of the minimum sized inverter with a load of two inverters.

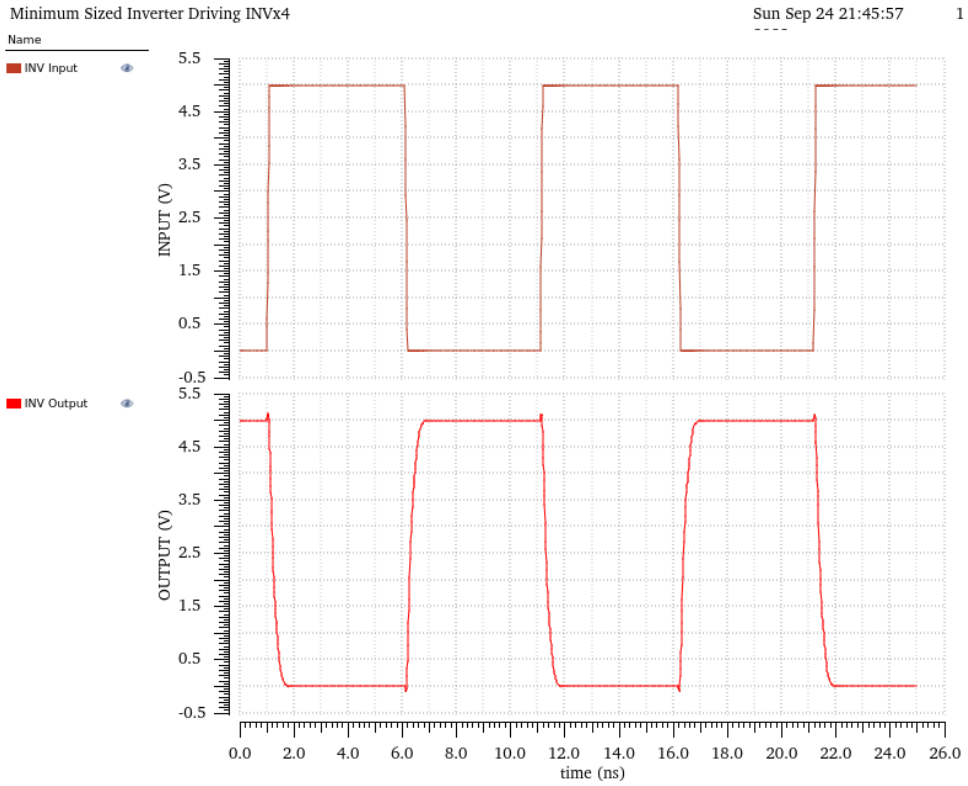

Figure 5: Input and output results of the minimum sized inverter with a load of four inverters.

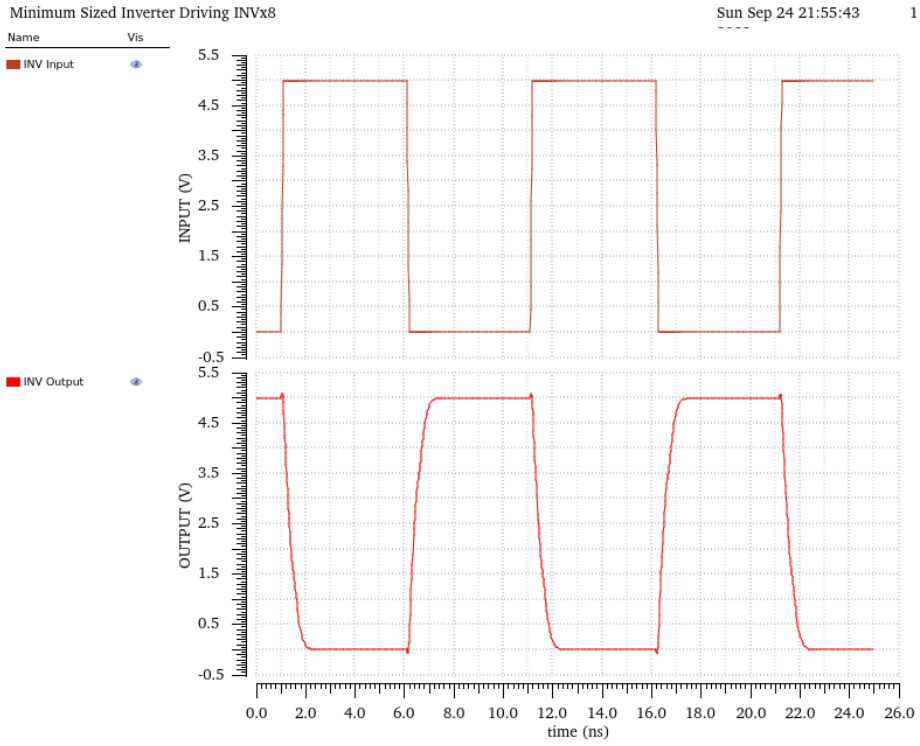

Figure 6: Input and output results of the minimum sized inverter with a load of eight inverters.

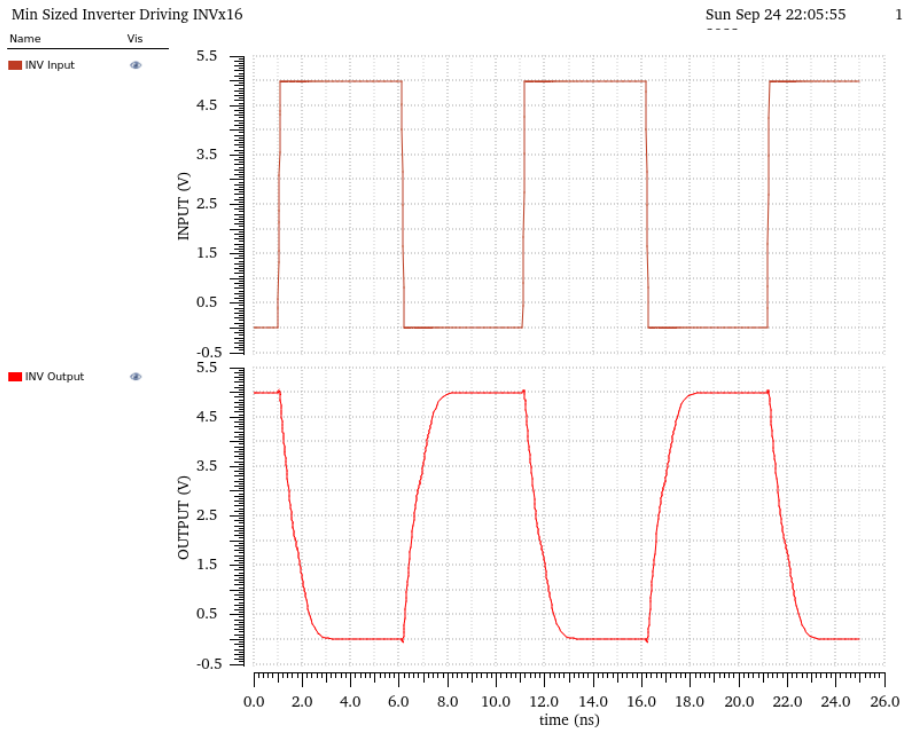

Figure 7: Input and output results of the minimum sized inverter with a load of sixteen inverters.

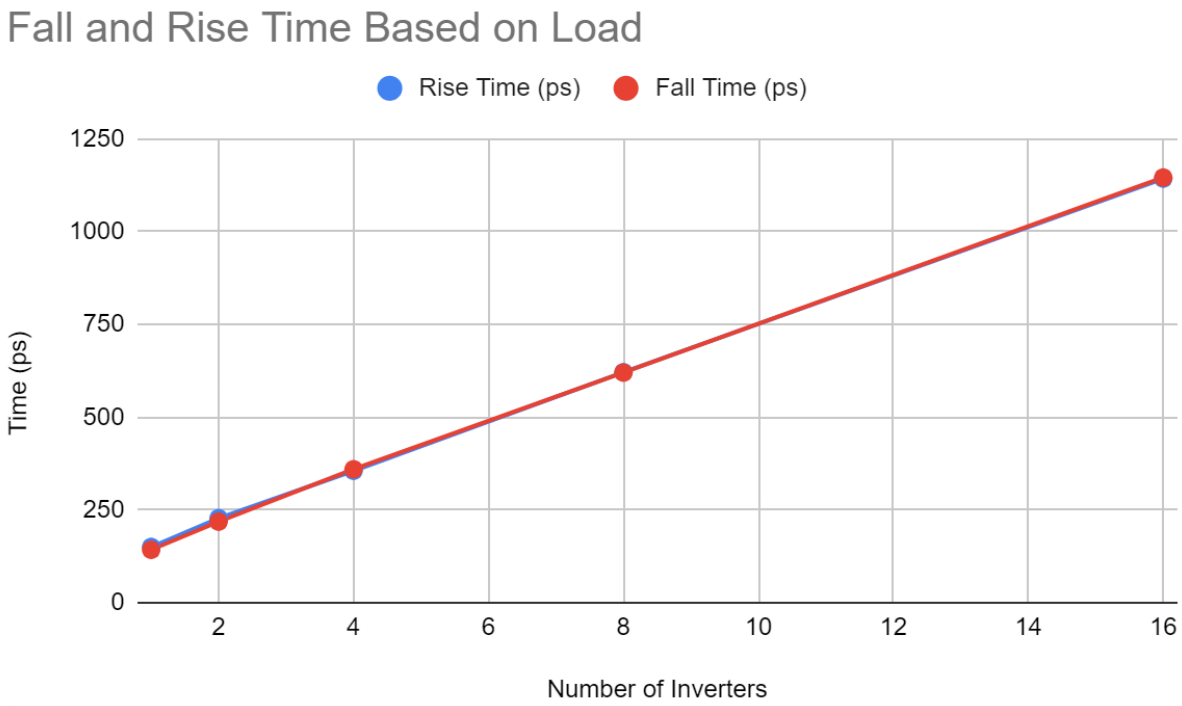

Figure 8: Graph showing a near linear increase in fall and rise time when the load is increased using data from Table 1,, which uses the INVx1.

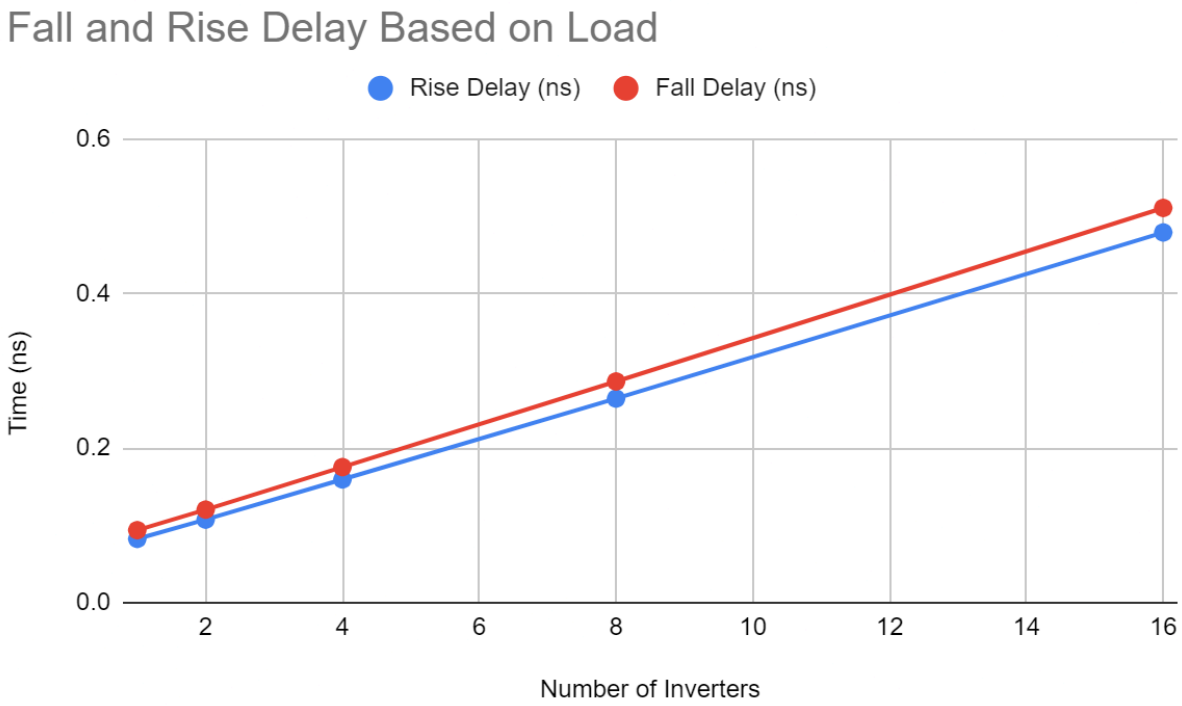

Figure 9: Graph showing a near linear increase in fall and rise delay when the load is increased using data from Table 1, which uses the INVx1.

Table 1: Comparing rise and fall times and delays of the minimum inverter based on load.

Inverters	Rise Time (ps)	Fall Time (ps)	Rise Delay (ns)	Fall Delay (ns)
1	150.3	142.5	0.0826	0.0938
2	227.9	218.4	0.1075	0.1204
4	355.4	359.7	0.1595	0.1754
8	621.3	620.1	0.2641	0.2862
16	1143	1146	0.4790	0.5107

INVx2 Simulation Results

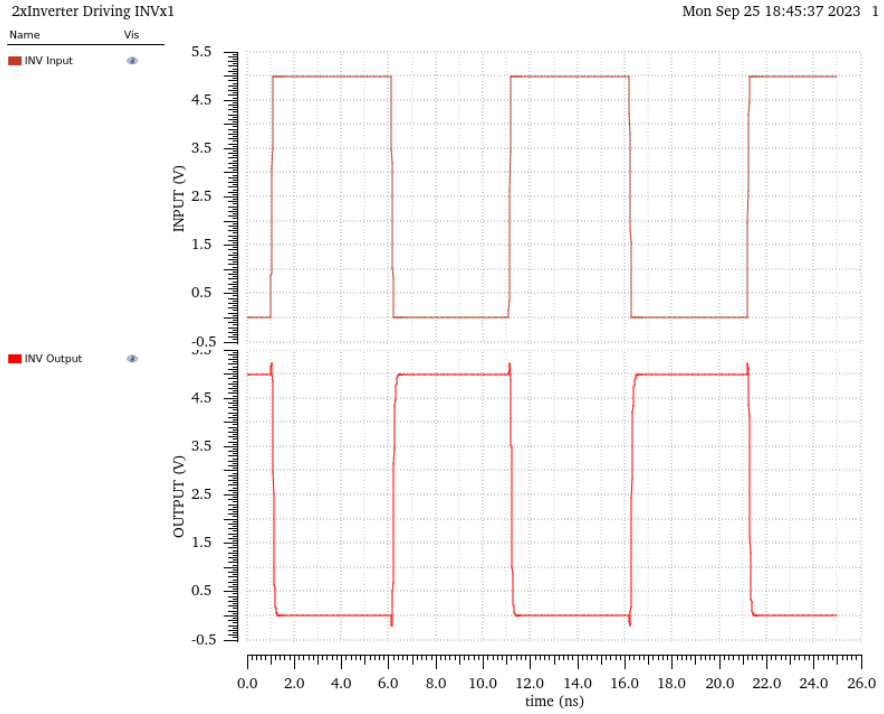

Figure 10: Input and output results of the double sized inverter with a load of one inverter.

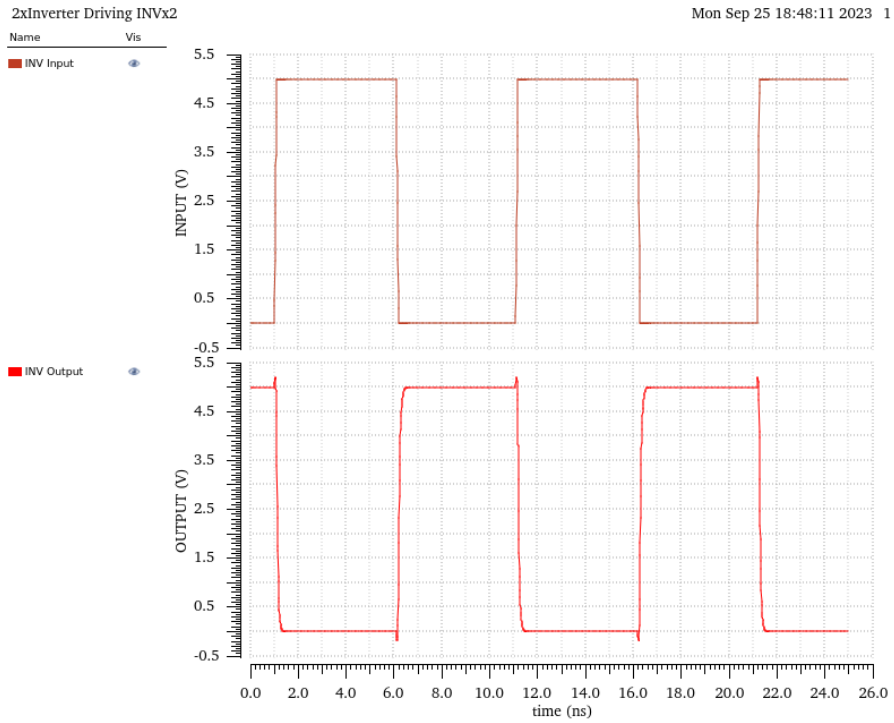

Figure 11: Input and output results of the double sized inverter with a load of two inverters.

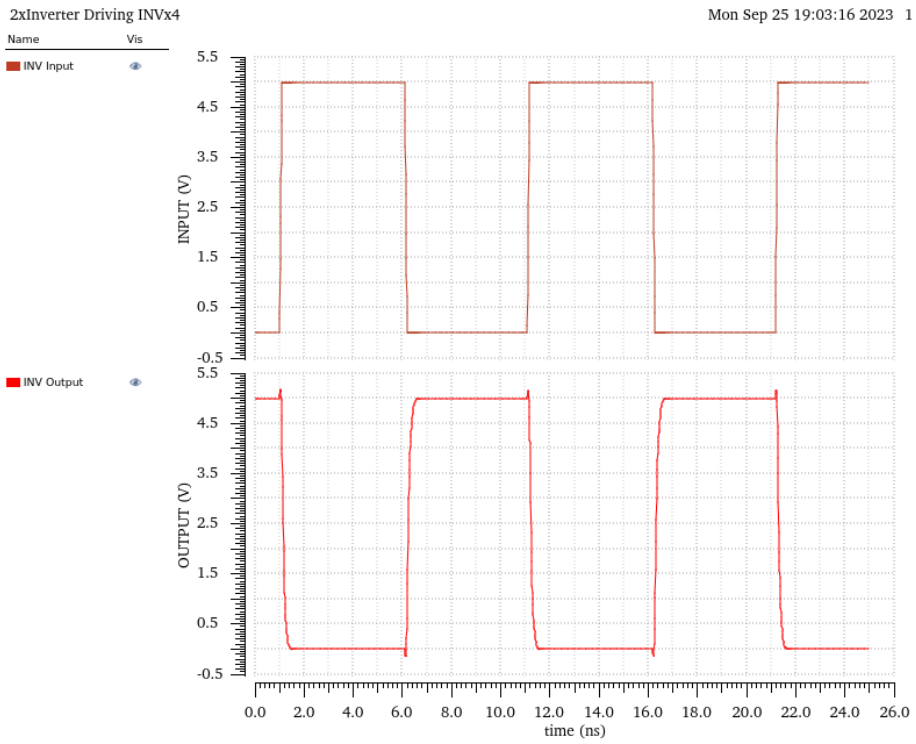

Figure 12: Input and output results of the double sized inverter with a load of four inverters.

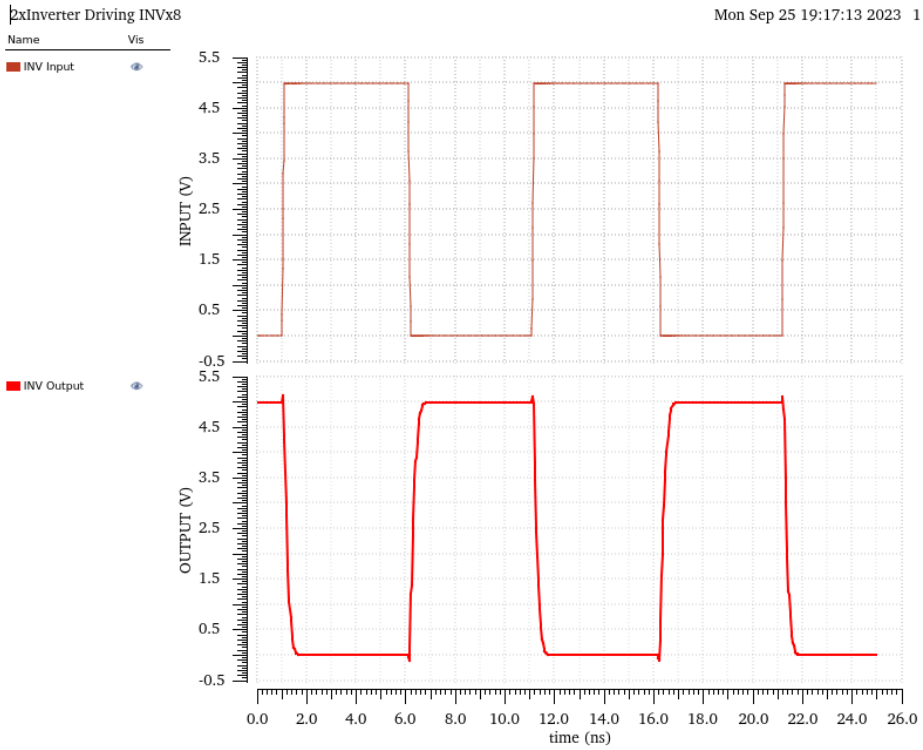

Figure 13: Input and output results of the double sized inverter with a load of eight inverters.

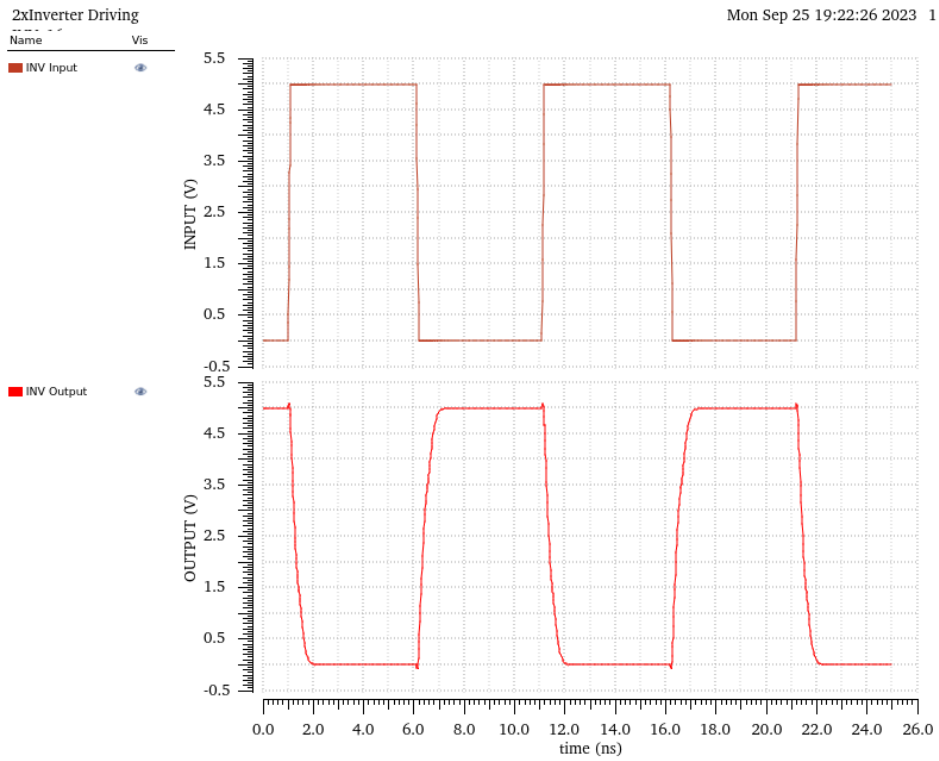

Figure 14: Input and output results of the double sized inverter with a load of sixteen inverters.

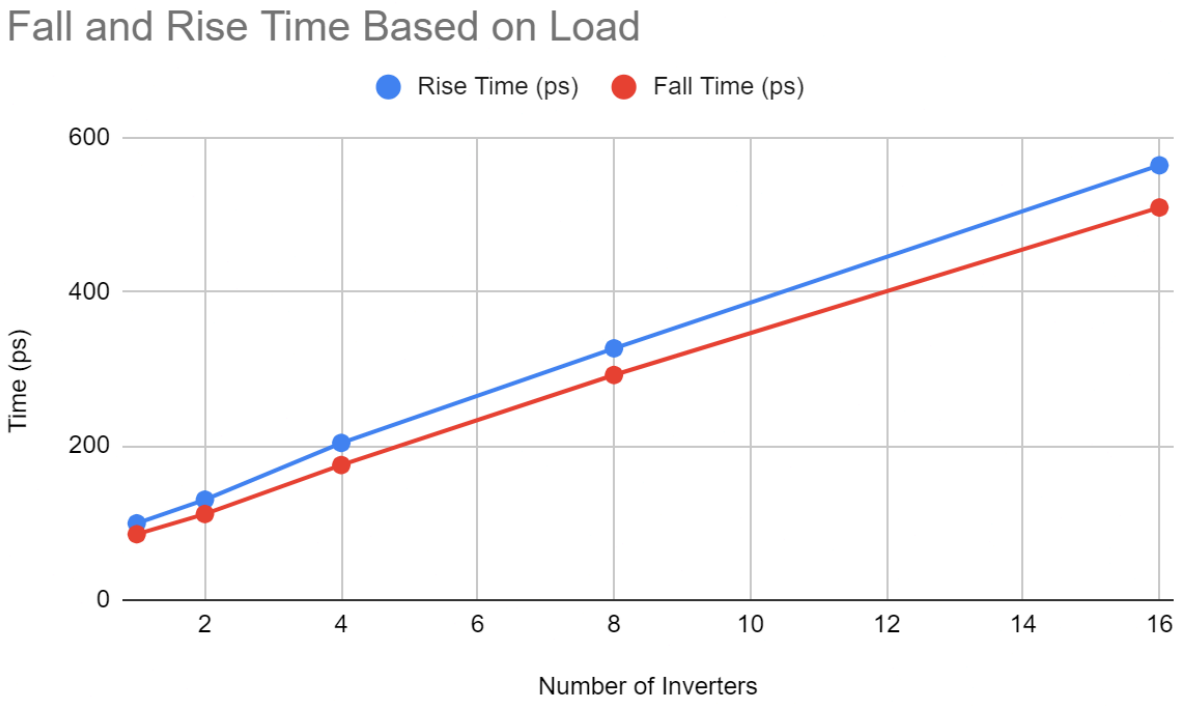

Figure 15: Graph showing a near linear increase in fall and rise time when the load is increased using data from Table 2, which uses the INVx2.

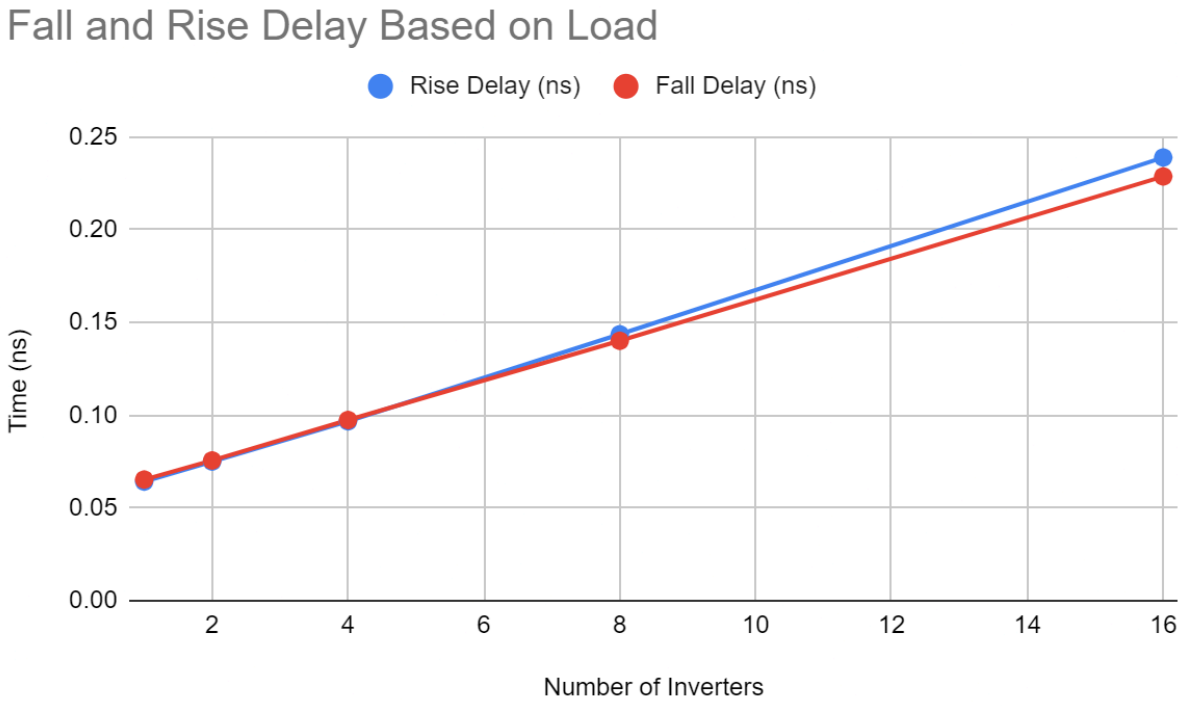

Figure 16: Graph showing a near linear increase in fall and rise delay when the load is increased using data from Table 2, which uses the INVx2.

Table 2: Comparing rise and fall times and delays of the INVx2 based on load.

Inverters	Rise Time (ps)	Fall Time (ps)	Rise Delay (ns)	Fall Delay (ns)
1	99.49	85.42	0.0642	0.0653
2	130.2	111.6	0.0750	0.0756
4	203.8	175.1	0.0967	0.0974
8	326.5	291.9	0.1436	0.1401
16	563.9	509.2	0.2389	0.2287

INVx4 Simulation Results

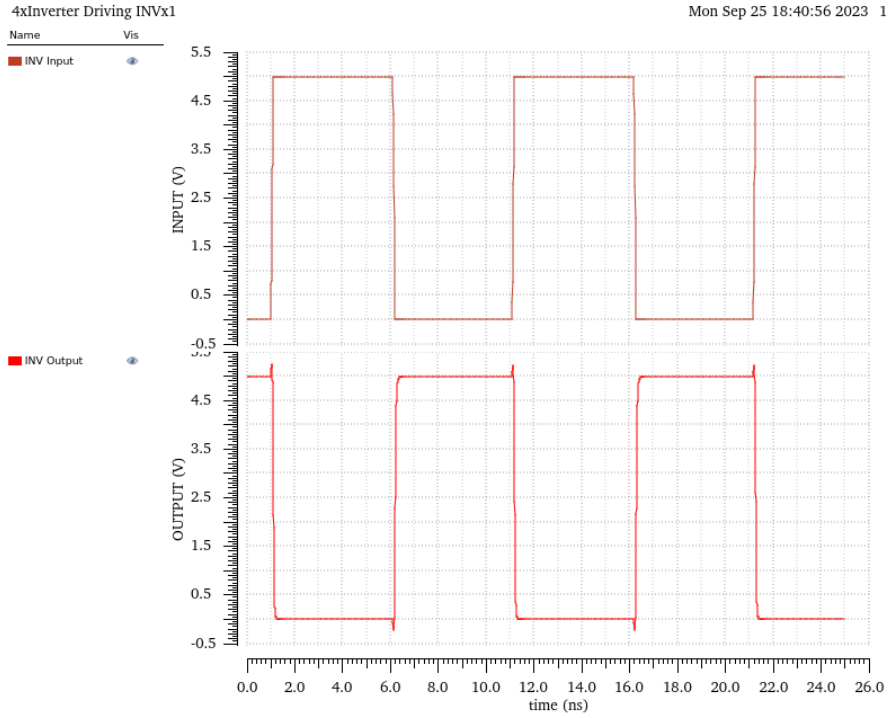

Figure 17: Input and output results of the quadruple sized inverter with a load of one inverter.

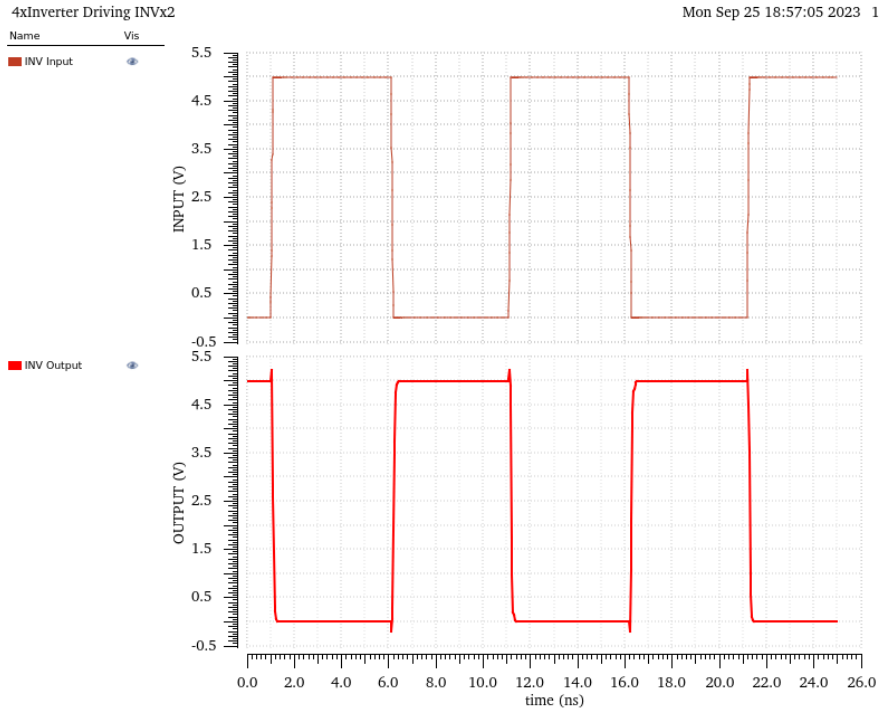

Figure 18: Input and output results of the quadruple sized inverter with a load of two inverters.

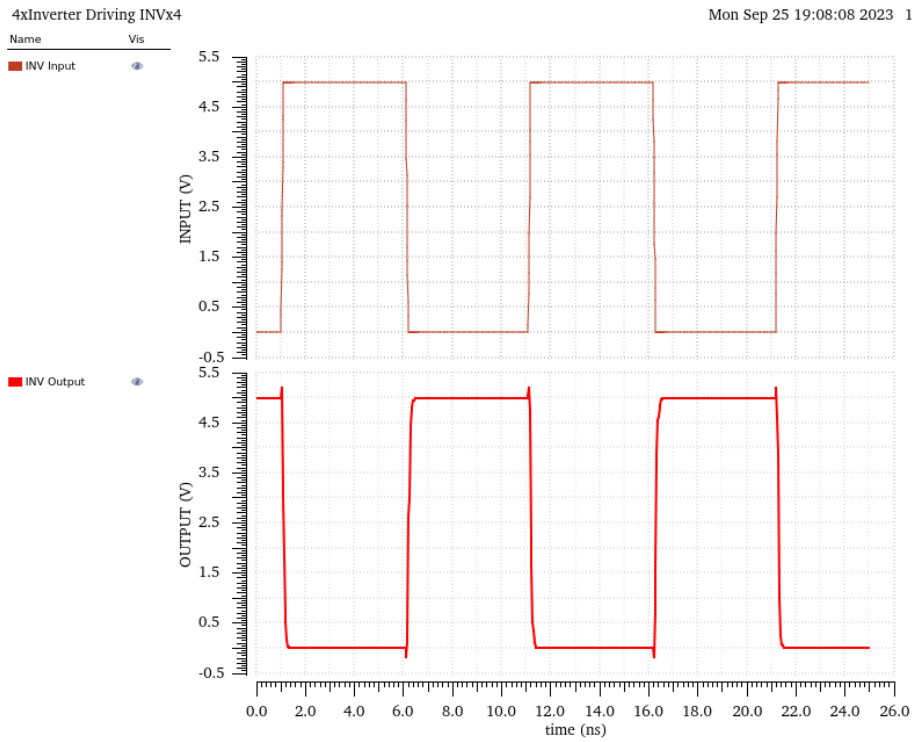

Figure 19: Input and output results of the quadruple sized inverter with a load of four inverters.

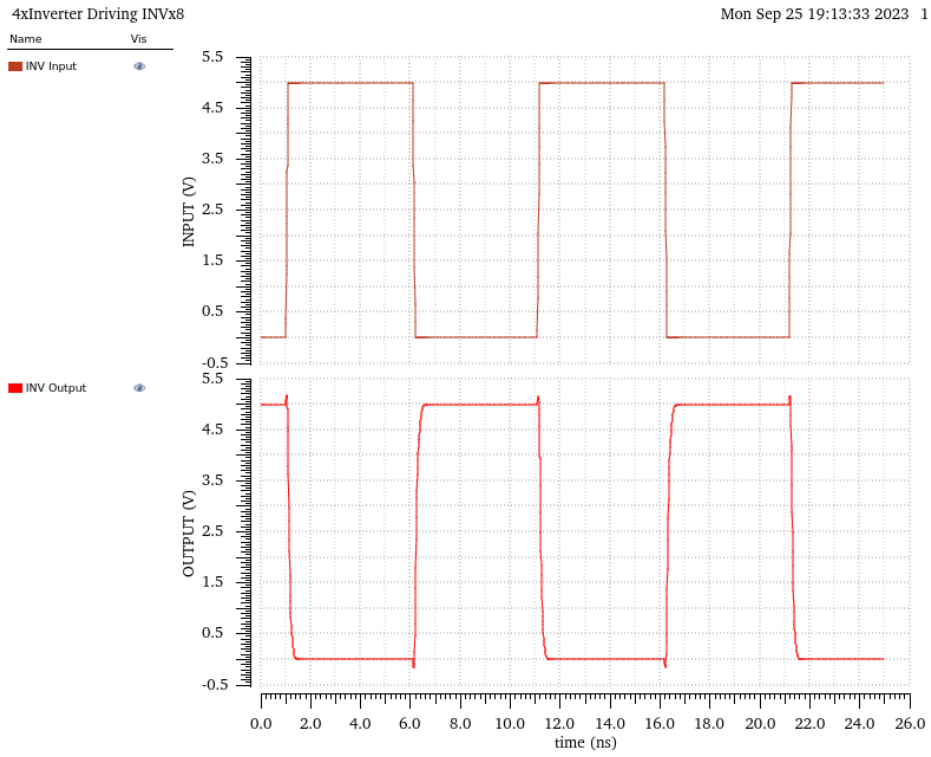

Figure 20: Input and output results of the quadruple sized inverter with a load of eight inverters.

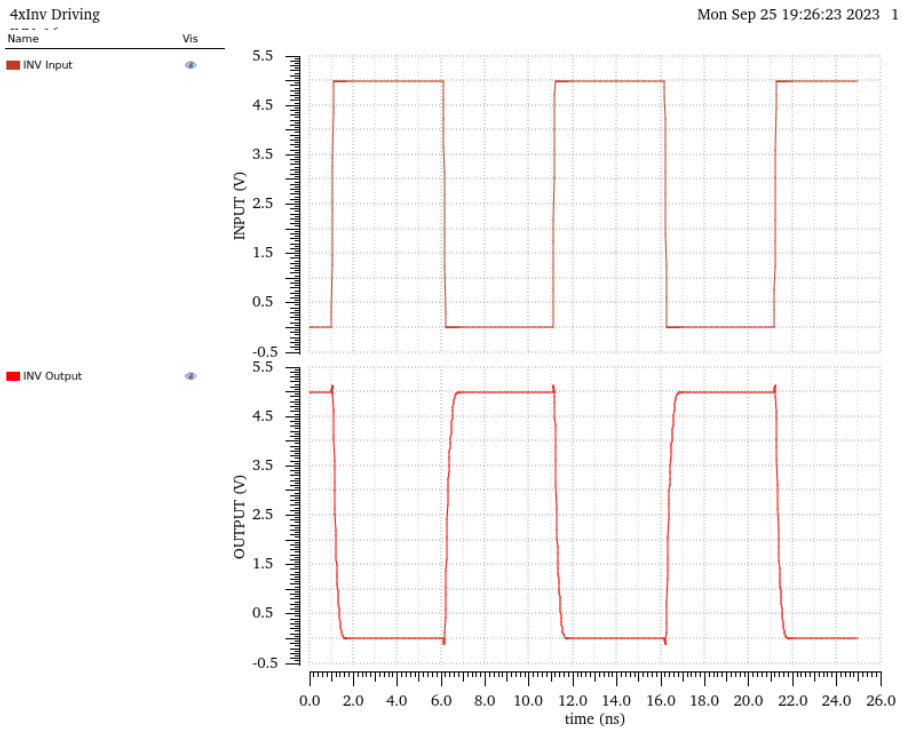

Figure 21: Input and output results of the quadruple sized inverter with a load of sixteen inverters, which uses the INVx4.

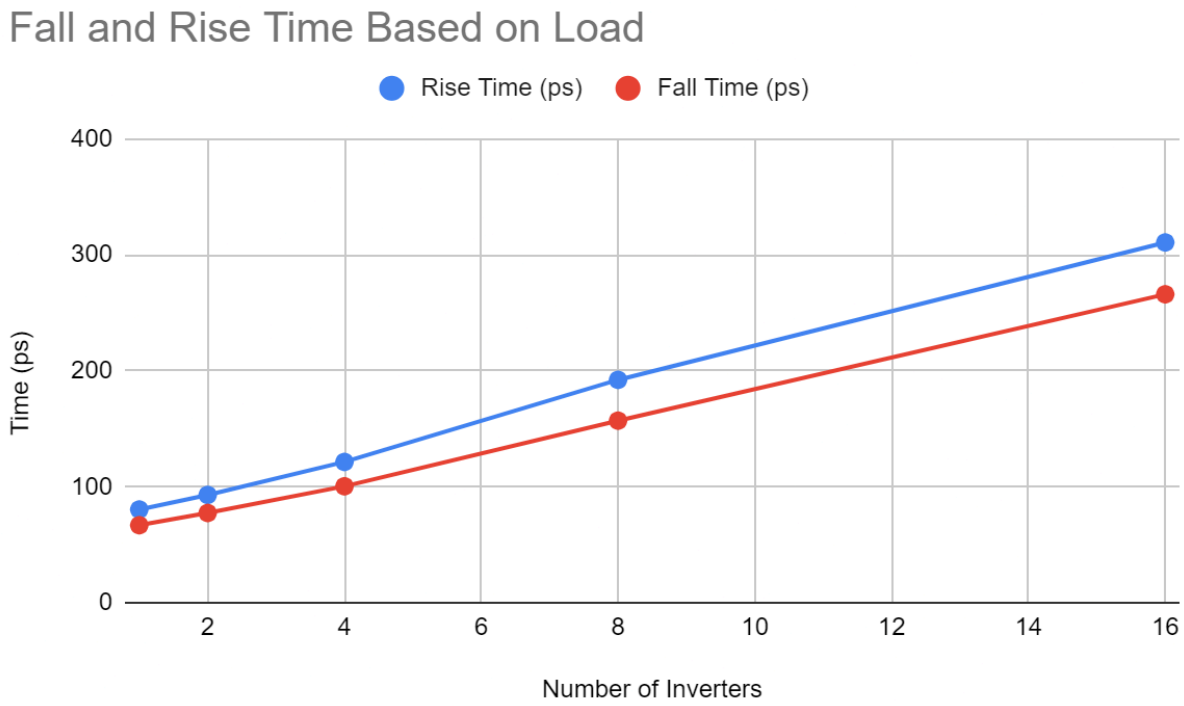

Figure 22: Graph showing a near linear increase in fall and rise time when the load is increased using data from Table 3, which uses the INVx4.

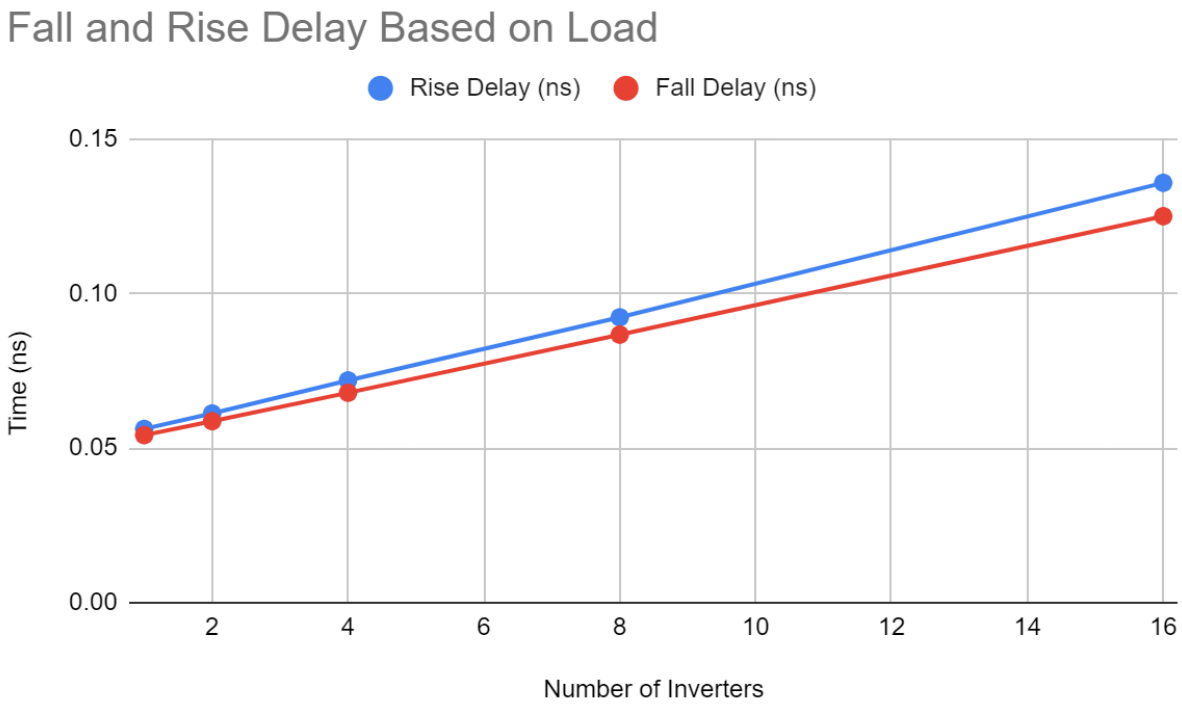

Figure 23: Graph showing a near linear increase in fall and rise delay when the load is increased using data from Table 3, which uses the INVx4.

Table 3: Comparing rise and fall times and delays of the INVx4 based on load.

Inverters	Rise Time (ps)	Fall Time (ps)	Rise Delay (ns)	Fall Delay (ns)
1	80.38	66.83	0.0562	0.0542
2	92.92	77.37	0.0612	0.0587
4	121.4	100.4	0.0719	0.0679
8	192.2	157.0	0.0923	0.0867
16	310.7	266.0	0.1358	0.1250

NAND Simulation Results

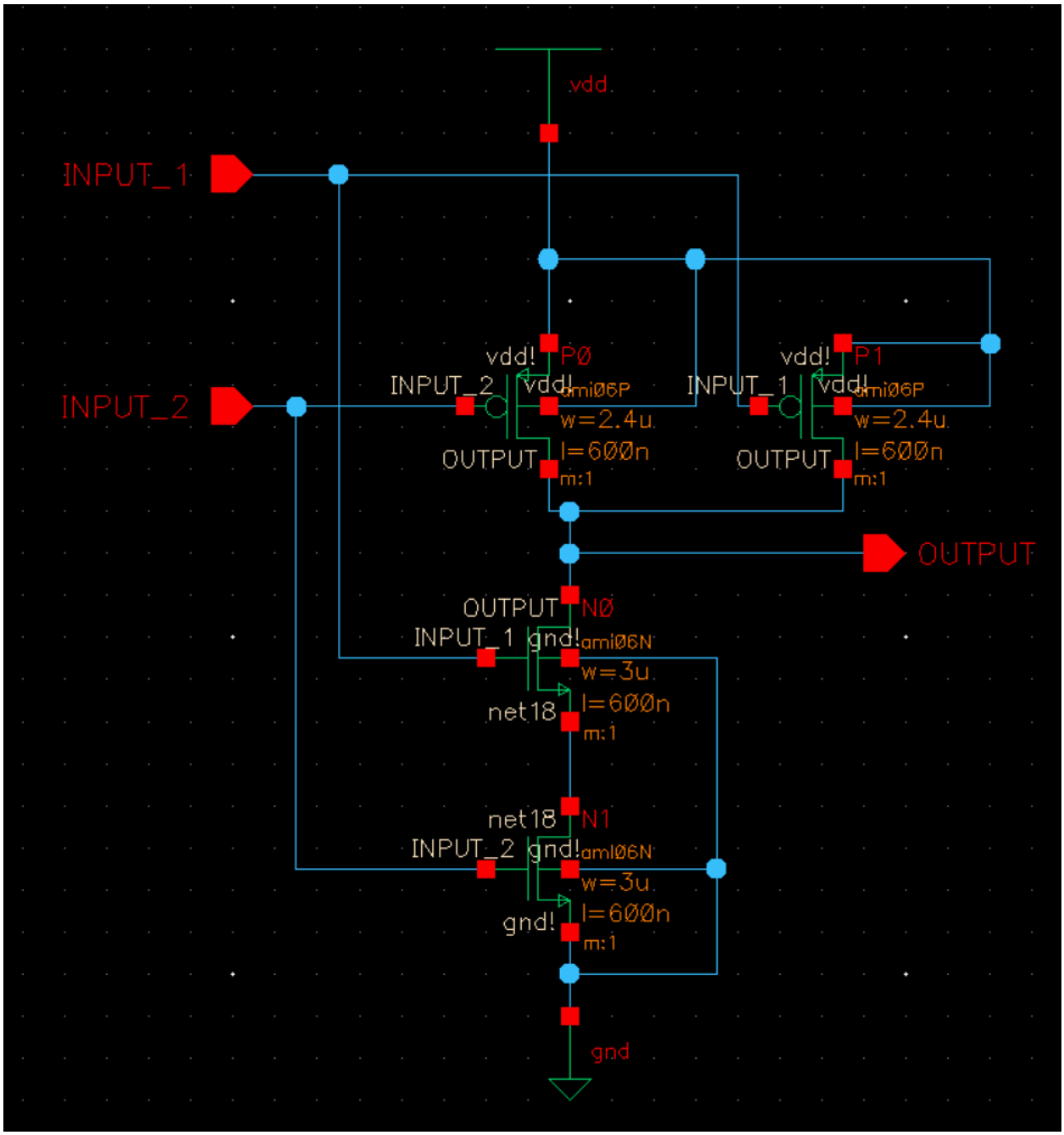

Figure 24: Schematic for NAND gate.

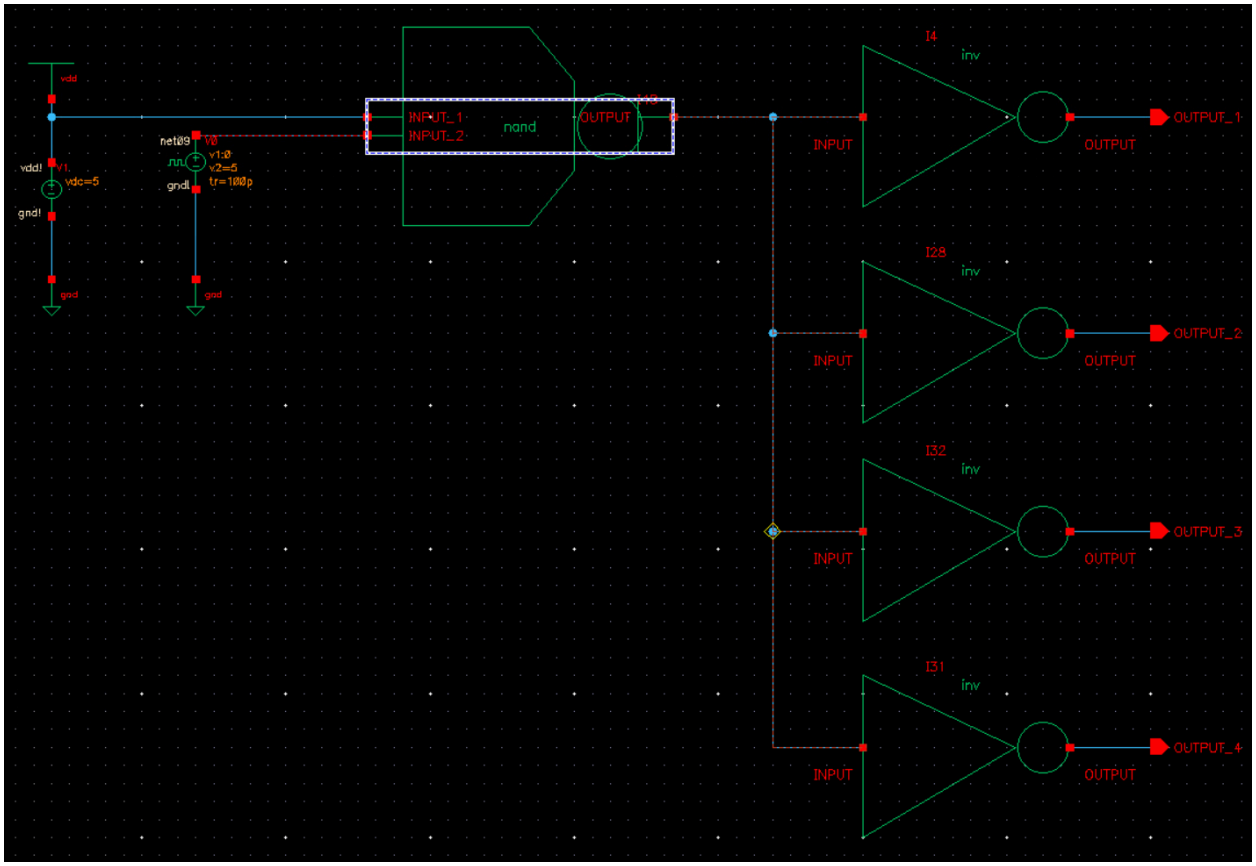

Figure 25: Schematic of “testbench” used for simulation for a load of 4 inverters. This style of simulation was used to retrieve the results in Table 4. Table 5’s testbench is similar, but instead the constant is held on input 2 of the NAND gate.

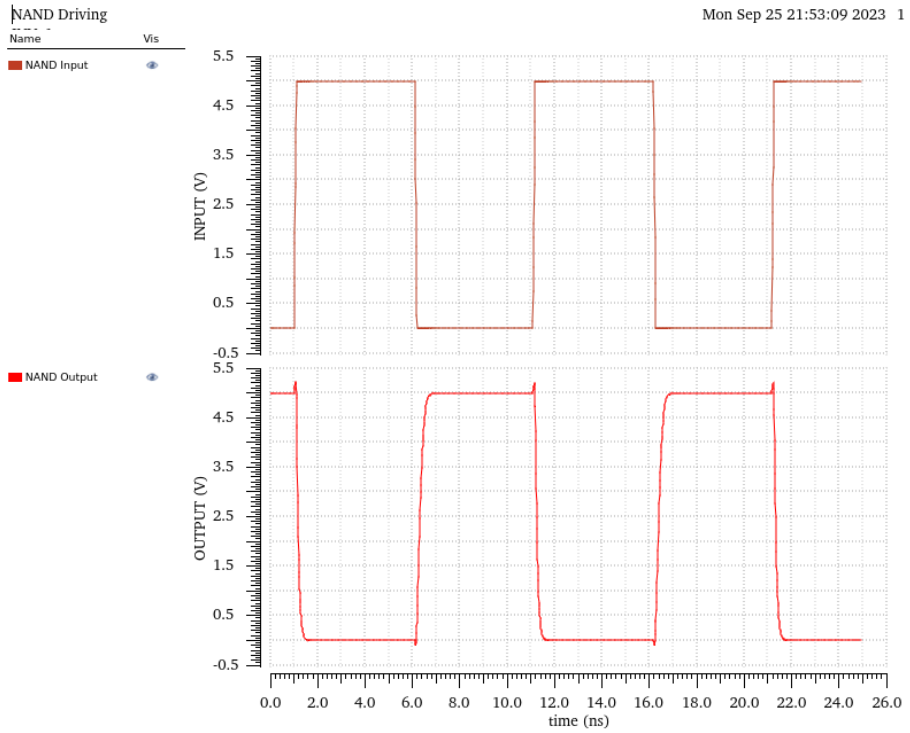

Figure 26: Input and output results of NAND with input 1 as constant with a load of one inverter.

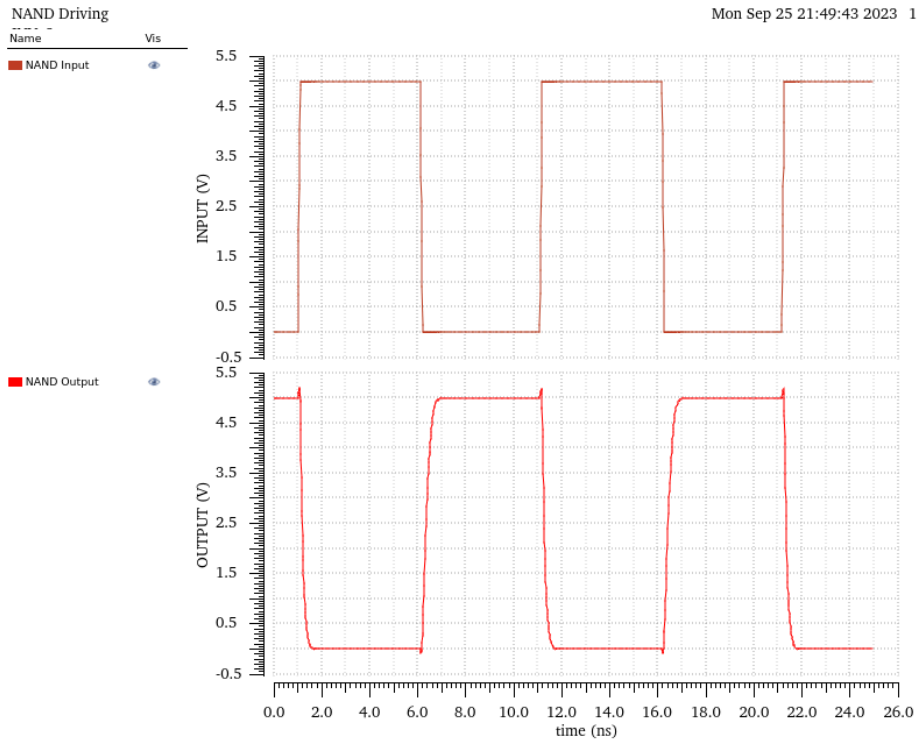

Figure 27: Input and output results of NAND with input 1 as constant with a load of two inverters.

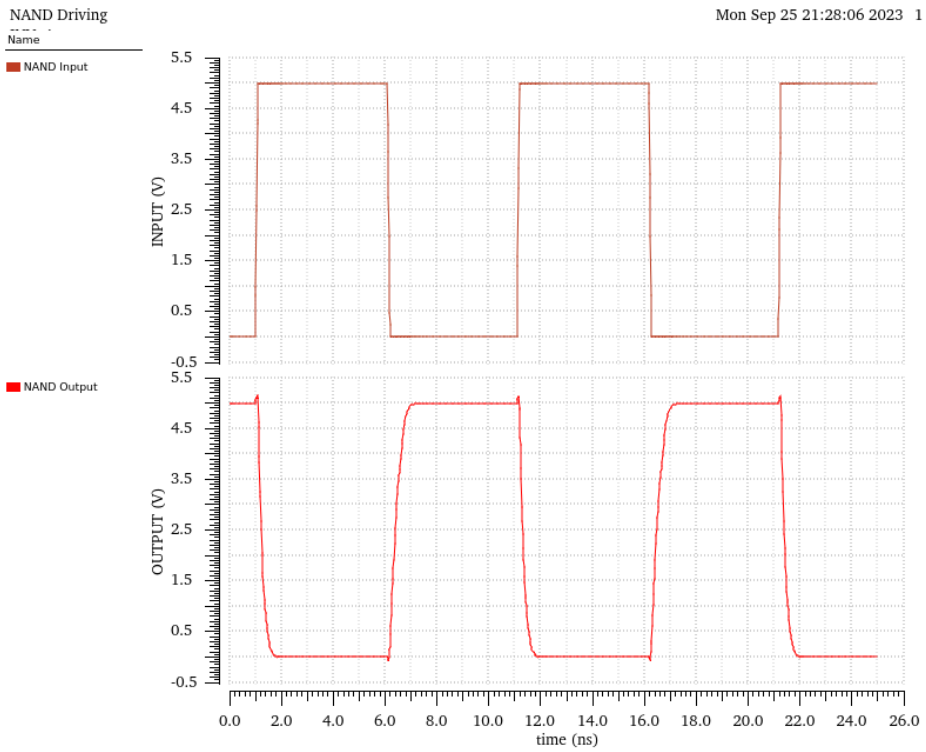

Figure 27: Input and output results of NAND with input 1 as constant with a load of four inverters.

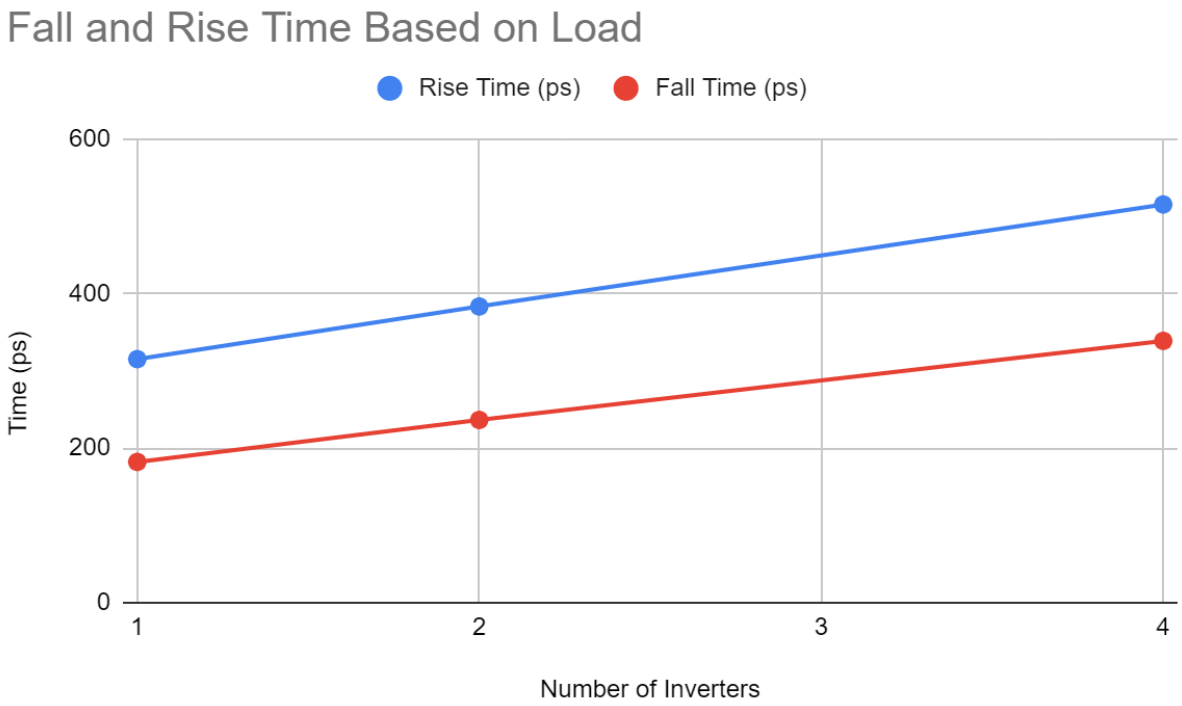

Figure 28: Graph showing a near linear increase in fall and rise time when the load is increased using data from Table 4, which uses the NAND with input 1 held constant.

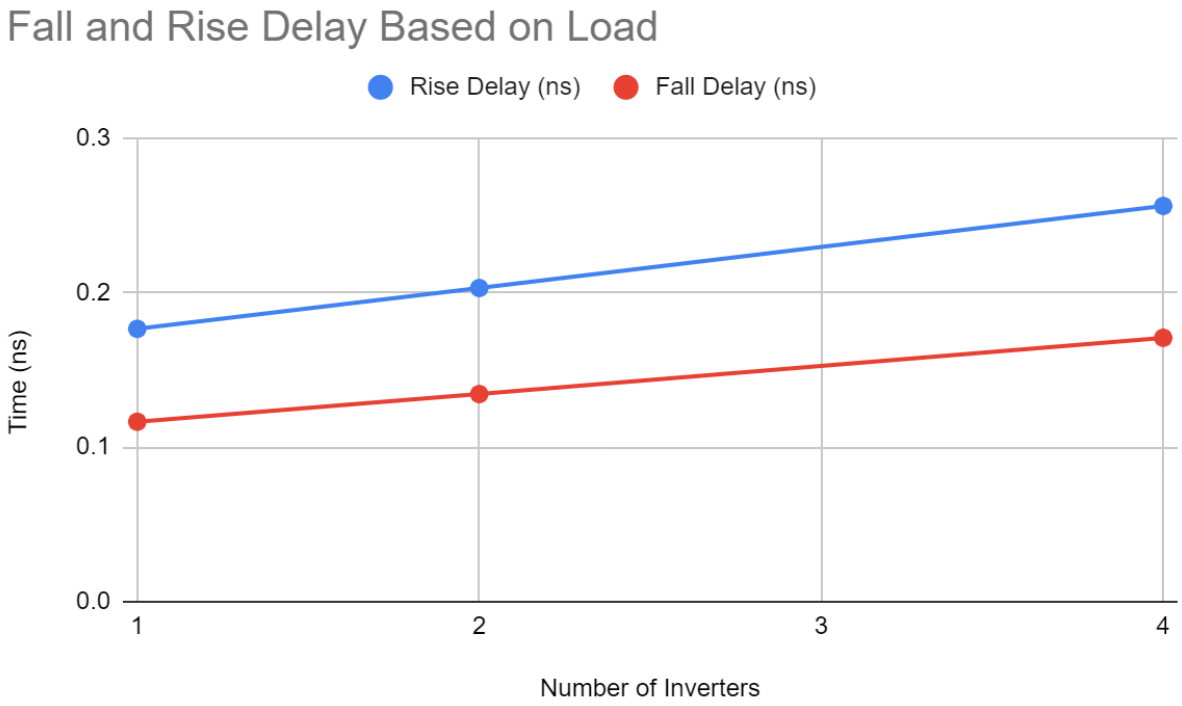

Figure 29: Graph showing a near linear increase in fall and rise delay when the load is increased using data from Table 4, which uses the NAND with input 1 held constant.

Table 4: Comparing rise and fall times and delays of a NAND gate with input 1 held constant based on load.

Inverters	Rise Time (ps)	Fall Time (ps)	Rise Delay (ns)	Fall Delay (ns)
1	315.1	182.1	0.1765	0.1164
2	383.2	236.4	0.2029	0.1343
4	515.2	338.7	0.2560	0.1707

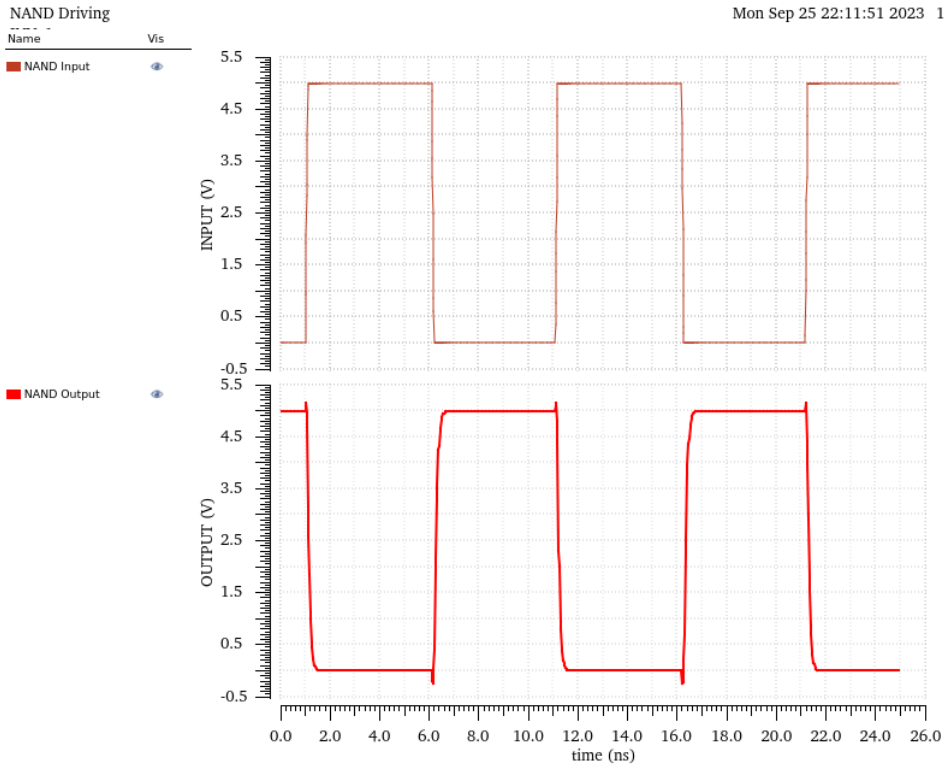

Figure 30: Input and output results of NAND with input 2 as constant with a load of one inverter.

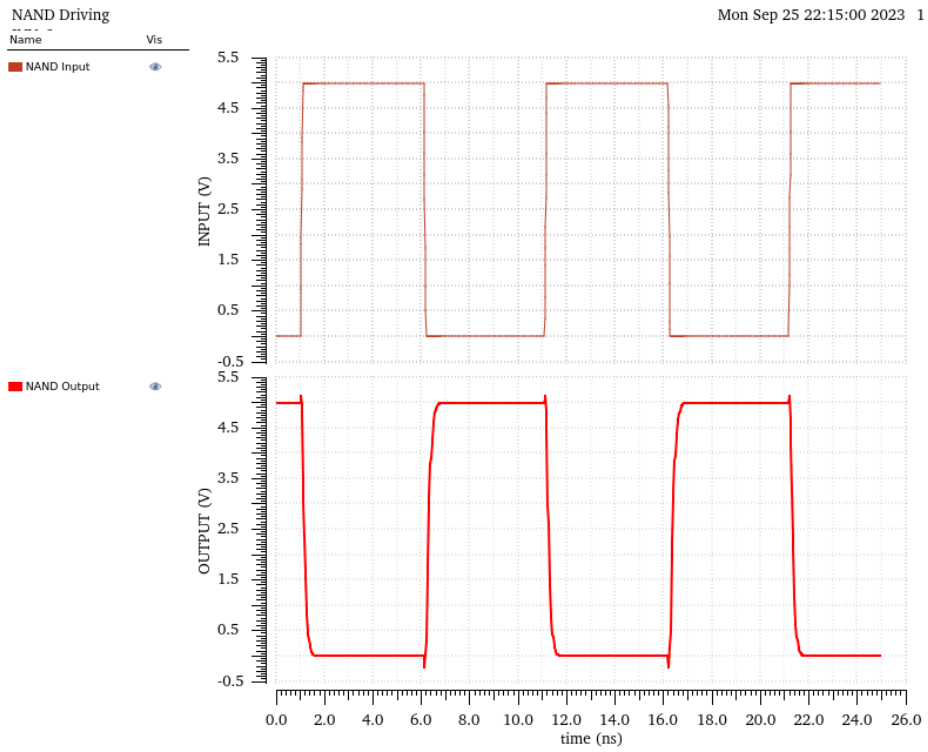

Figure 31: Input and output results of NAND with input 2 as constant with a load of two inverters.

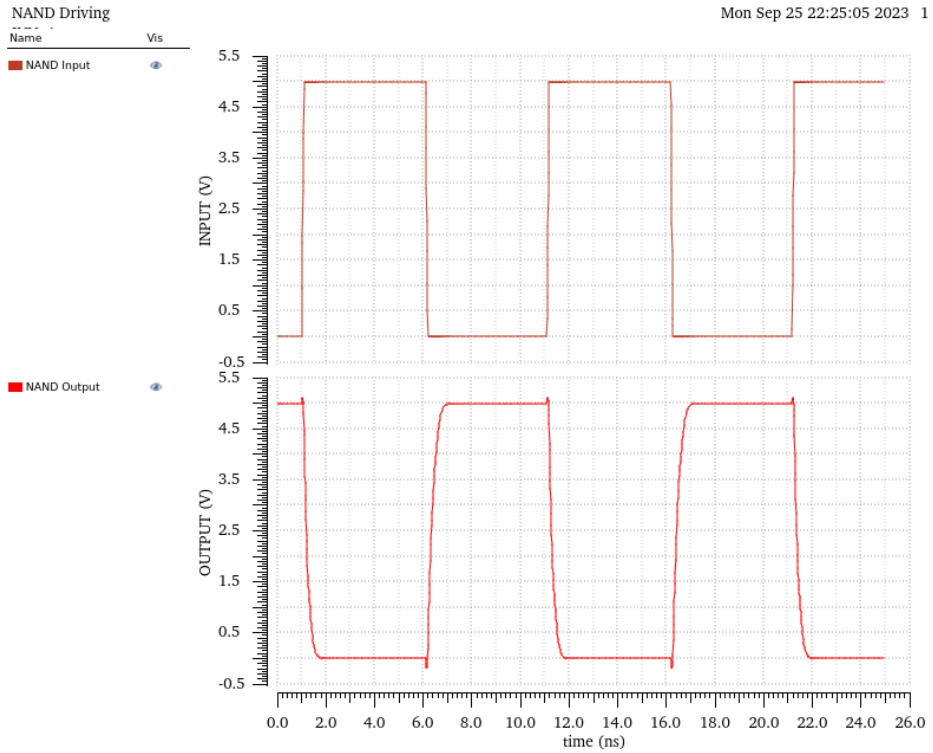

Figure 32: Input and output results of NAND with input 2 as constant with a load of four inverters.

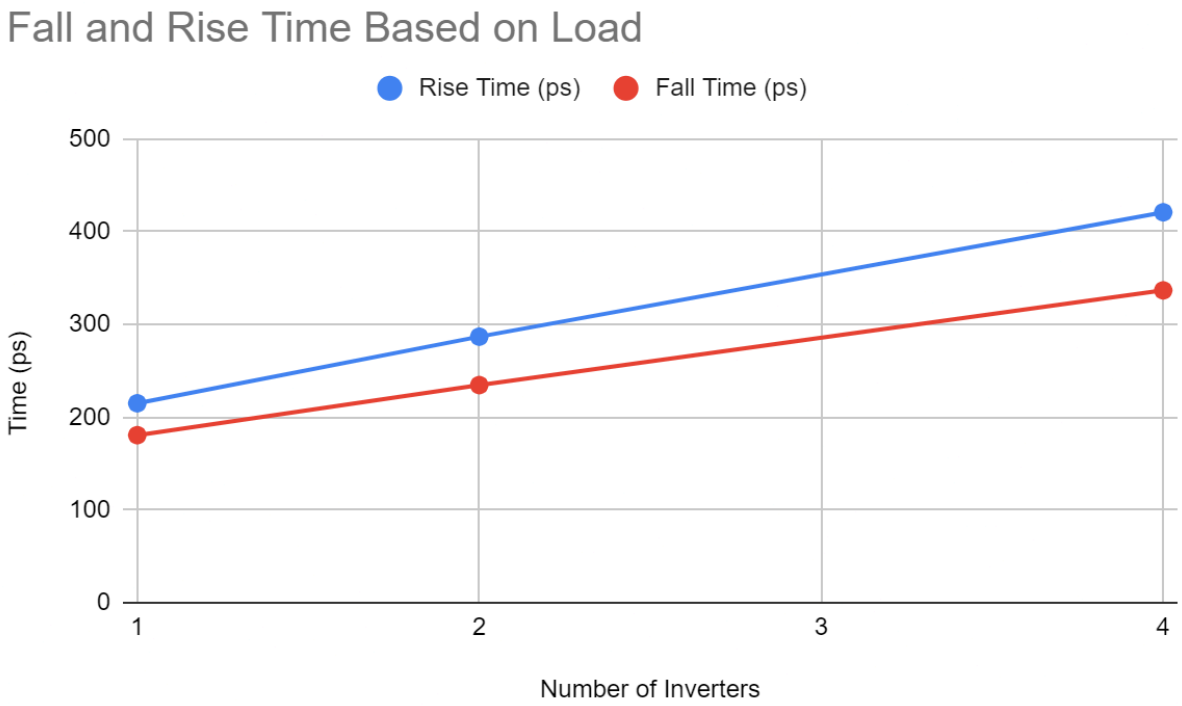

Figure 33: Graph showing a near linear increase in fall and rise time when the load is increased using data from Table 5, which uses the NAND with input 2 held constant.

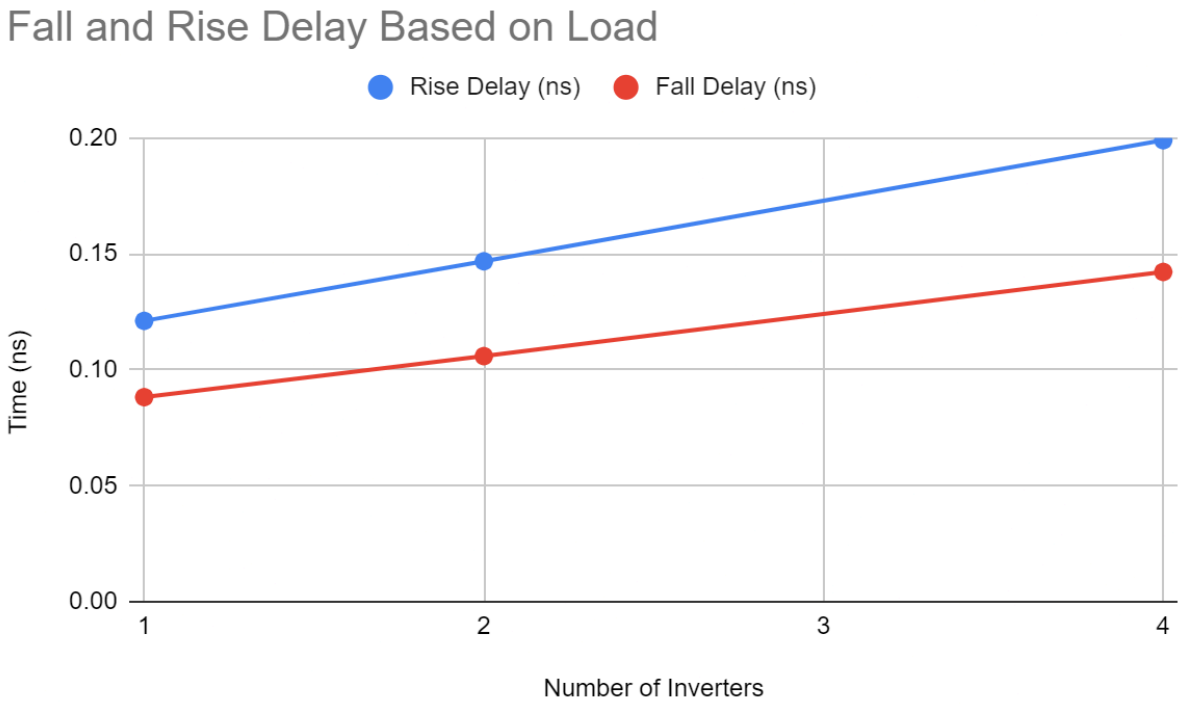

Figure 34: Graph showing a near linear increase in fall and rise delay when the load is increased using data from Table 5, which uses the NAND with input 2 held constant.

Table 5: Comparing rise and fall times and delays of a NAND gate with input 2 held constant based on load.

Inverters	Rise Time (ps)	Fall Time (ps)	Rise Delay (ns)	Fall Delay (ns)
1	215.0	180.6	0.1211	0.0882
2	286.8	234.6	0.1468	0.1059
4	420.9	336.7	0.1990	0.1422

NOR Simulation Results

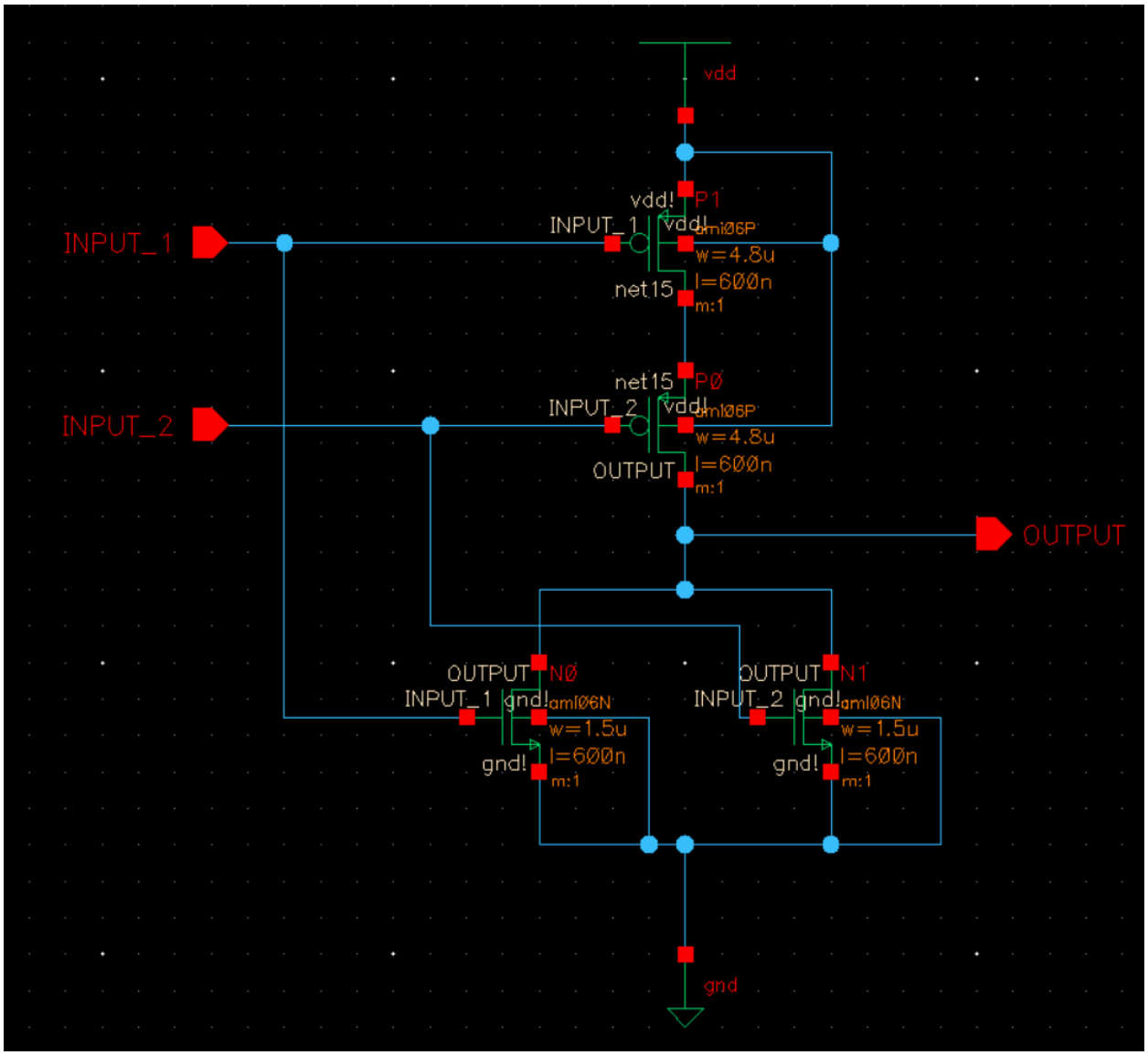

Figure 35: Schematic for NOR gate.

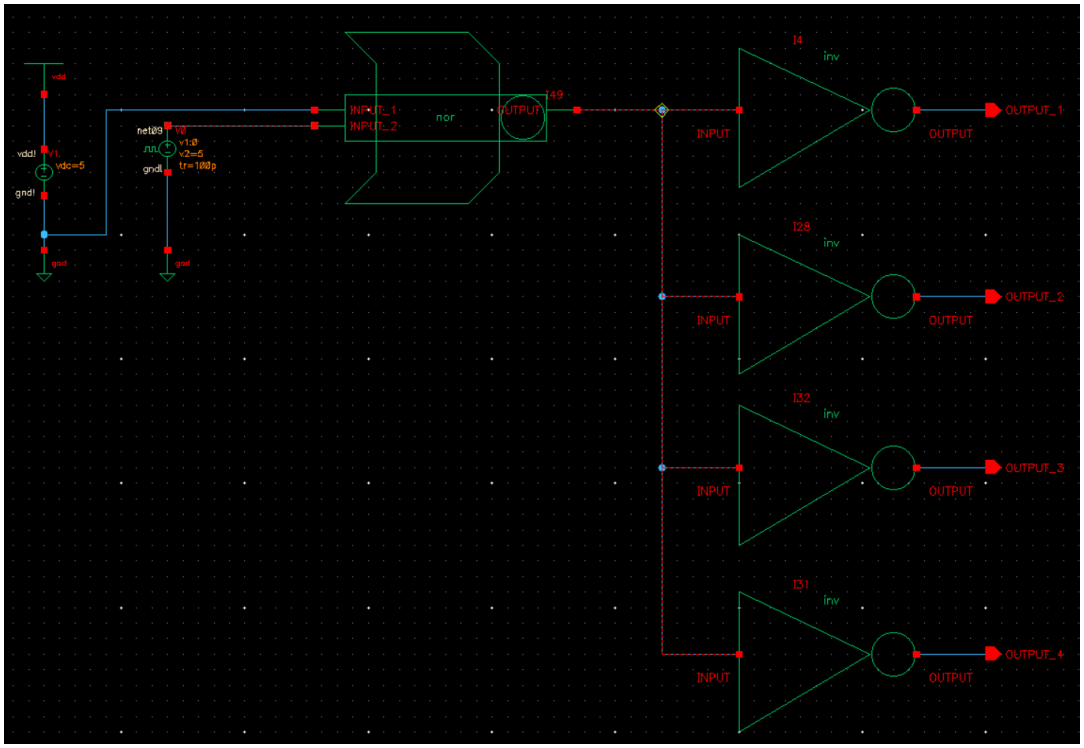

Figure 36: Schematic of “testbench” used for simulation for a load of 4 inverters. This style of simulation was used to retrieve the results in Table 6 and Table 7. Table 7’s testbench is similar, but instead the constant is held on input 2 of the NOR gate.

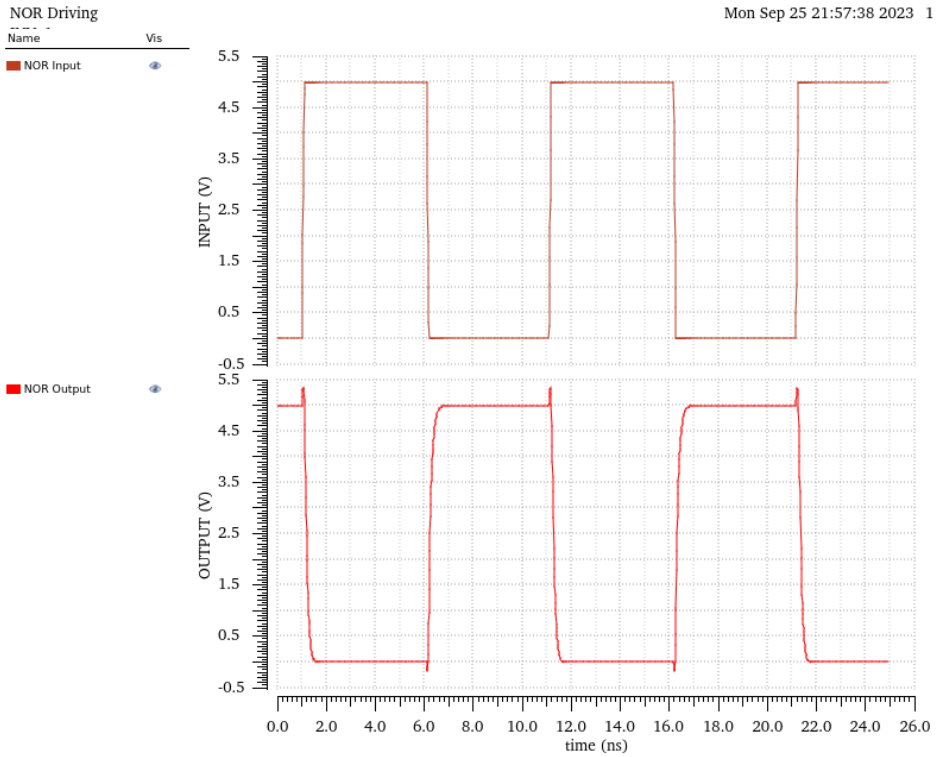

Figure 37: Input and output results of NOR with input 1 as constant with a load of one inverter.

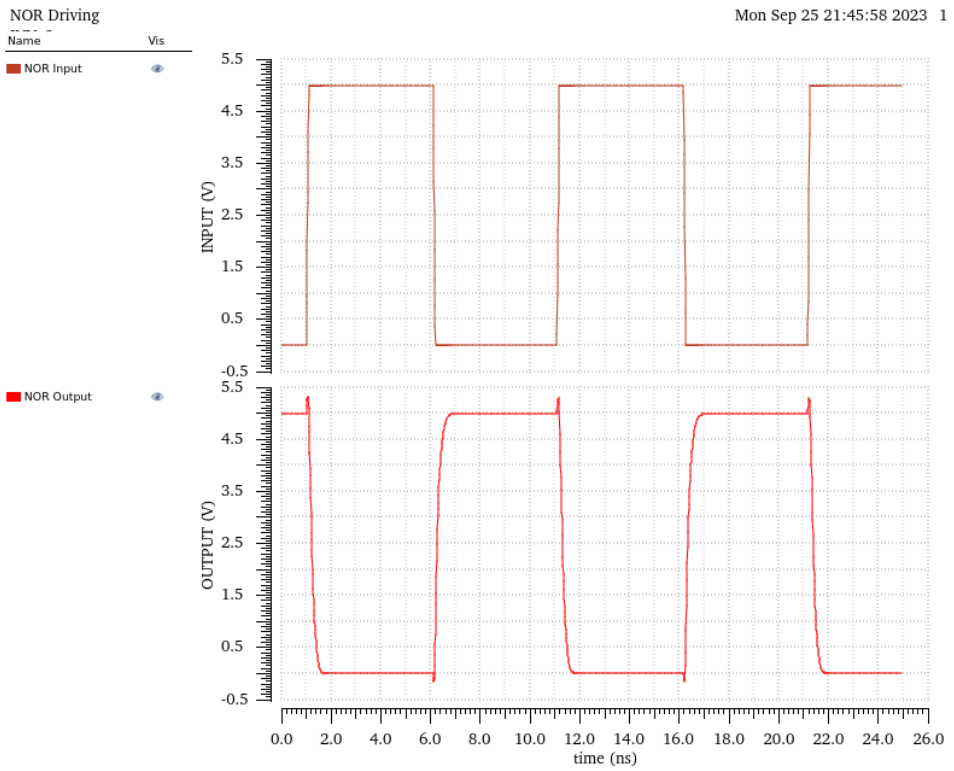

Figure 38: Input and output results of NOR with input 1 as constant with a load of two inverters.

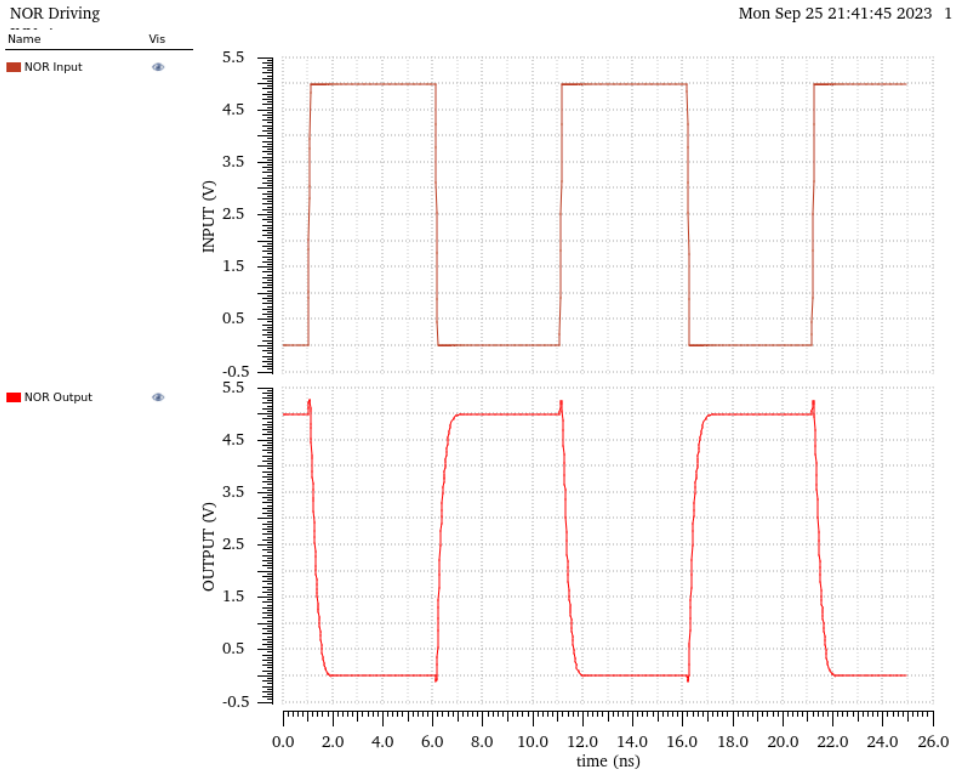

Figure 39: Input and output results of NOR with input 1 as constant with a load of four inverters.

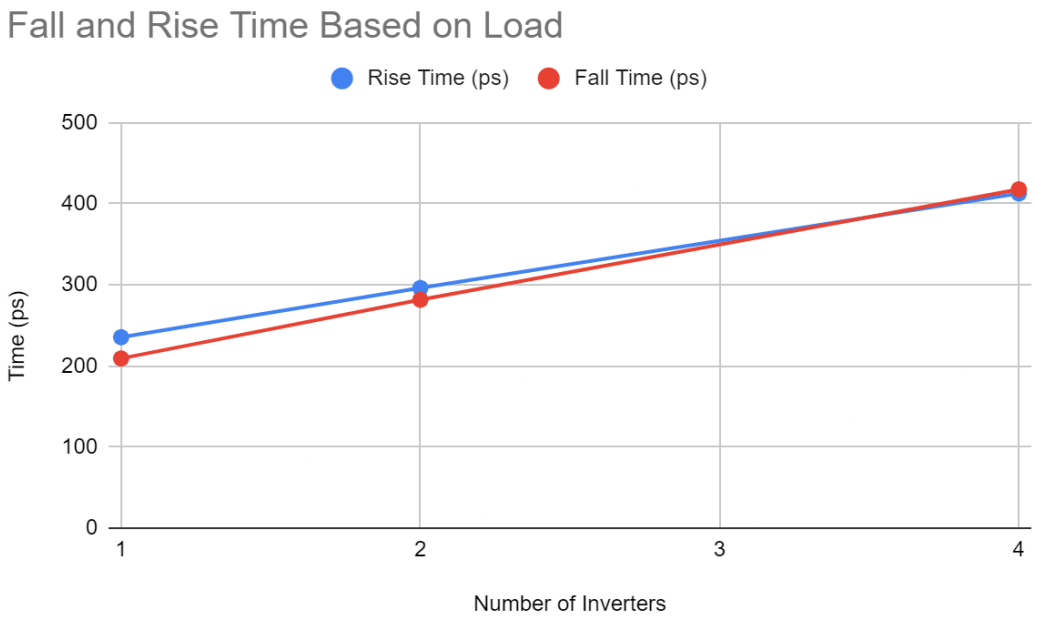

Figure 40: Graph showing a near linear increase in fall and rise time when the load is increased using data from Table 6, which uses the NOR with input 1 held constant.

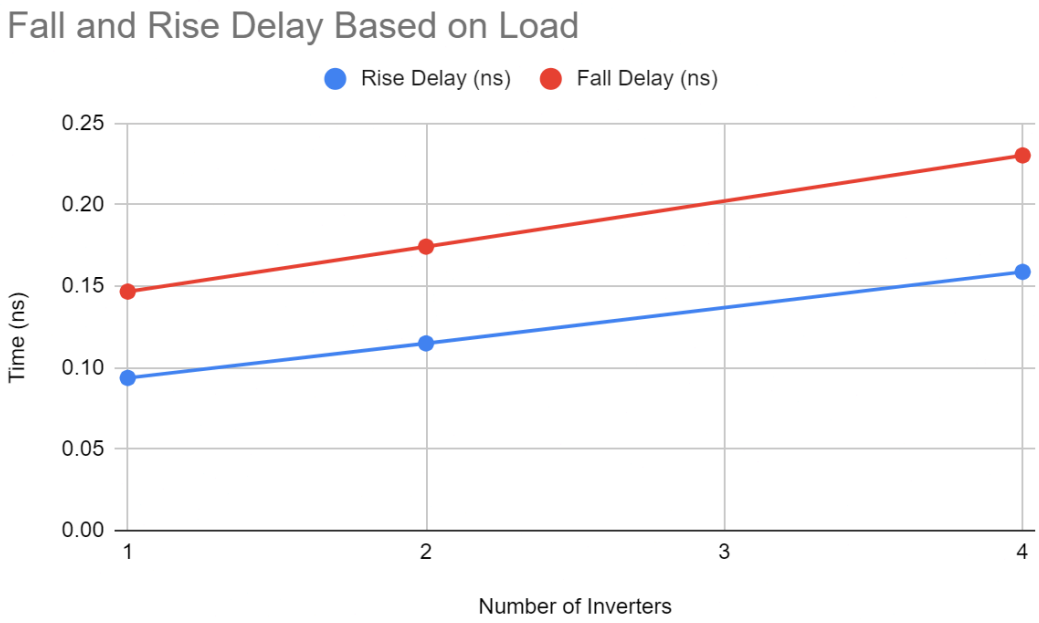

Figure 29: Graph showing a near linear increase in fall and rise delay when the load is increased using data from Table 6, which uses the NOR with input 1 held constant.

Table 6: Comparing rise and fall times and delays of a NOR gate with input 1 held constant based on load.

Inverters	Rise Time (ps)	Fall Time (ps)	Rise Delay (ns)	Fall Delay (ns)
1	235.4	209.2	0.0937	0.1467
2	296.1	281.6	0.1149	0.1743
4	412.7	417.8	0.1588	0.2303

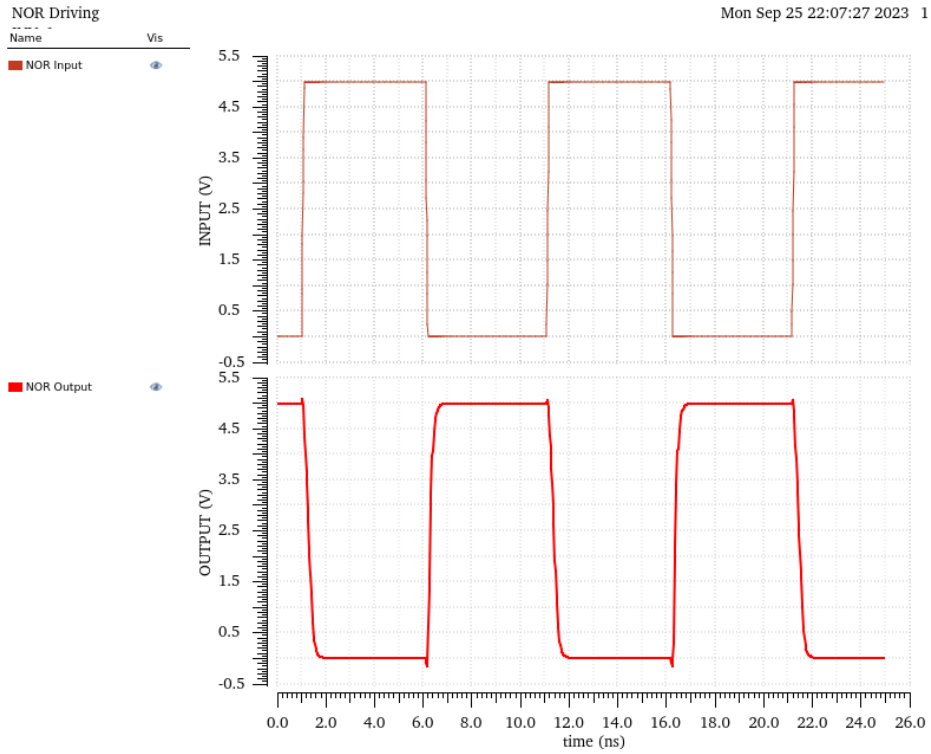

Figure 42: Input and output results of NOR with input 2 as constant with a load of one inverter.

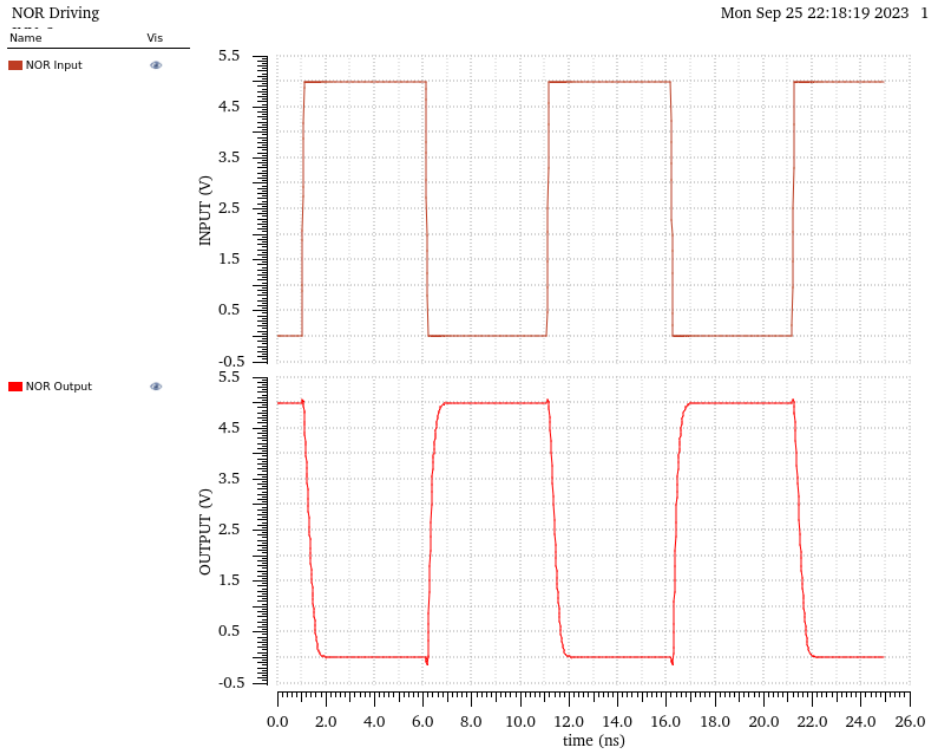

Figure 43: Input and output results of NOR with input 2 as constant with a load of two inverters.

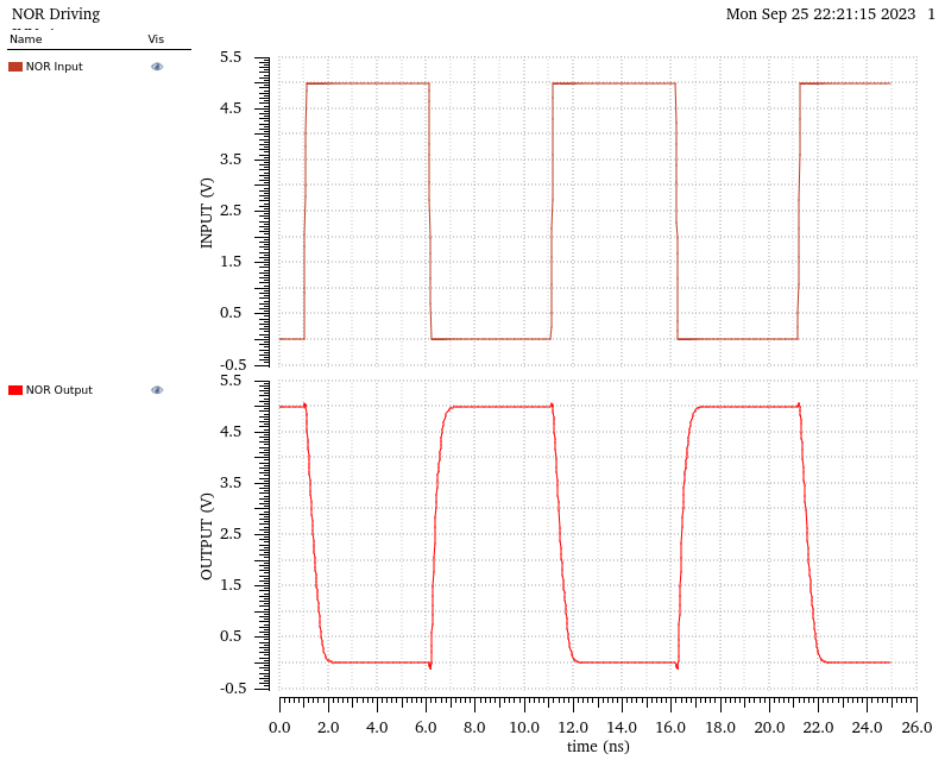

Figure 43: Input and output results of NOR with input 2 as constant with a load of three inverters.

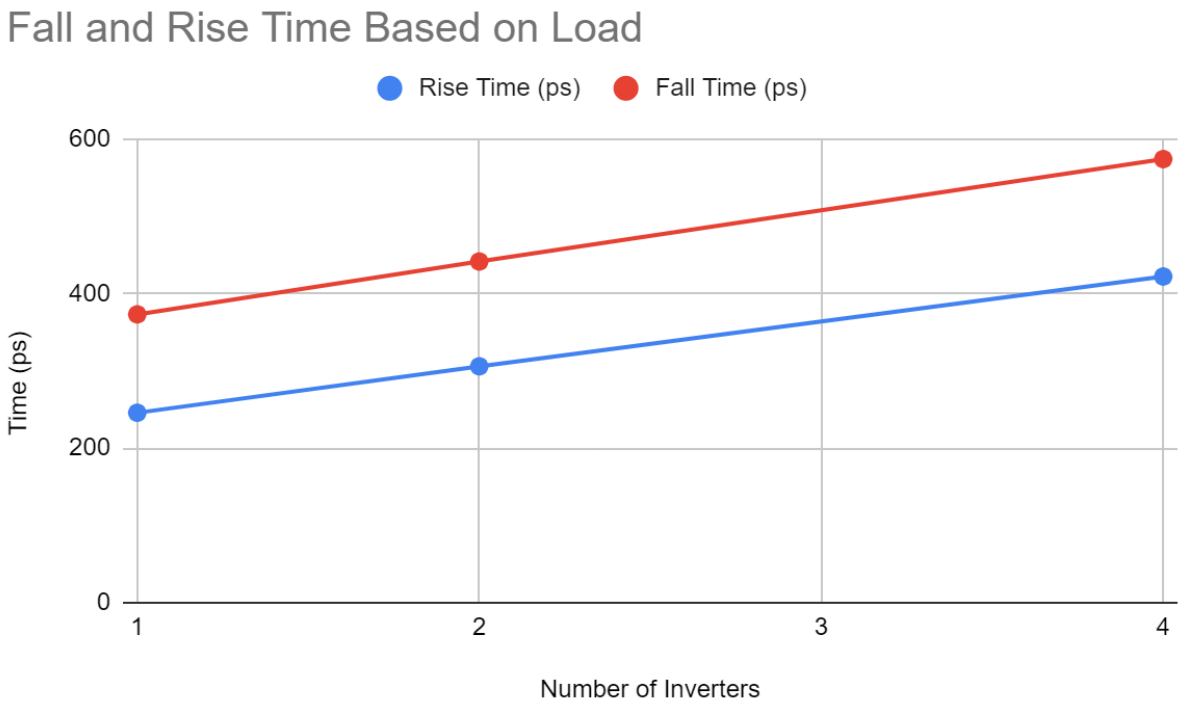

Figure 44: Graph showing a near linear increase in fall and rise time when the load is increased using data from Table 7, which uses the NOR with input 2 held constant.

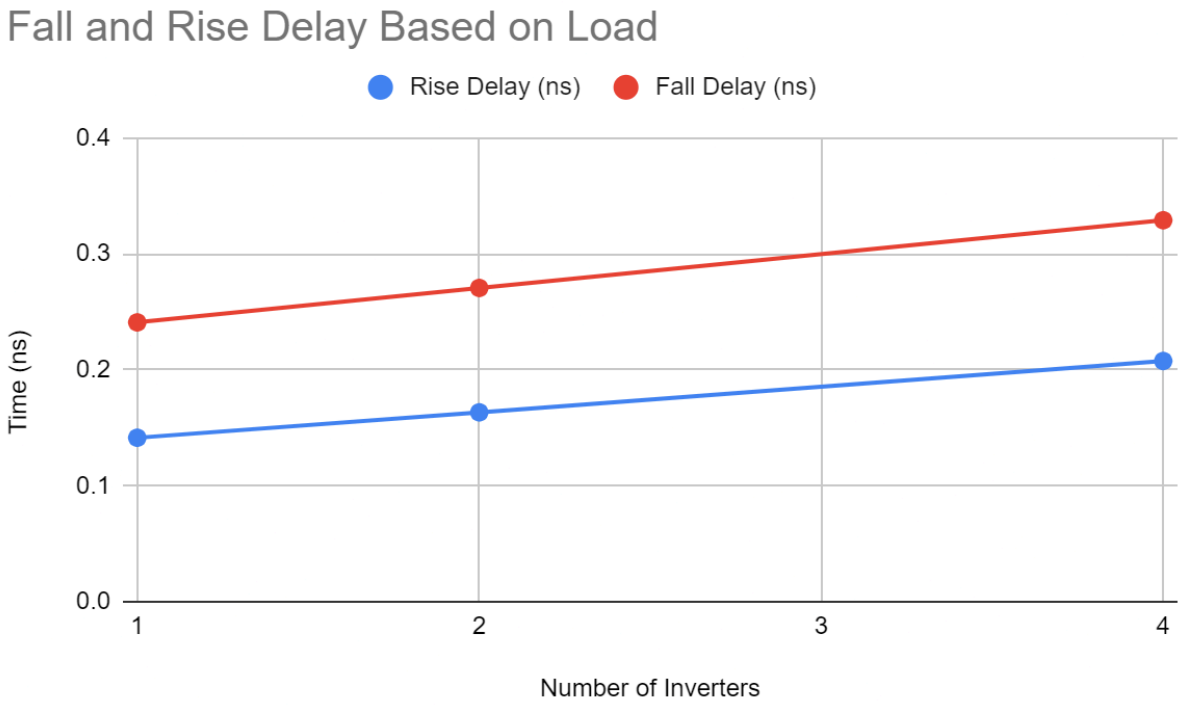

Figure 29: Graph showing a near linear increase in fall and rise delay when the load is increased using data from Table 7, which uses the NOR with input 2 held constant.

Table 7: Comparing rise and fall times and delays of a NOR gate with input 2 held constant based on load.

Inverters	Rise Time (ps)	Fall Time (ps)	Rise Delay (ns)	Fall Delay (ns)
1	245.7	373.0	0.1414	0.2409
2	305.8	441.4	0.1633	0.2706
4	422.0	573.9	0.2076	0.3290

Conclusion

Table 8: Dimensions of NMOS and PMOS transistors for each gate.

Gate Name	NMOS		PMOS	
	Width (uM)	Length (nM)	Width (uM)	Length (nM)
INVx1	1.5	600	2.4	600
INVx2	3.0	600	4.8	600
INVx4	6.0	600	9.6	600
NAND	3.0	600	2.4	600
NOR	1.5	600	4.8	600

1. Observing Figure 8 and other graphs mapping fall and rise time in relation to load, it can be concluded that the greater the load that has to be driven by the gate, the greater the fall and rise time will be. This relationship is linear.

2. Observing Figure 9 and other graphs mapping fall and rise delay in relation to load, it can be concluded that the greater the load that has to be driven by the gate, the greater the fall and rise delay will be. This relationship is linear.

3. Looking at Tables 1 through 3, it can be concluded that increasing the width of the NMOS and PMOS transistors (drive strength) significantly decreases the fall and rise time of an inverter. This relationship is linear. It is hypothesized that this would be true for other gate types.

4. Looking at Tables 1 through 3, it can be concluded that increasing the width of the NMOS and PMOS transistors significantly decreases the fall and rise delay of an inverter. This relationship is linear. It is hypothesized that this would be true for other gate types.

5. Looking at Tables 4 and 5, it can be concluded that the input held constant does affect both the fall and rise delay and rise time for a NAND gate. When input 1 was held constant, the NAND saw an increase in fall and rise delay and rise time. The PMOS transistor that input 1 was tied to was further from ground, which explains this behavior.

6. Looking at Tables 6 and 7, it can be concluded that the input held constant does affect both the fall and rise delay and fall time for a NOR gate. When input 2 was held constant, the NOR saw an increase in fall and rise delay and fall time. The NMOS transistor that input 1 was tied to was further from Vdd, which explains this behavior.