



15 USB

The USB core used in the Videocore is build from Synopsys IP. Details about the block can be found in [DWC_otg_databook.pdf](#) (Which can also be downloaded from https://www.synopsys.com/dw/ipdir.php?ds=dwc_usb_2_0_hs_otg).

15.1 Configuration

A number of features of the block are specified before the block is build and thus can not be changed using software. The above mentioned document has a list of these under the chapter "Configuration Parameters". The following table list all configuration parameters mentioned in that chapter and the values which have been chosen.

Feature/Parameter	Selected value
Mode of Operation	0: HNP- and SRP-Capable OTG (Device and Host)
LPM Mode of Operation	0: Non-LPM-capable core
HSIC Mode of Operation	0: Non-HSIC-capable core
Architecture	2: Internal DMA
Point-to-Point Application Only	0: No
High-Speed PHY Interfaces	1: UTMI+
USB 1.1 Full-Speed Serial Transceiver Interface	1: Dedicated FS
USB IC_USB Transceiver Interface	0: Non-IC_USB-capable
Default (Power on) Interface selection: FS_USB/IC_USB	0 : FS_USB interface
Data Width of the UTMI+ Interface	0: 8 bits
Enable I2C Interface	0: None
Enable ULPI Carkit	0: No
Enable PHY Vendor Control Interface	0: No



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Feature/Parameter	Selected value
Number of Device Mode Endpoints in Addition to Control Endpoint 0	7
Enable Dedicated Transmit FIFOs for Device IN Endpoints	1: Yes
Enable descriptor based scatter/gather DMA	0: No
Enable Option for Endpoint- Specific Interrupt	0: No
Number of Device Mode Periodic IN Endpoints	0
Number of Device Mode IN Endpoints including Control Endpoint 0	8
Number of Device Mode Control Endpoints in Addition to Endpoint 0	0
Number of Host Mode Channels	8
Is Periodic OUT Channel Support Needed in Host Mode	1: Yes
Total Data FIFO RAM Depth	4096
Enable Dynamic FIFO Sizing	1: Yes
Largest Rx Data FIFO Depth	4096
Largest Non-Periodic Host Tx Data FIFO Depth	1024
Largest Non-periodic Tx Data FIFO Depth	4096
Largest Host Mode Tx Periodic Data FIFO Depth	4096
Non-periodic Request Queue Depth	8
Host Mode Periodic Request Queue Depth	8
Device Mode IN Token Sequence Learning Queue Depth	8
Width of Transfer Size Counters	19



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Feature/Parameter	Selected value
Width of Packet Counters	10
Remove Optional Features	0: No
Power-on Value of User ID Register	0x2708A000
Enable Power Optimization	0: No
Is Minimum AHB Operating Frequency Less than 60 MHz	1: Yes
Reset Style of Clocked always Blocks in RTL	0: Asynchronous
Instantiate Double- Synchronization Flops	1: Yes
Enable Filter on "iddig" Signal from PHY	1: Yes
Enable Filter on "vbus_valid" Signal from PHY	1: Yes
Enable Filter on "a_valid" Signal from PHY	1: Yes
Enable Filter on "b_valid" Signal from PHY	1: Yes
Enable Filter on "session_end" Signal from PHY	1: Yes
Direction of Endpoints	Mode is {IN and OUT} for all endpoints
Largest Device Mode Periodic Tx Data FIFO n Depth	768 for all endpoints (Except 0)
Largest Device Mode IN Endpoint Tx FIFO Depth (n = 0 to 15) when using dynamic FIFO sizing	0=32 1..5=512 6,7=768

15.2 Extra / Adapted registers.

Besides the registers as specified in the documentation of Synopsys a number of extra registers have been added. These control the Analogue USB Phy and the connections of the USB block into the Video core bus structure. Also the USB_GAHBCFG register has an alternative function for the bits [4:1].

Base Address of the USB block – 0x7E98_0000



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Offset Address	Description		Size	Read/Write
0x080	USB_MDIO_CNTL	MDIO interface control		R/W
0x084	USB_MDIO_GEN	Data for MDIO interface	32	R/W
0x088	USB_VBUS_DRV	Vbus and other Miscellaneous controls		R/W

USB MDIO Control (USB_MDIO_CNTL)

Address 0x 7E98 0080

Bit Number	Field Name	Description	Read/Write	Reset
31	mdio_busy	1= MDIO read or write in progress 0= MDIO Idle	R	0
30-24	-	Unused	-	0
23	bb_mdo	Direct write (bitbash) MDO output	R/W	0
22	bb_mdc	Direct write (bitbash) MDC output	R/W	0
21	bb_enbl	1= MDIO bitbash enable 0= MDIO under control of the phy	R/W	0
20	freerun	1= MDC is continuous active 0 = MDC only active during data transfer	R/W	0
19:16	mdc_ratio	MDC clock freq is sysclk/mdc_ratio	R/W	0
15:0	mdi	16-bit read of MDIO input shift register. Updates on falling edge of MDC	RO	0

Table 15-1 MDIO Control

USB MDIO Data (USB_MDIO_DATA)

Address 0x 7E98 0084

Bit Number	Field Name	Description	Read/Write	Reset
31-0	mdio_data	32-bit sequence to send over MDIO bus	W	0
31-0	mdio_data	32-bit sequence received from MDIO bus	R	0

Table 15-2 USB MDIO data

A Preamble is not auto-generated so any MDIO access must be preceded by a write to this register of 0xFFFFFFFF. Furthermore, a bug in the USB PHY requires an extra clock edge so a write of 0x00000000 must follow the actual access.



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USB VBUS (USB_VBUS)

Address 0x 7E98 0088

Bit Number	Field Name	Description	Read/Write	Reset
31-20	-	Unused	-	0
19-16	axi_priority	Sets the USB AXI priority level	R/W	0
15:10	-	Unused	-	0
9	vbus_irq	1=one or more bits of [6:4] have changed since last read. This bit is cleared when the register is read.	RC	0
8	vbus_irq_en	1=Enable IRQ on VBUS status change	R/W	0
7	afe_non_driving	1=USB PHY AFE pull ups/pull downs are off 0=Normal USB AFE operation (Has no effect if MDIO mode is enabled in the phy)	R/W	0
6	utmisrp_dischrgvbus	Drive VBUS	R	0
5	utmisrp_chrgvbus	Charge VBUS	R	0
4	utmiotg_drvvbus	Discharge VBUS	R	0
3	utmiotg_valid	A session Valid	R/W	0
2	utmiotg_bvalid	B session Valid	R/W	0
1	utmiotg_vbusvalidd	VBUS valid	R/W	0
0	utmisrp_sessend	Session end	R/W	0

Table 15-3 USB MDIO data

The RW bits in this register are fed into the USB2.0 controller and the RO bits are coming out of it. In the real device, it will be up to the software to communicate this information between the USB2.0 controller and external VBUS device (some of these have I2C control, others will have to interface via GPIO).

USB AHB configuration (USB_GAHBCFG)

Address 0x 7E98 0008

The USB_GAHBCFG register has been adapted. Bits [4:1] which are marked in the Synopsys documentation as "Burst Length/Type (HBstLen)" have been used differently.

- [4] 1 = Wait for all outstanding AXI writes to complete before signalling (internally) that DMA is done.
0 = don't wait.
- [3] Not used
- [2:1] Sets the maximum AXI burst length, but the bits are inverted,
00 = maximum AXI burst length of 4,
01 = maximum AXI burst length of 3,
10 = maximum AXI burst length of 2
11 = maximum AXI burst length of 1