

```
-----INSTRUCTION FETCH STAGE-----
instruction: 1011111111111111001111
```

```
instruction: 00000000000000000000000000000000
```

[illegible][illegible][illegible]

```
instruction: nop
```

[illegible][illegible][illegible]

```
alu_out      = 0000000000000000000000000000000000000000000000000000000
```

```
write_en = 0
```

```
-----INSTRUCTION FETCH STAGE-----
```

instruction: 000000001000000111101100

```
-----INSTRUCTION DECODE STAGE-----
```

```
instruction: 1011111111111111111001111
```

instruction: li

```
field:      01
```

```
immediate: 1111111111111110
```

```
rd:      01111
```

[illegible]

instruction: 000001000011000110001100

[illegible]

```
alu_out      = 00000000000000000000000000000000111111111111110000000000000000
write_en     = 1
```

```
instruction: 1101111111111111111101111
```

```
instruction: a
  rs2(01100) = 1111111111111110000000000000000011111111111111100000000000000000
  rs1(01100) = 1111111111111110000000000000000011111111111111100000000000000000
  rd (01100) = 1111111111111110000000000000000011111111111111100000000000000000
```

-----EXECUTE/WRITE BACK STAGE-----

results.txt

```

instruction: bcw
  rs2      = 0000000000000000000000000000000000000000000000000000000000000000
  rs1      = 0000000000000000000000000000000000111111111111100000000000000000
  rd       = 0000000000000000000000000000000000000000000000000000000000000000

  alu_out  = 1111111111111100000000000000000000111111111111100000000000000000
  write_en = 1

```

Cycle 4

```
-----INSTRUCTION FETCH STAGE-----
instruction: 000001001011000111100001
```

```
-----INSTRUCTION DECODE STAGE-----
instruction: 11011111111111111101111
```

```
instruction: li
field:      10
immediate:  1111111111111111
rd:         01111
```

```
-----EXECUTE/WRITE BACK STAGE-----
instruction: a
```

```
rs2      = 1111111111111100000000000000000011111111111111000000000000000000
rs1      = 1111111111111100000000000000000011111111111111000000000000000000
rd       = 1111111111111100000000000000000011111111111111000000000000000000

alu_out   = 1111111111111100000000000000000011111111111111000000000000000000
write_en  = 1
```

Cycle 5

```
-----INSTRUCTION FETCH STAGE-----
instruction: 0000000100110001111100001
```

```
-----INSTRUCTION DECODE STAGE-----
instruction: 000001001011000111100001
```

[illegible]

```
-----EXECUTE/WRITE BACK STAGE-----
instruction: li
```

[illegible]

```
-----INSTRUCTION FETCH STAGE-----
instruction:  0000000110110001111100001
```

[illegible][illegible]

```
-----INSTRUCTION FETCH STAGE-----
instruction: 0000001000000000111100001
```

[illegible]

```
instruction: and
      rs2      = 1111111111111100000000000000000011111111111111000000000000000000
```

[illegible]

results.txt

[illegible]

Cycle 12

```
-----INSTRUCTION FETCH STAGE-----
```

```
instruction: 000001010011110000101100
```

```
-----INSTRUCTION DECODE STAGE-----
```

instruction: 000000111011010111100001

instruction: shlhi

[illegible]

```
rs1(01111) = 00000000000000000111111111111111111111111111000000000000000
```

[illegible]

```
-----EXECUTE/WRITE BACK STAGE-----
```

```
instruction: rot
```

[illegible]

```
rs1      = 0000000000000000011111111111111111111111111111111000000000000000
```

[illegible][illegible]

```
write_en    = 1
```

Cycle 13

```
-----INSTRUCTION FETCH STAGE-----
```

instruction: 000001011011110110001101

```
-----INSTRUCTION DECODE STAGE-----
```

```
instruction: 000001010011110000101100
```

instruction: ah

[illegible]

```
rs1(00001) = 00000000000000001111111111110111111111110000000000000000
```

```
rd (01100) = 111111111111110000000000000000001111111111110000000000000000
```

```
-----EXECUTE/WRITE BACK STAGE-----
```

instruction: shlhi

[illegible]

```
rs1      = 0000000000000000011111111111111111111111111111100000000000000000
```

```
rd      = 0000000000000000000111111111111111111111111111110000000000000000
```

```

                                results.txt
alu_out    = 0000000000000000111111111111101111111111110000000000000000
write_en   = 1
=====
Cycle 14
-----INSTRUCTION FETCH STAGE-----
instruction: 1001000000000000000001

-----INSTRUCTION DECODE STAGE-----
instruction: 000001011011110110001101
instruction: sfh
    rs2(01111) = 000000000000000011111111111111111111111111000000000000000
    rs1(01100) = 00000000000000001111111111110111111111111101000000000000000
    rd (01101) = 0000000000000000000000000000000000000000000000000000000001

-----EXECUTE/WRITE BACK STAGE-----
instruction: ah
    rs2      = 000000000000000011111111111111111111111111110000000000000000
    rs1      = 000000000000000011111111111110111111111111110000000000000000
    rd       = 111111111111100000000000000000001111111111111000000000000000

    alu_out   = 000000000000000011111111111101111111111111010000000000000000
    write_en  = 1
=====
Cycle 15
-----INSTRUCTION FETCH STAGE-----
instruction: 10101111111111111000001

-----INSTRUCTION DECODE STAGE-----
instruction: 1001000000000000000001
instruction: li
    field:    00
    immediate: 1000000000000000
    rd:       00001

-----EXECUTE/WRITE BACK STAGE-----
instruction: sfh
    rs2      = 000000000000000011111111111111111111111111110000000000000000
    rs1      = 000000000000000011111111111101111111111111110100000000000000
    rd       = 000000000000000000000000000000000000000000000000000000000001

    alu_out   = 000000000000000000000000000000000000000000000000000000000000

```



```
write_en = 1
```

```
=====
```

Cycle 16

```
-----INSTRUCTION FETCH STAGE-----
```

```
instruction: 10100000000000111101101
```

```
-----INSTRUCTION DECODE STAGE-----
```

```
instruction: 10101111111111111000001
```

```
instruction: li
```

```
field: 01
```

```
immediate: 011111111111110
```

```
rd: 00001
```

```
-----EXECUTE/WRITE BACK STAGE-----
```

```
instruction: li
```

```
field: 00
```

```
immediate: 1000000000000000
```

```
rd: 00001
```

```
alu_out = 00000000000000011111111111110111111111111100100000000000000
```

```
write_en = 1
```

```
=====
```

Cycle 17

```
-----INSTRUCTION FETCH STAGE-----
```

```
instruction: 000001100011010110001101
```

```
-----INSTRUCTION DECODE STAGE-----
```

```
instruction: 101000000000000111101101
```

```
instruction: li
```

```
field: 01
```

```
immediate: 0000000000001111
```

```
rd: 01101
```

```
-----EXECUTE/WRITE BACK STAGE-----
```

```
instruction: li
```

```
field: 01
```

```
immediate: 011111111111110
```

```
rd: 00001
```

```
alu_out = 00000000000000011111111111110011111111111101000000000000000
```

```
write_en = 1
```

```
-----INSTRUCTION FETCH STAGE-----
```

```
-----INSTRUCTION DECODE STAGE-----
```

[illegible]

rd: 01101

```
write_en    = 1
```

```
-----INSTRUCTION FETCH STAGE-----
```

```
-----INSTRUCTION DECODE STAGE-----
```

```
rd (01101) = 0000000000000000111111111111010000000000100100000000000000
```

[illegible]

```
write_en    = 1
```

Cycle 20

-----INSTRUCTION FETCH STAGE-----

instruction: 1100101010101010100010

-----INSTRUCTION DECODE STAGE-----

instruction: 1001010101010101000010

instruction: li

field: 00

immediate: 1010101010101010

rd: 00010

-----EXECUTE/WRITE BACK STAGE-----

instruction: sfhs

rs2 = 000000000000000011111111111101111111111110100000000000000000

rs1 = 000000000000000011111111111111111111111110000000000000000000

rd = 000000000000000011111111111101000000000010010000000000000000

alu_out = 000000000000000000000000000010000000000001000000000000000000

write_en = 1

Cycle 21

-----INSTRUCTION FETCH STAGE-----

instruction: 000001110000100001000010

-----INSTRUCTION DECODE STAGE-----

instruction: 1100101010101010100010

instruction: li

field: 10

immediate: 0101010101010101

rd: 00010

-----EXECUTE/WRITE BACK STAGE-----

instruction: li

field: 00

immediate: 1010101010101010

rd: 00010

alu_out = 0000000000000000000000000000000000000000010101010101010

write_en = 1

Cycle 22

-----INSTRUCTION FETCH STAGE-----

instruction: 000001111000010111101101

-----INSTRUCTION DECODE STAGE-----

instruction: 000001110000100001000010

instruction: mpyu

rs2(00010) = 00000000000000000101010101010100000000000000010101010101010

rs1(00010) = 00000000000000000101010101010100000000000000010101010101010

rd (00010) = 00000000000000000101010101010100000000000000010101010101010

-----EXECUTE/WRITE BACK STAGE-----

instruction: li

field: 10

immediate: 01010101010101

rd: 00010

alu_out = 00000000000000000101010101010100000000000000010101010101010

write_en = 1

=====
Cycle 23

-----INSTRUCTION FETCH STAGE-----

instruction: 000001111011110000101101

-----INSTRUCTION DECODE STAGE-----

instruction: 000001111000010111101101

instruction: absdb

rs2(00001) = 0000000000000000011111111111110011111111111110100000000000000

rs1(01111) = 0000000000000000011111111111111111111111111110000000000000000

rd (01101) = 0000000000000000000000000000000100000000000001000000000000000

-----EXECUTE/WRITE BACK STAGE-----

instruction: mpyu

rs2 = 00000000000000000101010101010100000000000000010101010101010

rs1 = 00000000000000000101010101010100000000000000010101010101010

rd = 00000000000000000101010101010100000000000000010101010101010

alu_out = 0001110001110001100011100011100101110001110001100011100011100100

write_en = 1

=====
Cycle 24

-----INSTRUCTION FETCH STAGE-----

```
instruction: 00000111011110000101101
```

[illegible][illegible]

```
alu_out      = 00000000000000000000000000000110000000000000001000000000000000  
write_en     = 1
```

instruction: 010101110011100111000010

```
instruction: 101001000000000000001110
```

```
instruction: li
field:      01
immediate:  0010000000000000
rd:         01110
```

[illegible]

```
alu_out      = 0000000000000000000000000000000011000000000000000100000000000000
write_en     = 1
```

instruction: 010101110011100011000010

```
write_en    = 1
```

Cycle 28

```
-----INSTRUCTION FETCH STAGE-----
```

instruction: 110000000000000010100110

```
-----INSTRUCTION DECODE STAGE-----
```

instruction: 011101110011100011000010

instruction: MS high

[illegible][illegible][illegible][illegible]

```
-----EXECUTE/WRITE BACK STAGE-----
```

instruction: MA high

[illegible][illegible][illegible][illegible][illegible]

```
write_en = 1
```

Cycle 29

```
-----INSTRUCTION FETCH STAGE-----
```

```
instruction: 1000000000000000011000110
```

```
-----INSTRUCTION DECODE STAGE-----
```

```
instruction: 110000000000000010100110
```

```
instruction: li
```

```
field:      10
```

```
immediate: 00000000000000101
```

rd: 00110

```
-----EXECUTE/WRITE BACK STAGE-----
```

instruction: MS high

[illegible][illegible][illegible][illegible]

results.txt

```
alu_out      = 0000000000000000000000000000000011111100000000000000000000000000
write_en     = 1
```

Cycle 30

```
-----INSTRUCTION FETCH STAGE-----
```

```
instruction: 010000110001100011000010
```

```
-----INSTRUCTION DECODE STAGE-----
```

instruction: 10000000000000001100110

```
instruction: li
```

```
field:      00
```

```
immediate: 00000000000000110
```

rd: 00110

```
-----EXECUTE/WRITE BACK STAGE-----
```

```
instruction: li
```

```
field:      10
```

```
immediate:    0000000000000101
```

```
rd:      00110
```

[illegible]

```
write_en = 1
```

Cycle 31

```
-----INSTRUCTION FETCH STAGE-----
```

instruction: 011000110001100011000010

```
-----INSTRUCTION DECODE STAGE-----
```

instruction: 010000110001100011000010

instruction: MA low

[illegible][illegible][illegible][illegible]

-----EXECUTE/WRITE BACK STAGE-----

```
instruction: li
```

```
field:      00
```

```
immediate:    0000000000000110
```

rd: 00110

results.txt

```
alu_out      = 000000000000000000000000000000101000000000000000000000000000110
write_en     = 1
```

Cycle 32

```
-----INSTRUCTION FETCH STAGE-----
```

```
instruction: 1011111111111111111001111
```

```
-----INSTRUCTION DECODE STAGE-----
```

instruction: 011000110001100011000010

instruction: MS low

[illegible][illegible][illegible][illegible]

```
-----EXECUTE/WRITE BACK STAGE-----
```

instruction: MA low

[illegible][illegible][illegible][illegible][illegible]

```
write_en    = 1
```

Cycle 33

```
-----INSTRUCTION FETCH STAGE-----
```

```
instruction: 000000001000000111101100
```

```
-----INSTRUCTION DECODE STAGE-----
```

```
instruction: 10111111111111111111001111
```

```
instruction: li
```

field: 01

```
immediate: 1111111111111110
```

```
rd:      01111
```

```
-----EXECUTE/WRITE BACK STAGE-----
```

instruction: MS low

[illegible]

