Pipelined Processor

Project 3

Chenkai Shao

Jeongsoo Kim

Approach Description

We implemented the pipelined processor by dividing the single cycle data-path into five stages and adding registers between the stages. We used the provided single-cycle processor as our framework to implement the 5 stage pipeline processor. We basically followed what our professor recommended us to implement it. Since we worked on the singe-cycle processor that we did not create, we first tried to understand implementations on the template. Then we discussed our overall implementation for 5 stage pipeline processor such as stored values for each register. After we spend about 2 days to discuss about basic sketches of our implementation, we started implementing.

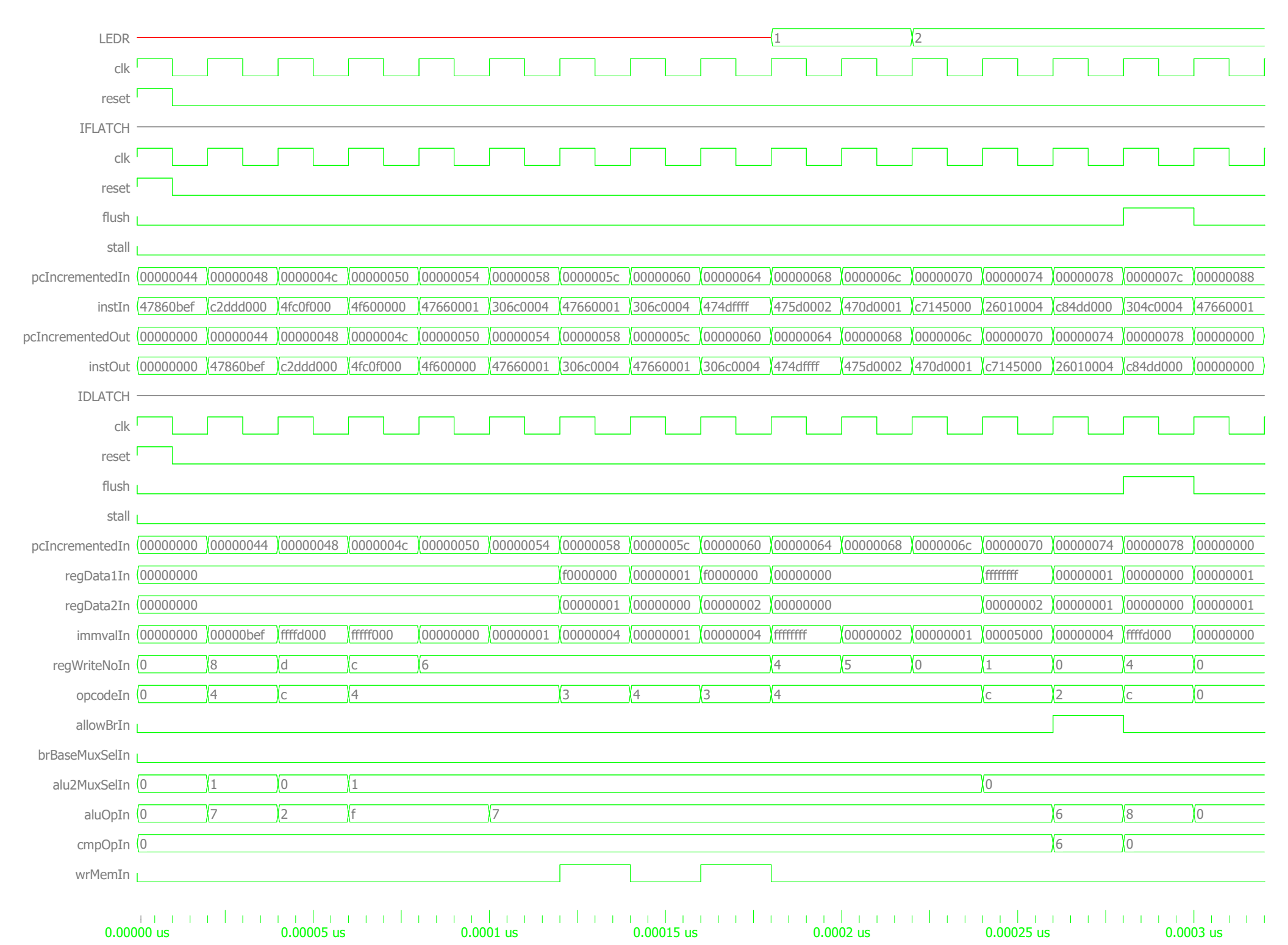
Problems Encountered

When we started debugging, we encountered several small syntax errors. However, those were pretty easy to fix it. The part that we encountered most problems was forwarding part. The first problem that we encountered was that we missed checking a proper condition for stalling the pipelines. When an opcode in MEM stage is not LW, we should not forward an output from memory. We discussed about it during our discussion, but we forgot to implement it. So, we spent a little while to figure it out. The second problem that we encountered was that we accidently flushed if-latch, when our pipeline was stalled. When we realized that the condition was incorrect. We simply changed to stalling if-latch and flushing ID-latch, when any stalling occurred. After we fixed it, we have the fully functioning 5 stage pipeline!

Contribution

Jeongsoo Kim: Data-path and Latches

Simulation Waveforms



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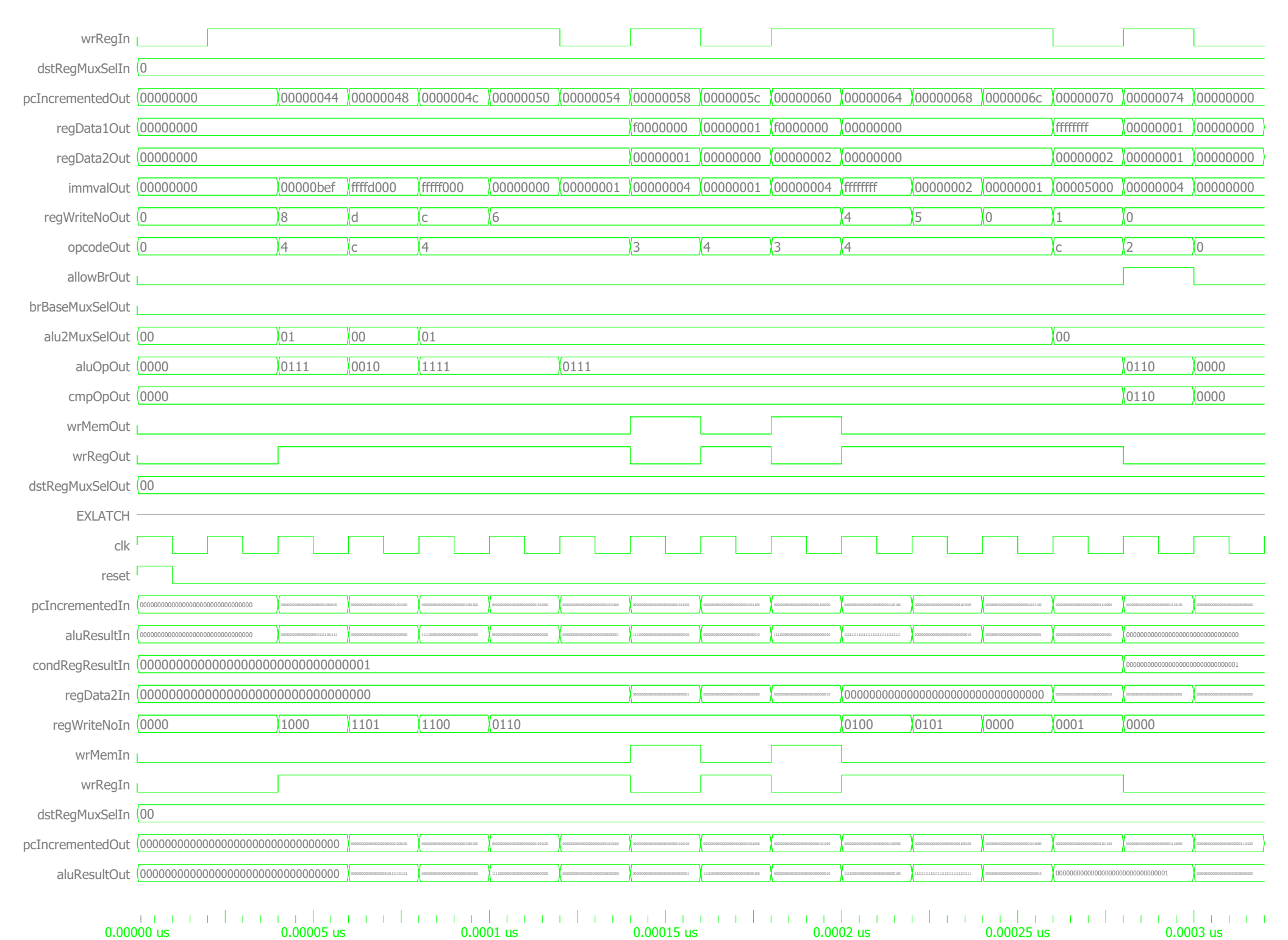

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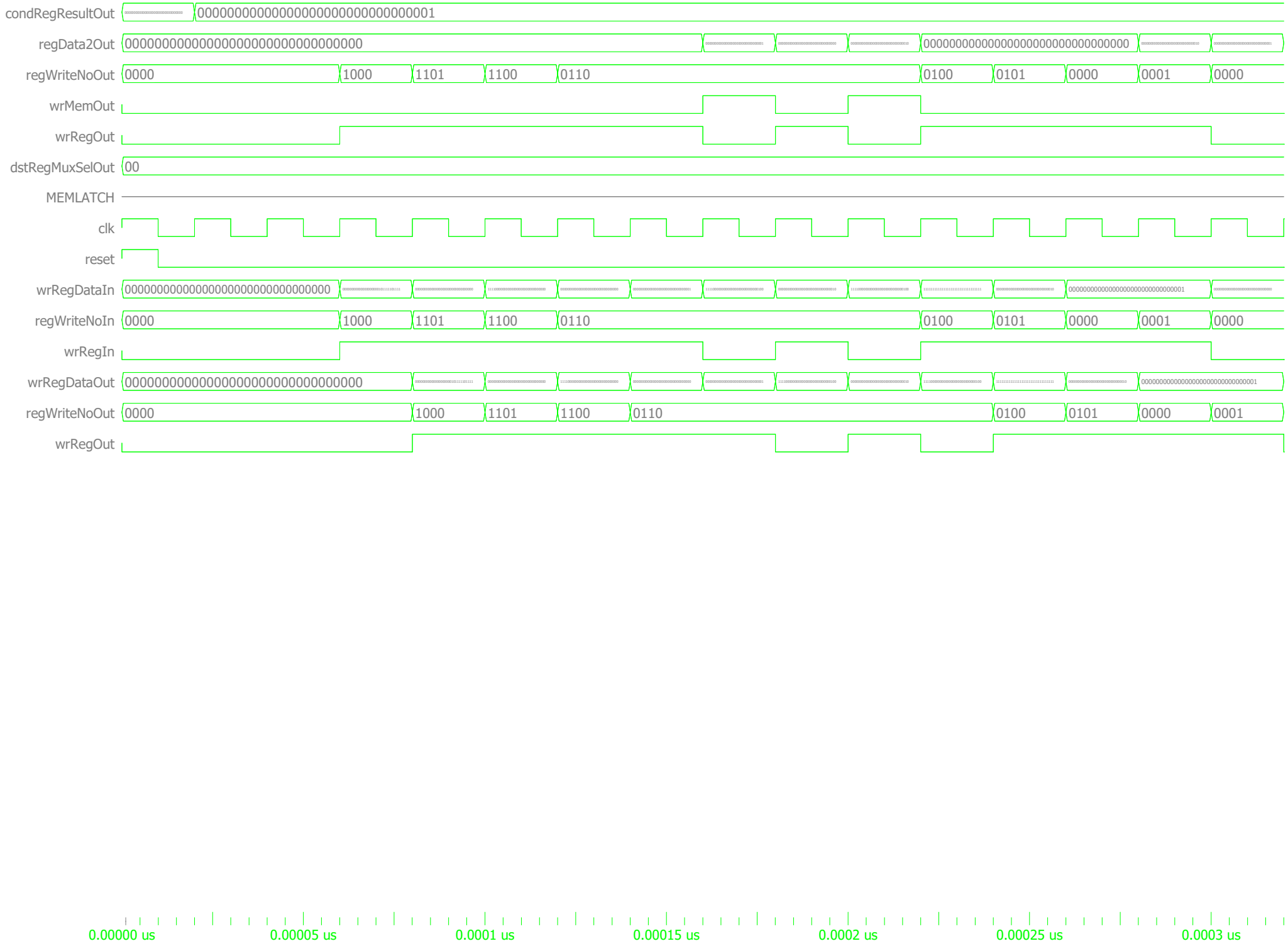
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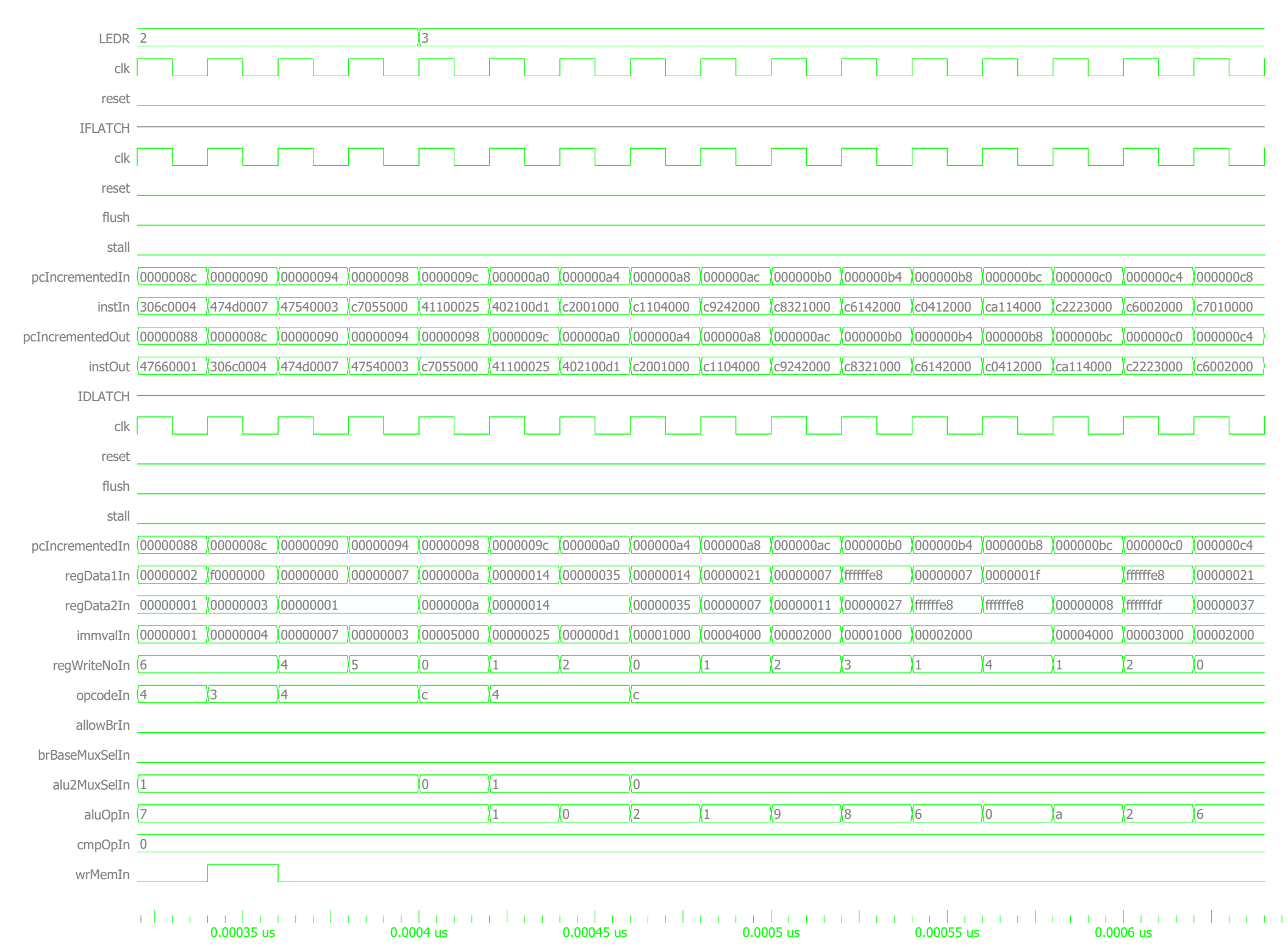
regData2Out
00000000000000000000000000000000
00000000000000000000000000000000
regWriteNoOut
0000
1000
1101
1100
0110
0100
0101
0000
0001
0000
wrMemOut
wrRegOut
dstRegMuxSelOut
00
MEMLATCH
clk
reset
wrRegDataIn
00000000000000000000000000000000
00000000000000000000000000000001
regWriteNoIn
0000
1000
1101
1100
0110
0100
0101
0000
0001
0000
wrRegIn
wrRegDataOut
00000000000000000000000000000000
00000000000000000000000000000001
regWriteNoOut
0000
1000
1101
1100
0110
0100
0101
0000
0001
wrRegOut
0.00000 us
0.00005 us
0.0001 us
0.00015 us
0.0002 us
0.00025 us
0.0003 us



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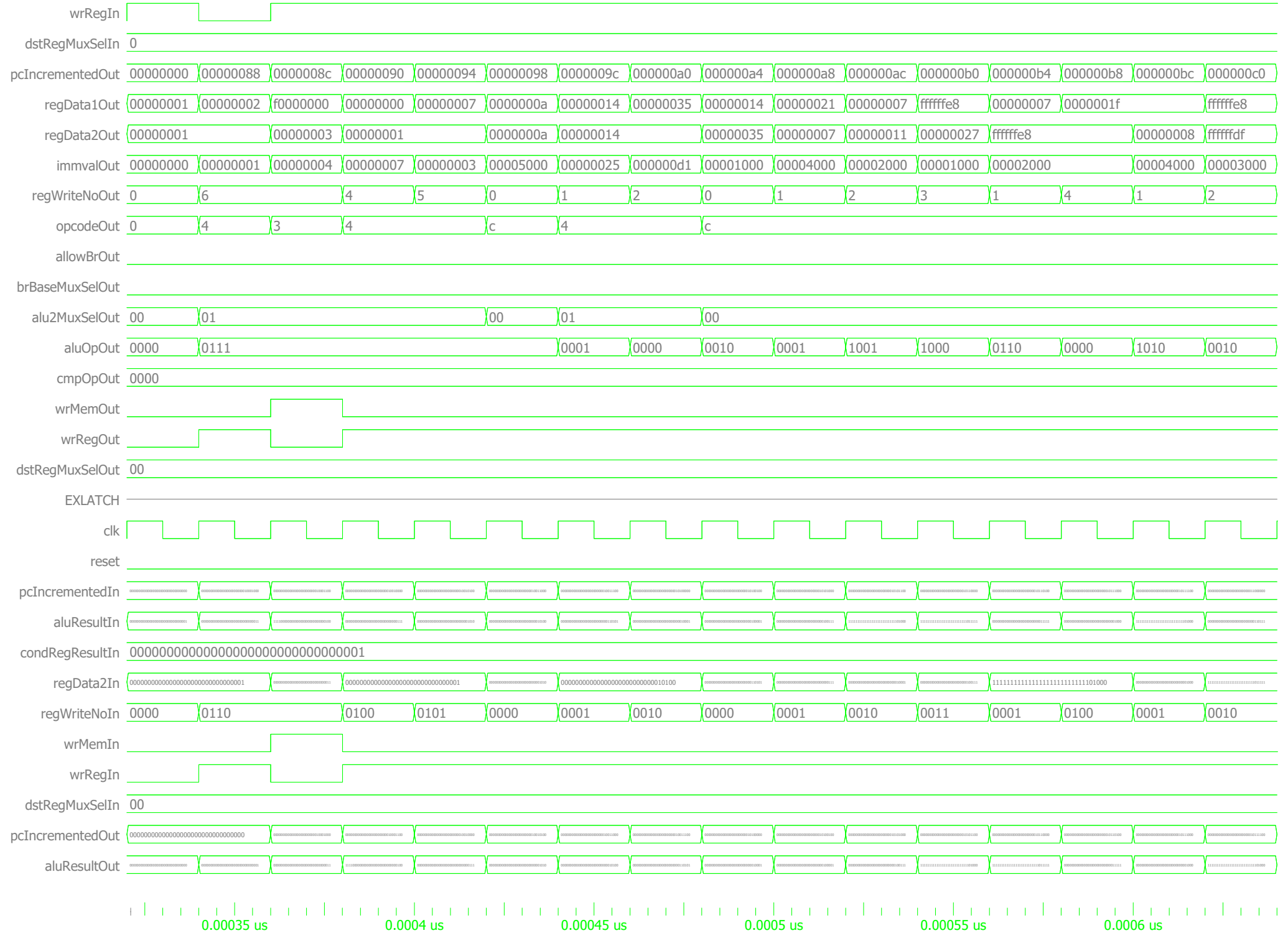

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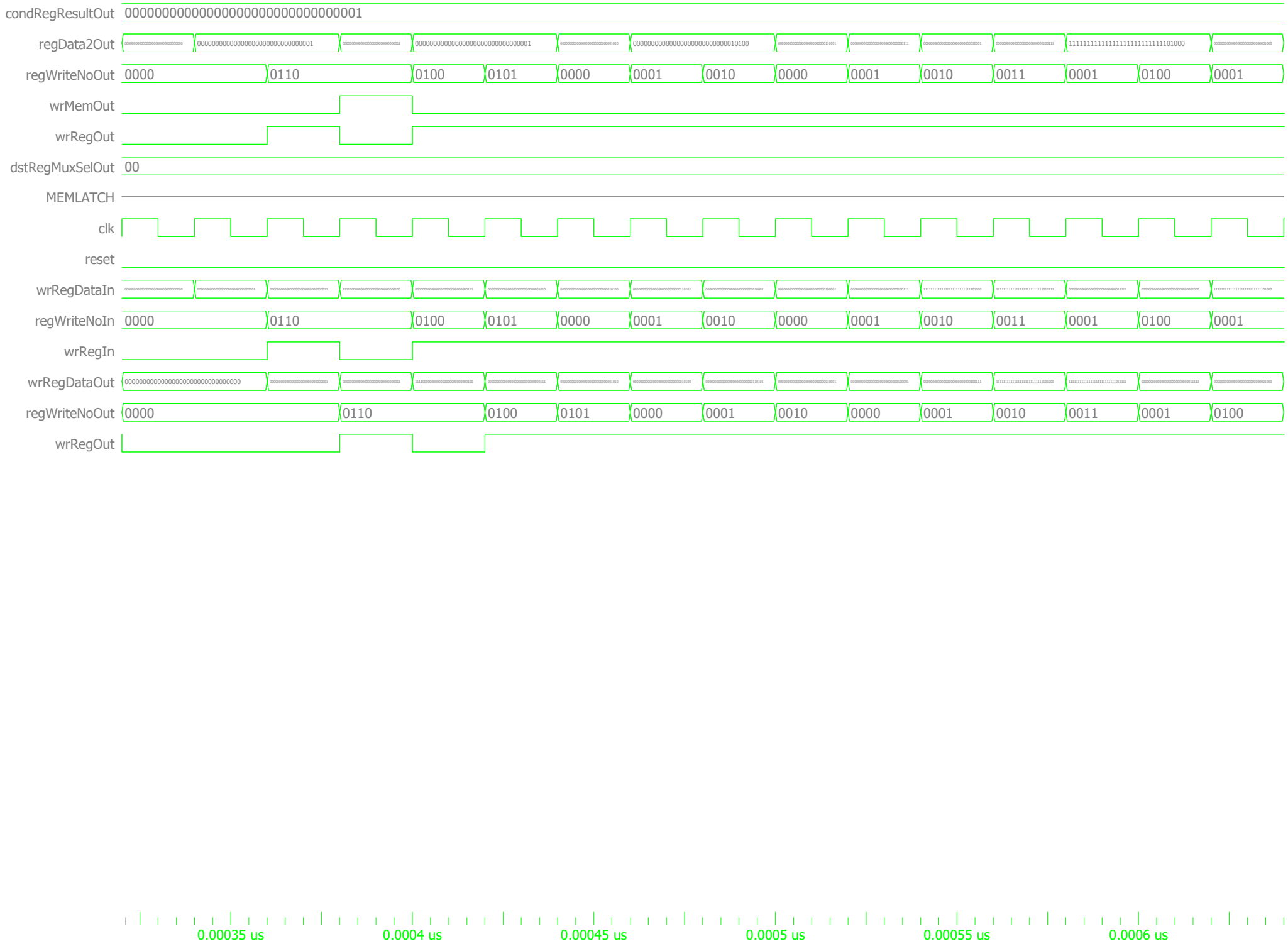
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regData2Out
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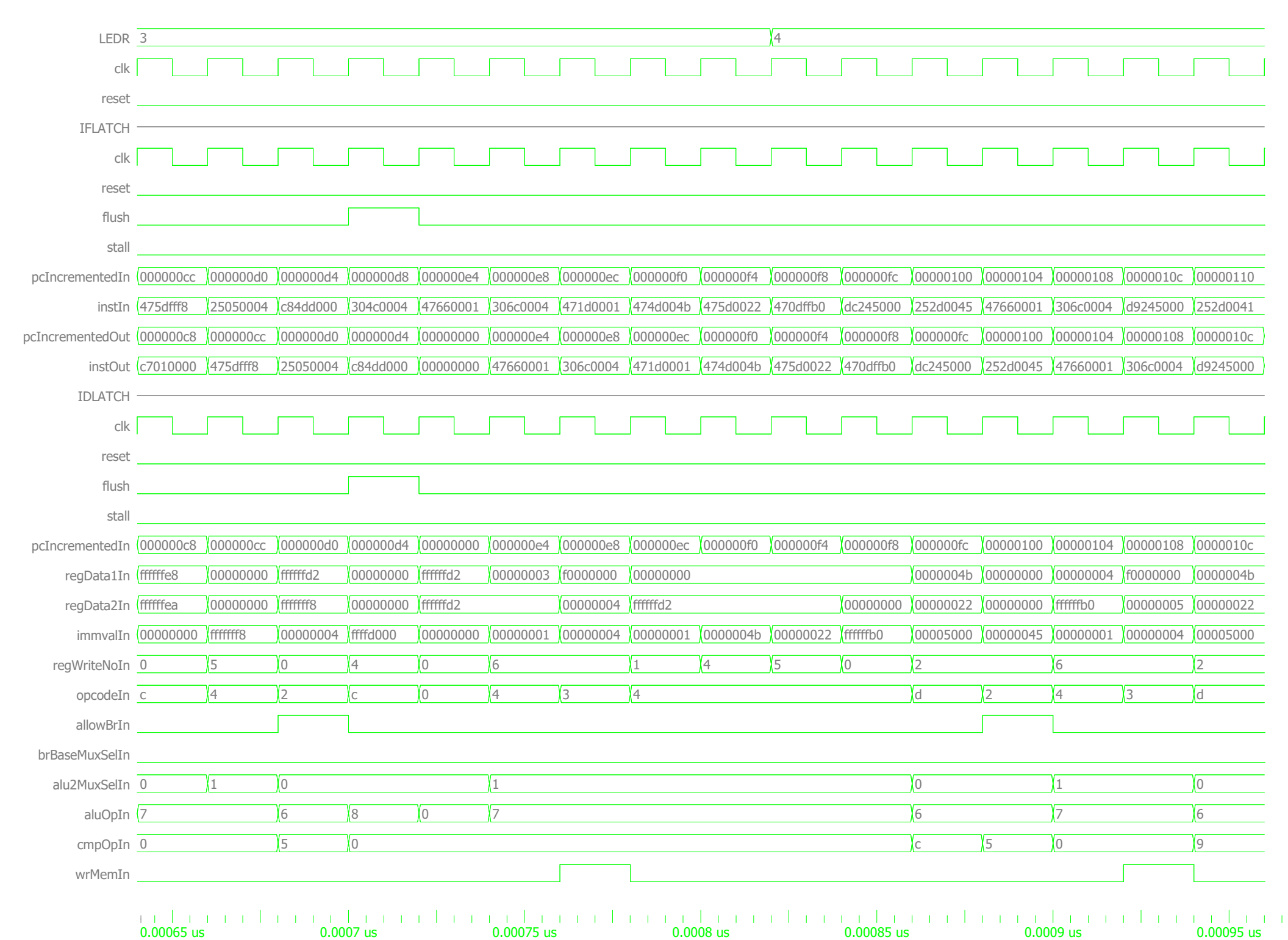
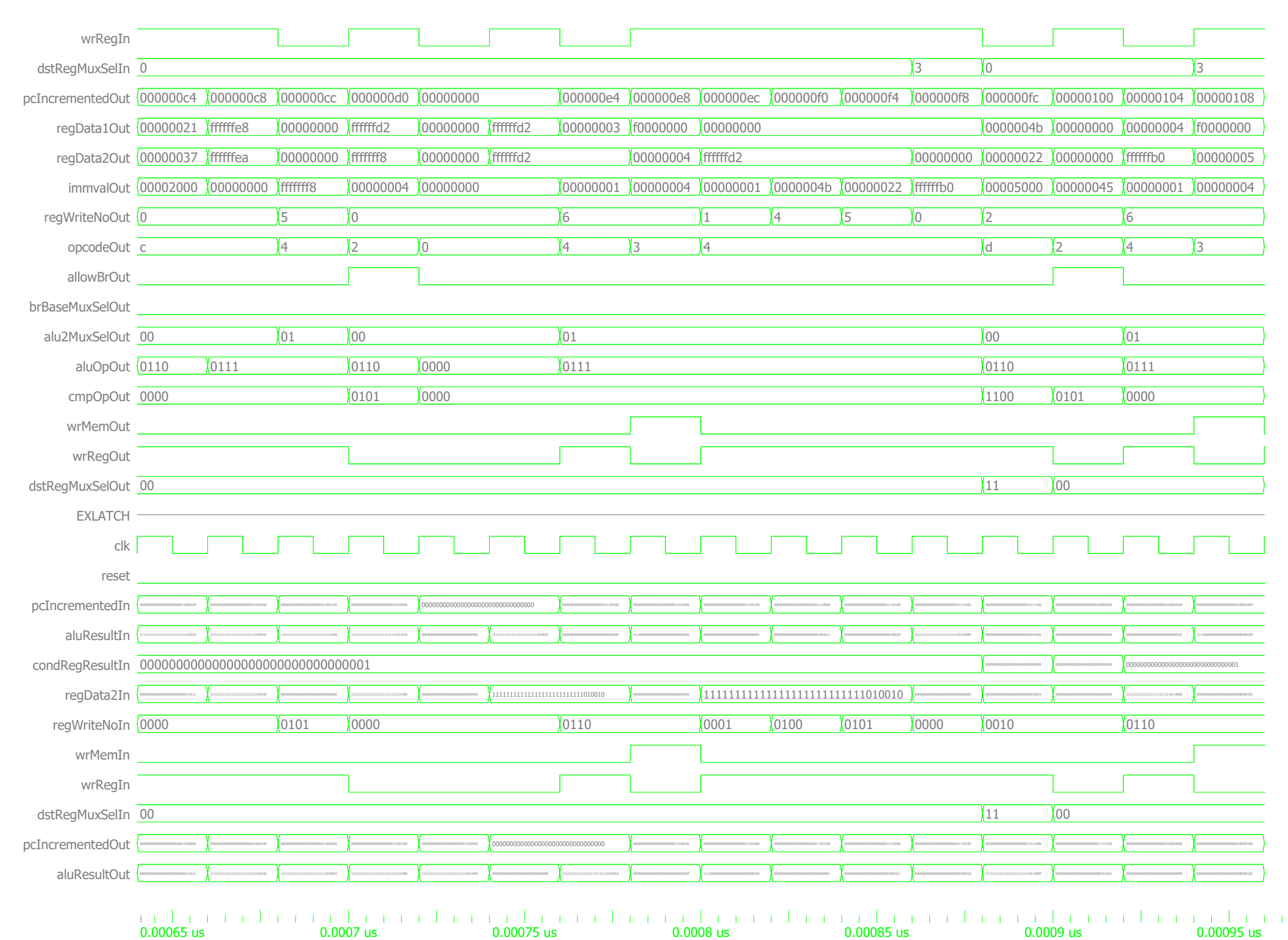
0110
0100
0101
0000
0001
0010
0000
0001
0010
0011
0001
0100
0001
wrMemOut
wrRegOut
dstRegMuxSelOut
00
MEMLATCH
clk
reset
wrRegDataIn
regWriteNoIn
0000
0110
0100
0101
0000
0001
0010
0000
0001
0010
0011
0001
0100
0001
wrRegIn
wrRegDataOut
00000000000000000000000000000000
regWriteNoOut
0000
0110
0100
0101
0000
0001
0010
0000
0001
0010
0011
0001
0100
wrRegOut
0.00035 us
0.0004 us
0.00045 us
0.0005 us
0.00055 us
0.0006 us


LEDR 3 4
clk
reset
IFLATCH
clk
reset
flush
stall
pcIncrementedIn 000000cc 000000d0 000000d4 000000d8 000000e4 000000e8 000000ec 000000f0 000000f4 000000f8 000000fc 00000100 00000104 00000108 0000010c 00000110
instIn 475dfff8 25050004 c84dd000 304c0004 47660001 306c0004 471d0001 474d004b 475d0022 470dffb0 dc245000 252d0045 47660001 306c0004 d9245000 252d0041
pcIncrementedOut 000000c8 000000cc 000000d0 000000d4 00000000 000000e4 000000e8 000000ec 000000f0 000000f4 000000f8 000000fc 00000100 00000104 00000108 0000010c
instOut c7010000 475dfff8 25050004 c84dd000 00000000 47660001 306c0004 471d0001 474d004b 475d0022 470dffb0 dc245000 252d0045 47660001 306c0004 d9245000
IDLATCH
clk
reset
flush
stall
pcIncrementedIn 000000c8 000000cc 000000d0 000000d4 00000000 000000e4 000000e8 000000ec 000000f0 000000f4 000000f8 000000fc 00000100 00000104 00000108 0000010c
regData1In fffffffe8 00000000 fffffffd2 00000000 fffffffd2 00000003 f0000000 00000000 0000004b 00000000 00000004 f0000000 0000004b
regData2In fffffffea 00000000 fffffffff8 00000000 fffffffd2 00000004 fffffffd2 00000000 00000022 00000000 fffffffb0 00000005 00000022
immvalIn 00000000 fffffffff8 00000004 ffffd000 00000000 00000001 00000004 00000001 0000004b 00000022 fffffffb0 00005000 00000045 00000001 00000004 00005000
regWriteNoIn 0 5 0 4 0 6 1 4 5 0 2 6 2
opcodeIn c 4 2 c 0 4 3 4 d 2 4 3 d
allowBrIn
brBaseMuxSelIn
alu2MuxSelIn 0 1 0 1 0 1 0
aluOpIn 7 6 8 0 7 6 7 6
cmpOpIn 0 5 0 c 5 0 9
wrMemIn
0.00065 us 0.0007 us 0.00075 us 0.0008 us 0.00085 us 0.0009 us 0.00095 us



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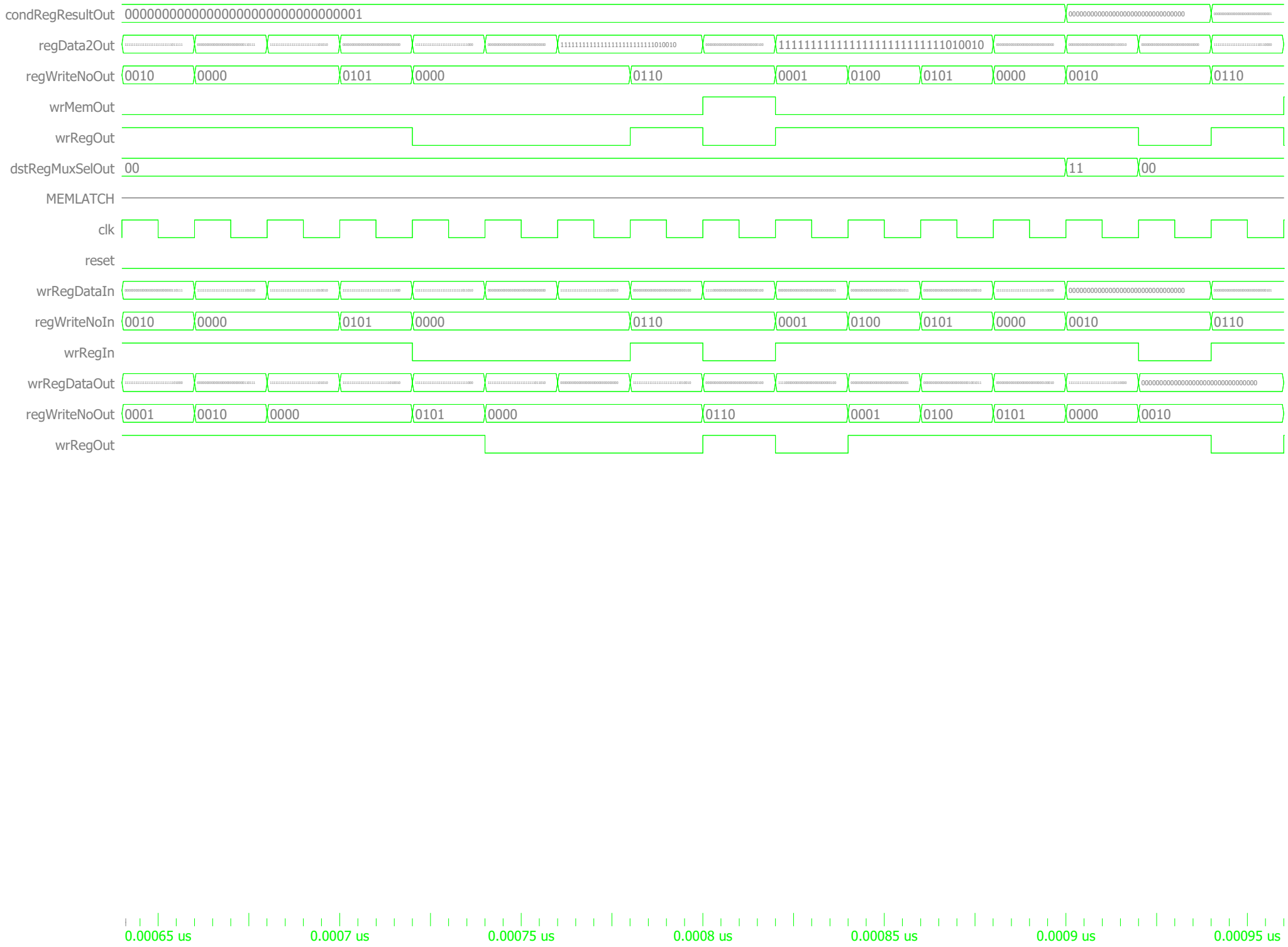
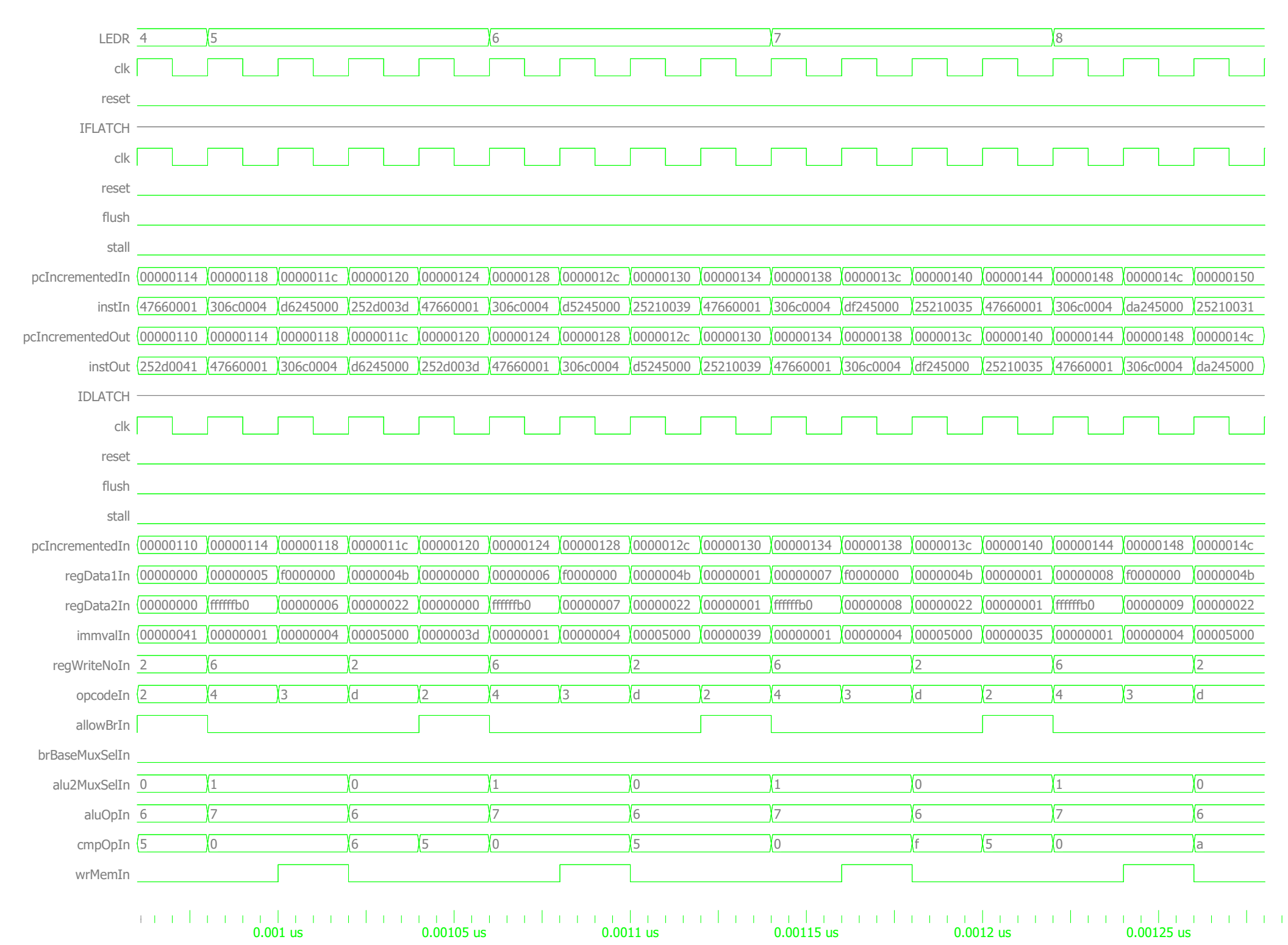
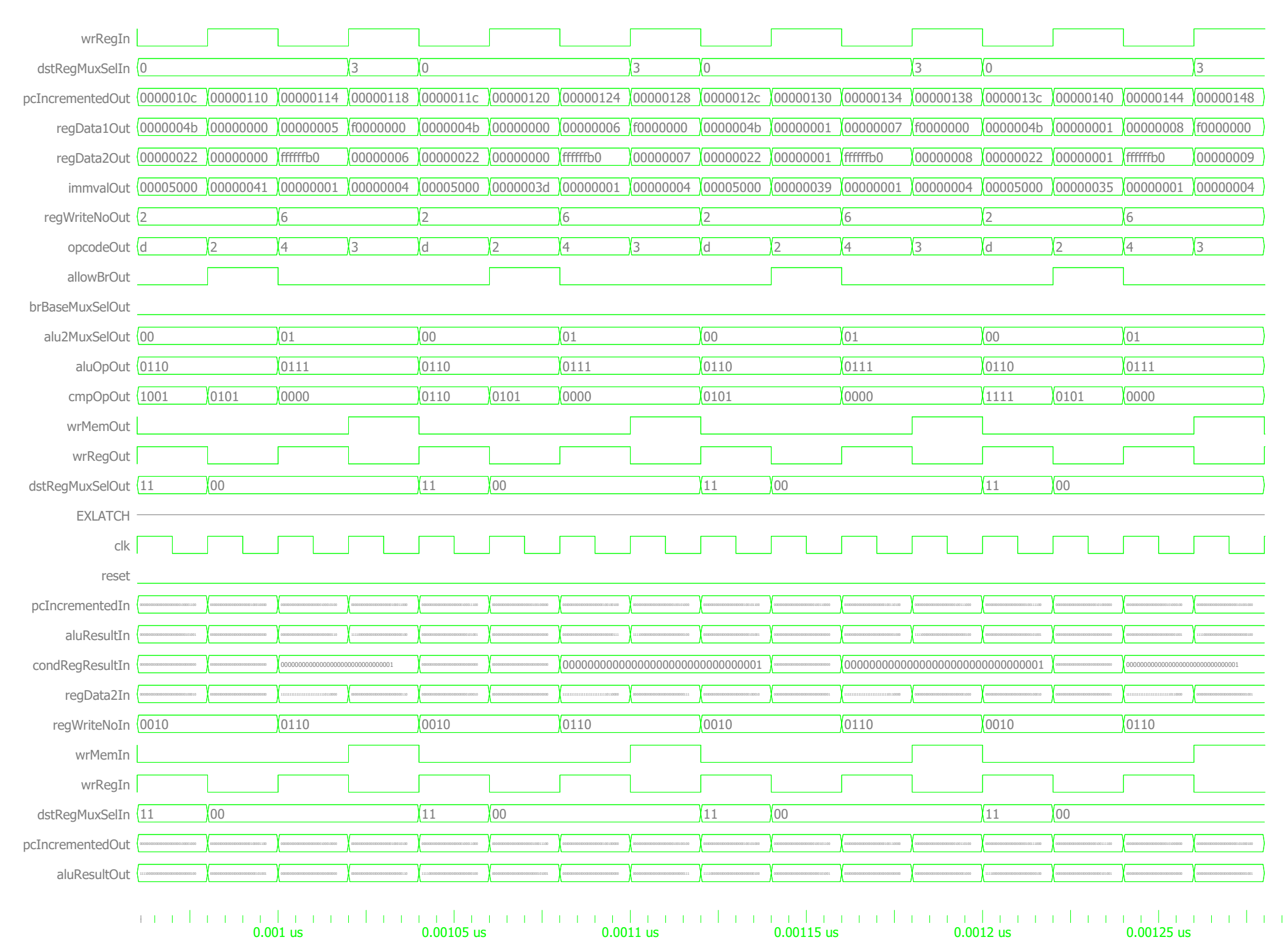

condRegResultOut
00000000000000000000000000000001
regData2Out
1111111111111111111111111010010
11111111111111111111111111010010
regWriteNoOut
0010
0000
0101
0000
0110
0001
0100
0101
0000
0010
0110
wrMemOut
wrRegOut
dstRegMuxSelOut
00
11
00
MEMLATCH
clk
reset
wrRegDataIn
00000000000000000000000000000000
regWriteNoIn
0010
0000
0101
0000
0110
0001
0100
0101
0000
0010
0110
wrRegIn
wrRegDataOut
00000000000000000000000000000000
regWriteNoOut
0001
0010
0000
0101
0000
0110
0001
0100
0101
0000
0010
wrRegOut
0.00065 us
0.0007 us
0.00075 us
0.0008 us
0.00085 us
0.0009 us
0.00095 us


LEDR 4 5 6 7 8
clk
reset
IFLATCH
clk
reset
flush
stall
pcIncrementedIn 00000114 00000118 0000011c 00000120 00000124 00000128 0000012c 00000130 00000134 00000138 0000013c 00000140 00000144 00000148 0000014c 00000150
instIn 47660001 306c0004 d6245000 252d003d 47660001 306c0004 d5245000 25210039 47660001 306c0004 df245000 25210035 47660001 306c0004 da245000 25210031
pcIncrementedOut 00000110 00000114 00000118 0000011c 00000120 00000124 00000128 0000012c 00000130 00000134 00000138 0000013c 00000140 00000144 00000148 0000014c
instOut 252d0041 47660001 306c0004 d6245000 252d003d 47660001 306c0004 d5245000 25210039 47660001 306c0004 df245000 25210035 47660001 306c0004 da245000
IDLATCH
clk
reset
flush
stall
pcIncrementedIn 00000110 00000114 00000118 0000011c 00000120 00000124 00000128 0000012c 00000130 00000134 00000138 0000013c 00000140 00000144 00000148 0000014c
regData1In 00000000 00000005 f0000000 0000004b 00000000 00000006 f0000000 0000004b 00000001 00000007 f0000000 0000004b 00000001 00000008 f0000000 0000004b
regData2In 00000000 fffffffb0 00000006 00000022 00000000 fffffffb0 00000007 00000022 00000001 fffffffb0 00000008 00000022 00000001 fffffffb0 00000009 00000022
immvalIn 00000041 00000001 00000004 00005000 0000003d 00000001 00000004 00005000 00000039 00000001 00000004 00005000 00000035 00000001 00000004 00005000
regWriteNoIn 2 6 2 6 2 6 2 6 2
opcodeIn 2 4 3 d 2 4 3 d 2 4 3 d 2 4 3 d
allowBrIn
brBaseMuxSelIn
alu2MuxSelIn 0 1 0 1 0 1 0 1 0
aluOpIn 6 7 6 7 6 7 6 7 6
cmpOpIn 5 0 6 5 0 5 0 f 5 0 a
wrMemIn
0.001 us
0.00105 us
0.0011 us
0.00115 us
0.0012 us
0.00125 us



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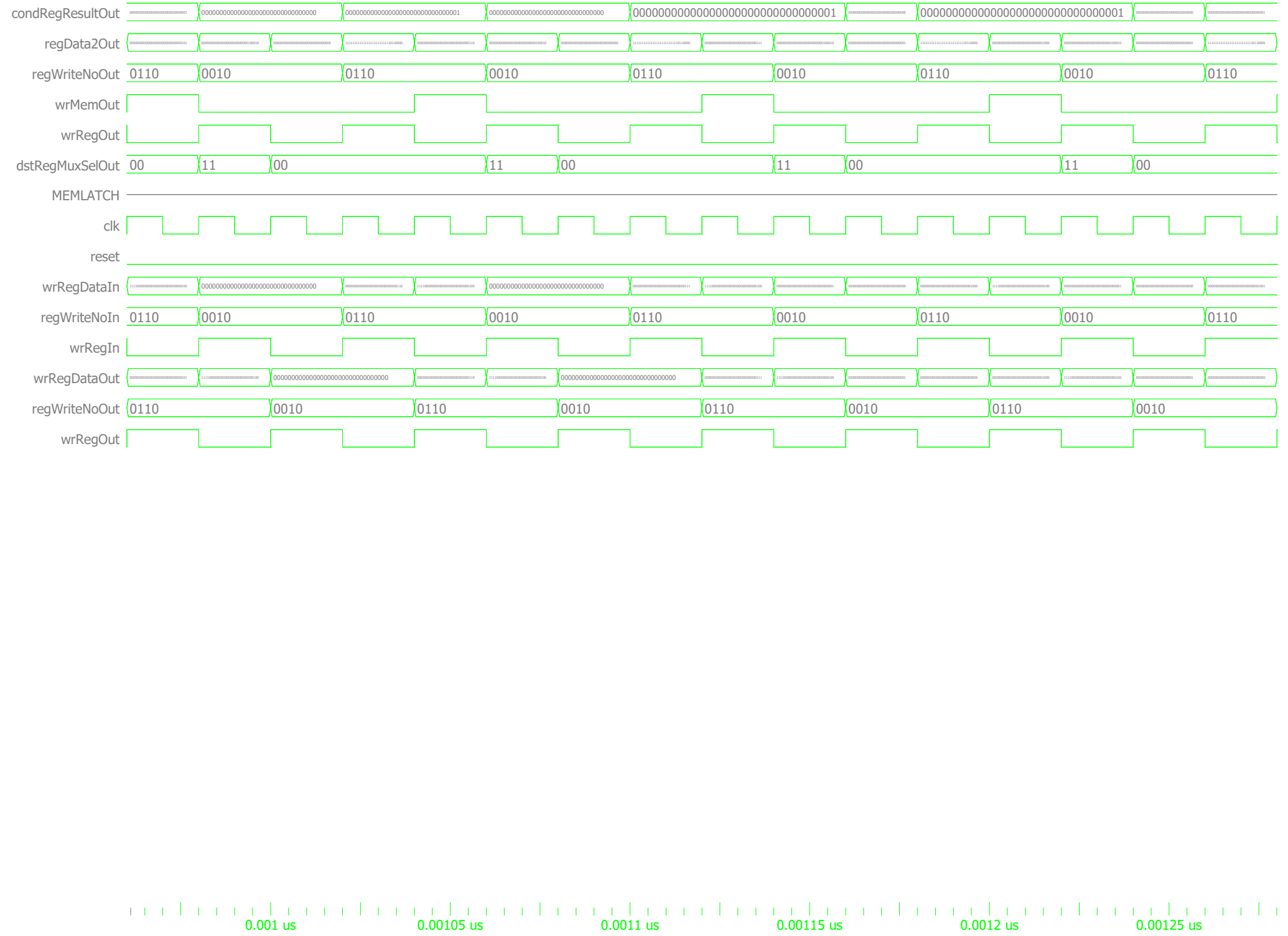
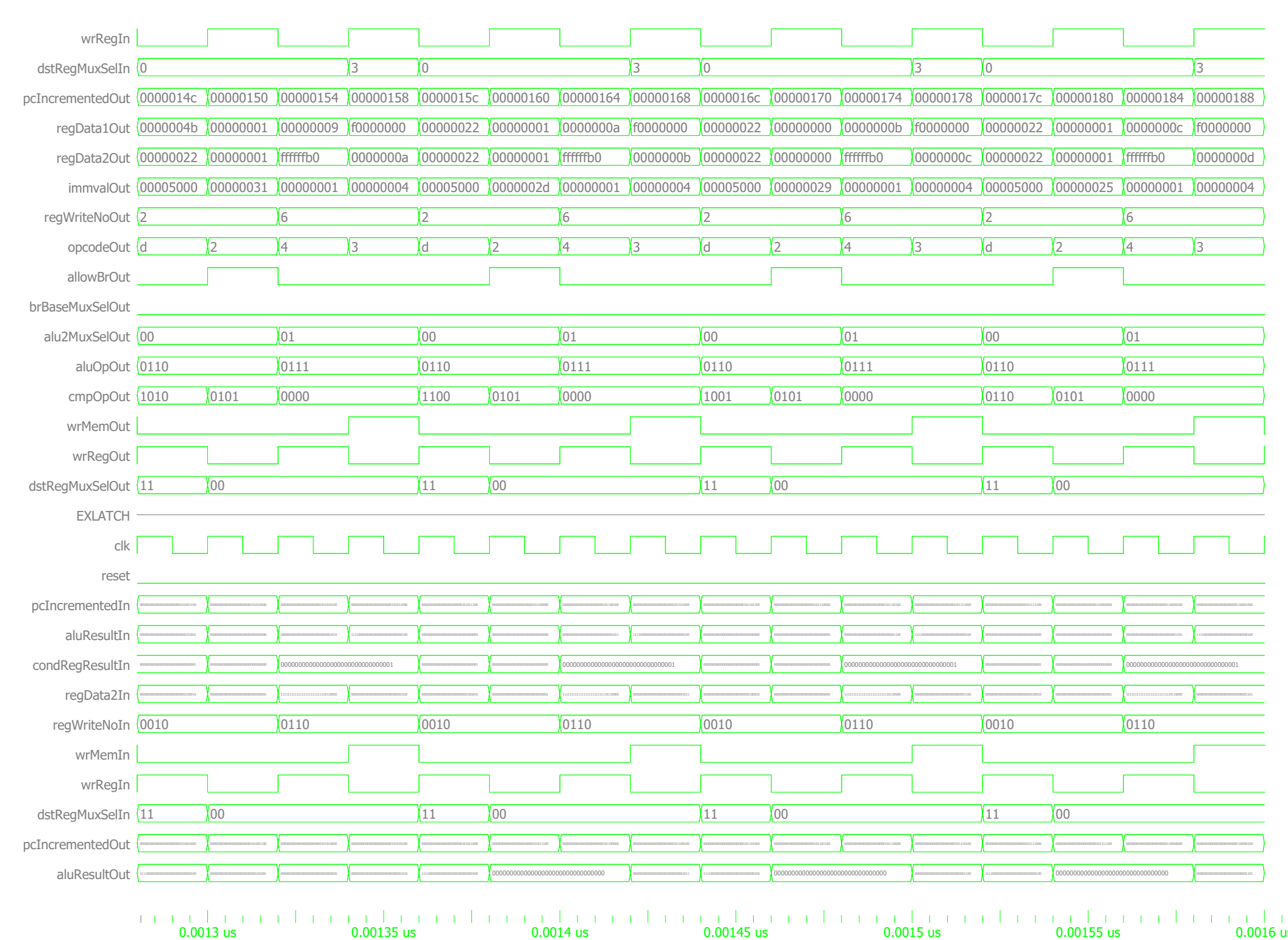

condRegResultOut
regData2Out
regWriteNoOut
0110
0010
0110
0010
0110
0010
0110
0010
0110
wrMemOut
wrRegOut
dstRegMuxSelOut
00
11
00
11
00
11
00
11
00
MEMLATCH
clk
reset
wrRegDataIn
regWriteNoIn
0110
0010
0110
0010
0110
0010
0110
0010
0110
wrRegIn
wrRegDataOut
regWriteNoOut
0110
0010
0110
0010
0110
0010
0110
0010
wrRegOut
0.001 us
0.00105 us
0.0011 us
0.00115 us
0.0012 us
0.00125 us


LEDR 8 9 10 11 12
clk
reset
IFLATCH
clk
reset
flush
stall
pcIncrementedIn 00000154 00000158 0000015c 00000160 00000164 00000168 0000016c 00000170 00000174 00000178 0000017c 00000180 00000184 00000188 0000018c 00000190
instIn 47660001 306c0004 dc255000 2521002d 47660001 306c0004 d9255000 252d0029 47660001 306c0004 d6255000 25210025 47660001 306c0004 d5255000 252d0021
pcIncrementedOut 00000150 00000154 00000158 0000015c 00000160 00000164 00000168 0000016c 00000170 00000174 00000178 0000017c 00000180 00000184 00000188 0000018c
instOut 25210031 47660001 306c0004 dc255000 2521002d 47660001 306c0004 d9255000 252d0029 47660001 306c0004 d6255000 25210025 47660001 306c0004 d5255000
IDLATCH
clk
reset
flush
stall
pcIncrementedIn 00000150 00000154 00000158 0000015c 00000160 00000164 00000168 0000016c 00000170 00000174 00000178 0000017c 00000180 00000184 00000188 0000018c
regData1In 00000001 00000009 f0000000 00000022 00000001 0000000a f0000000 00000022 00000000 0000000b f0000000 00000022 00000001 0000000c f0000000 00000022
regData2In 00000001 fffffffb0 0000000a 00000022 00000001 fffffffb0 0000000b 00000022 00000000 fffffffb0 0000000c 00000022 00000001 fffffffb0 0000000d 00000022
immvalIn 00000031 00000001 00000004 00005000 0000002d 00000001 00000004 00005000 00000029 00000001 00000004 00005000 00000025 00000001 00000004 00005000
regWriteNoIn 2 6 2 6 2 6 2 6 2
opcodeIn 2 4 3 d 2 4 3 d 2 4 3 d 2 4 3 d
allowBrIn
brBaseMuxSelIn
alu2MuxSelIn 0 1 0 1 0 1 0 1 0
aluOpIn 6 7 6 7 6 7 6 7 6
cmpOpIn 5 0 c 5 0 9 5 0 6 5 0 5
wrMemIn
0.0013 us
0.00135 us
0.0014 us
0.00145 us
0.0015 us
0.00155 us
0.0016 us



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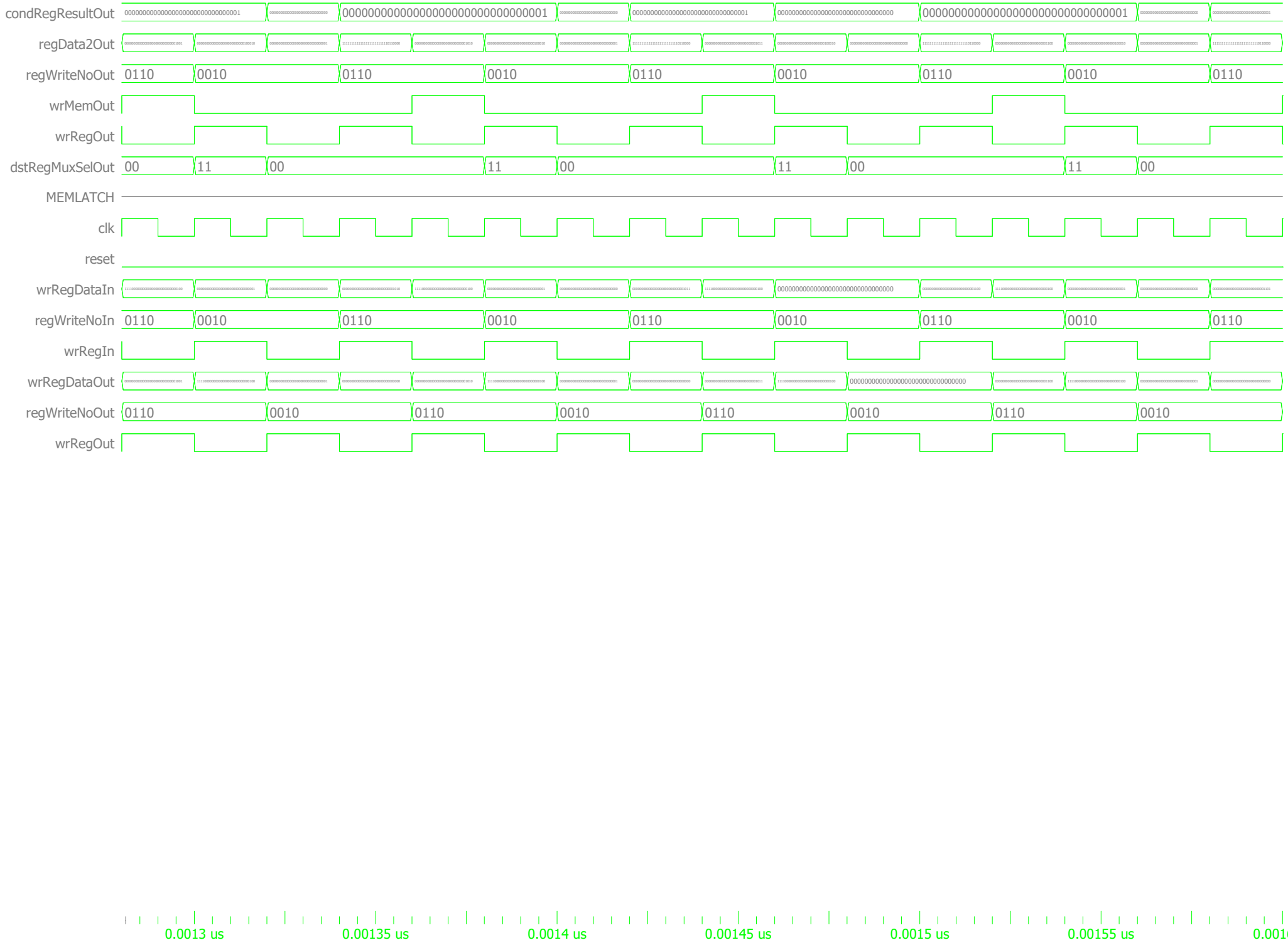
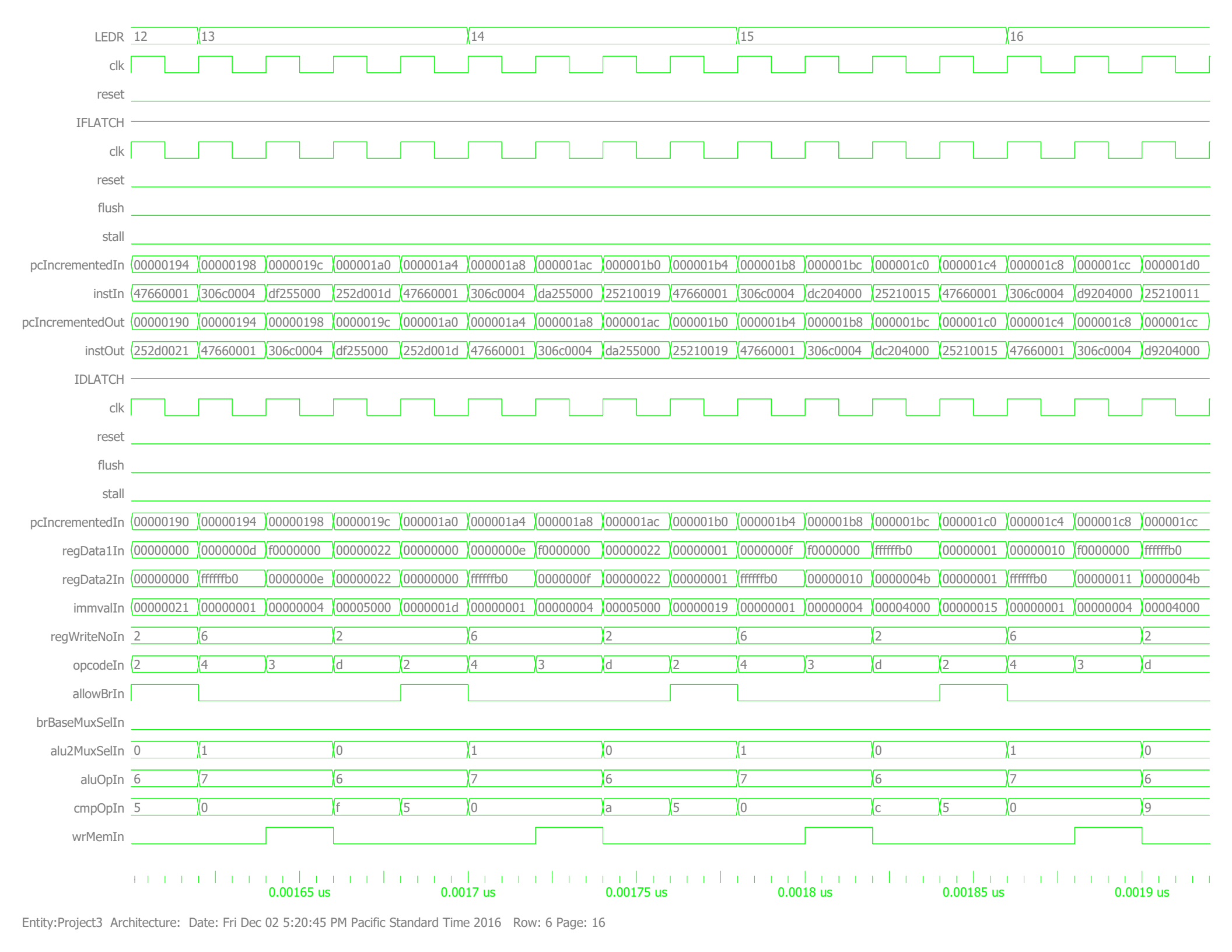
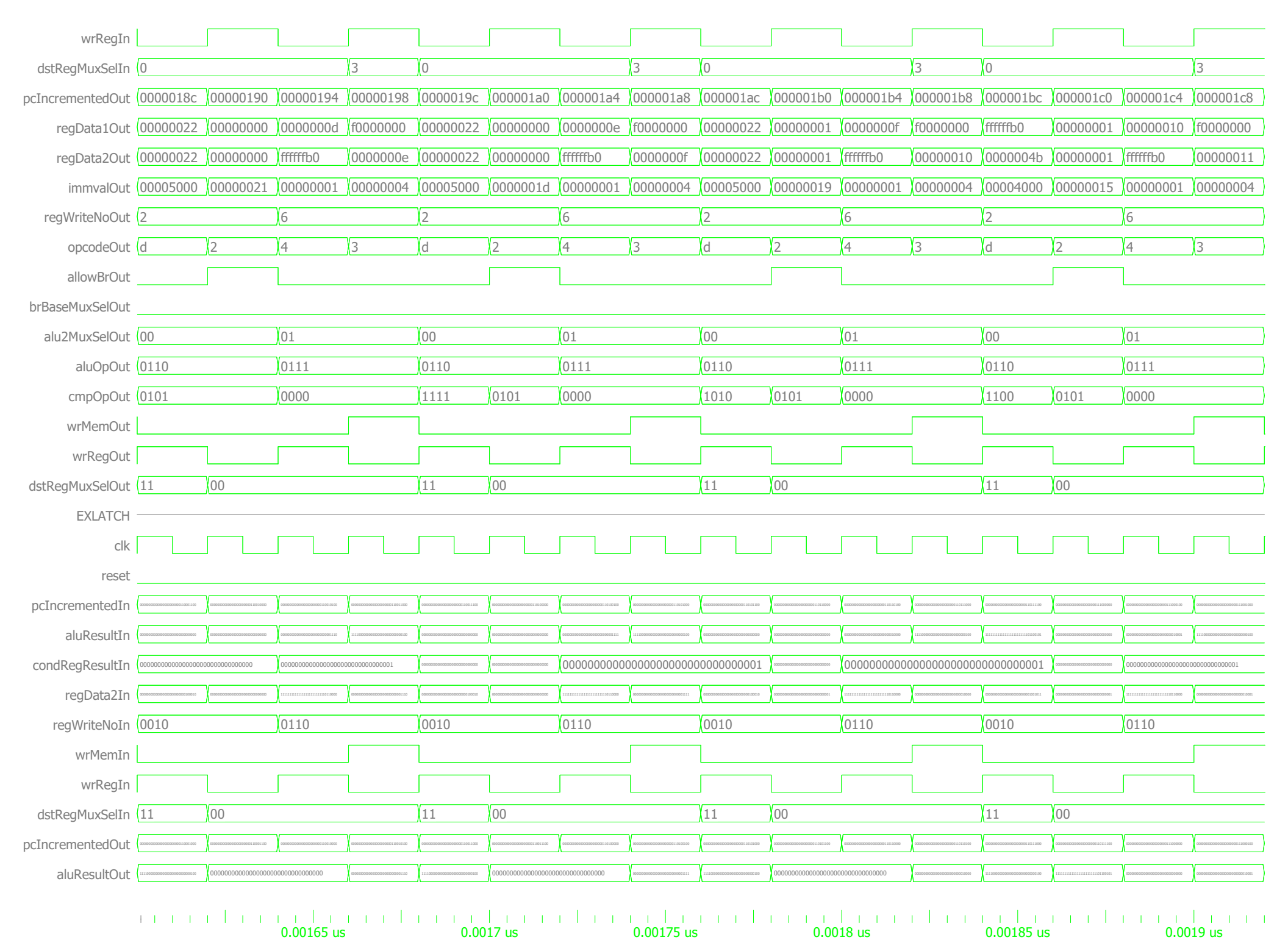
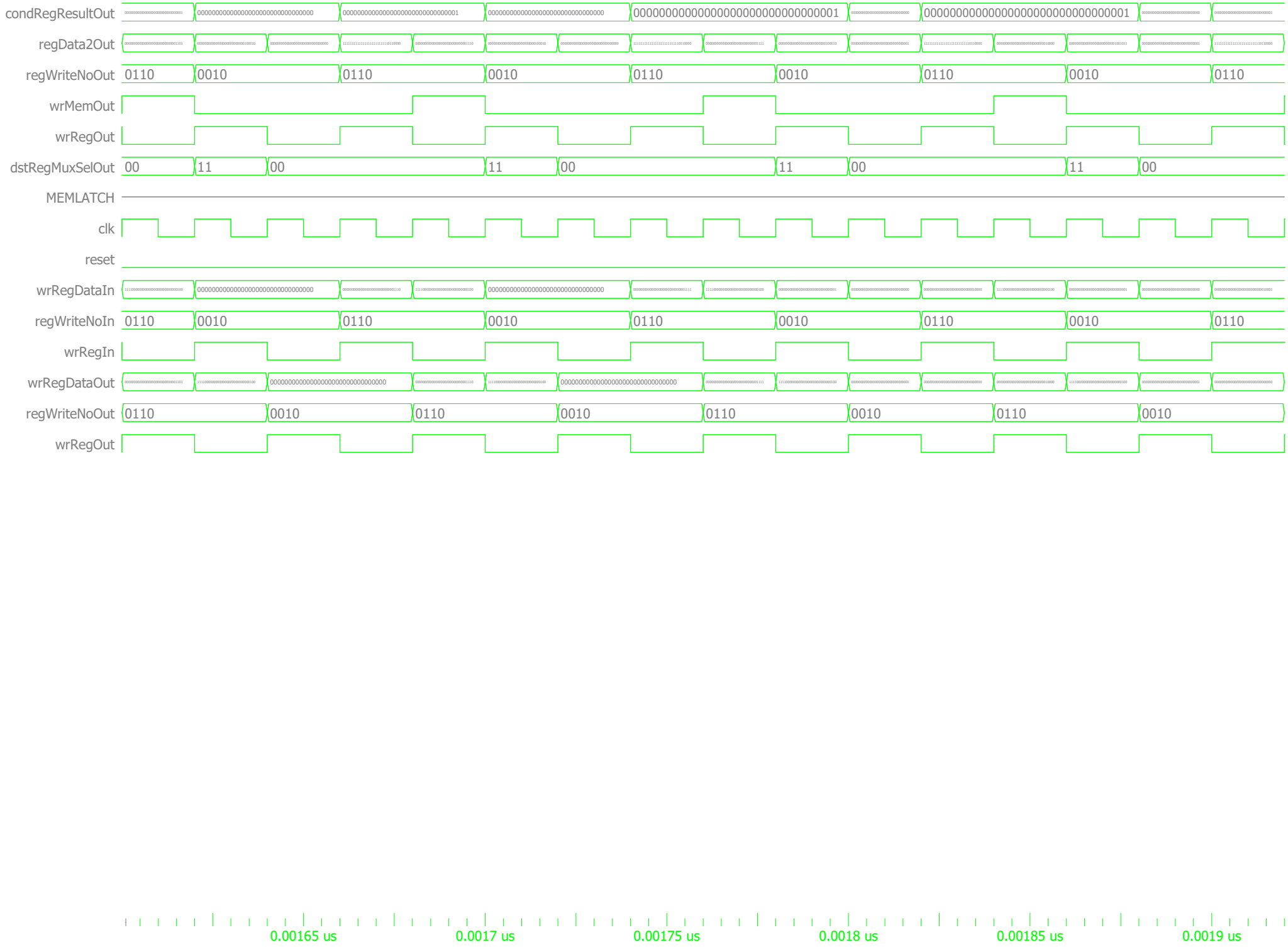
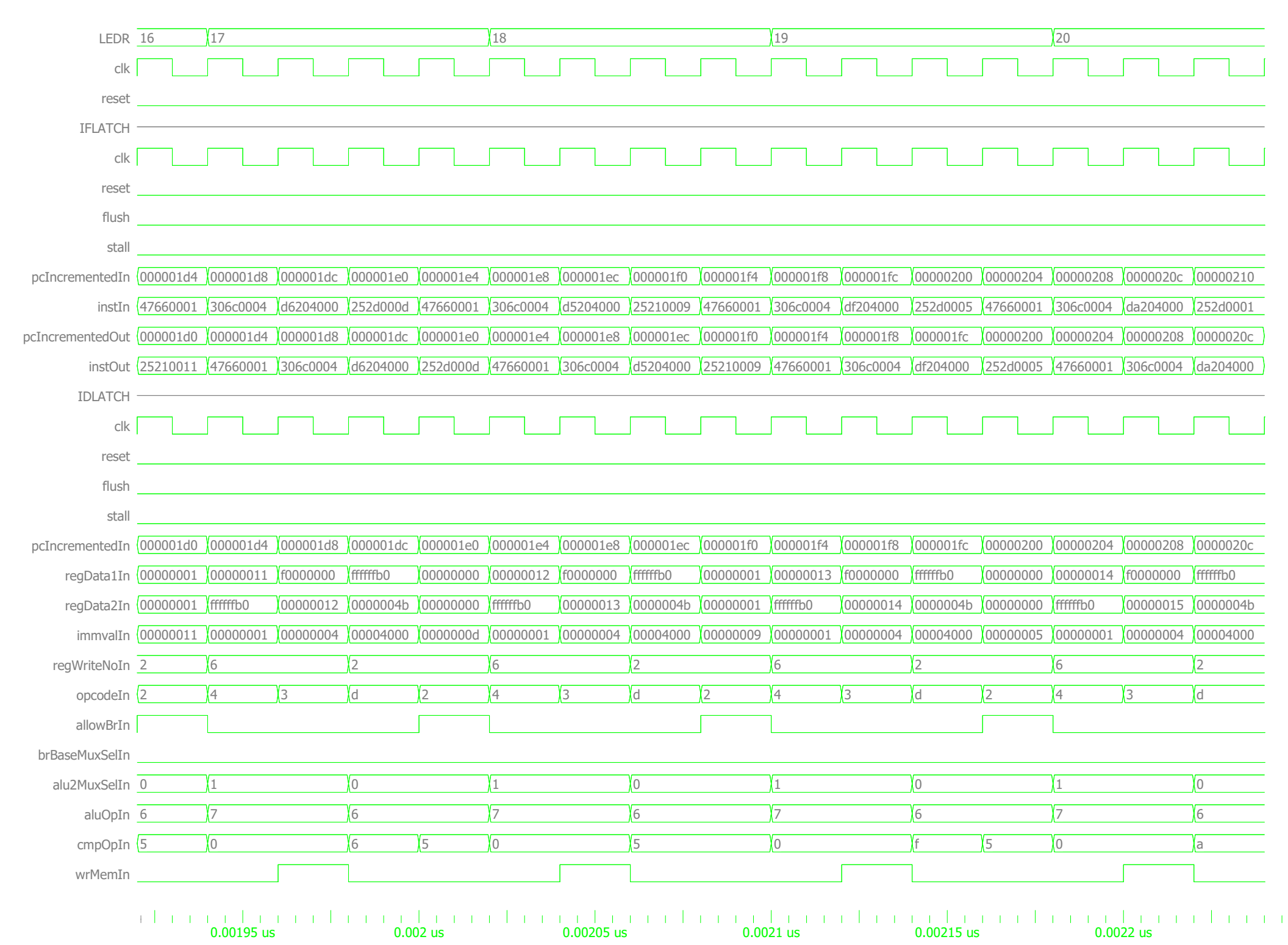

condRegResultOut
regData2Out
regWriteNoOut
0110
0010
0110
0010
0110
0010
0110
0010
0110
wrMemOut
wrRegOut
dstRegMuxSelOut
00
11
00
11
00
11
00
11
00
MEMLATCH
clk
reset
wrRegDataIn
regWriteNoIn
0110
0010
0110
0010
0110
0010
0110
0010
0110
wrRegIn
wrRegDataOut
regWriteNoOut
0110
0010
0110
0010
0110
0010
0110
0010
wrRegOut
0.0013 us
0.00135 us
0.0014 us
0.00145 us
0.0015 us
0.00155 us
0.0016 us


LEDR 12 13 14 15 16
clk
reset
IFLATCH
clk
reset
flush
stall
pcIncrementedIn 00000194 00000198 0000019c 000001a0 000001a4 000001a8 000001ac 000001b0 000001b4 000001b8 000001bc 000001c0 000001c4 000001c8 000001cc 000001d0
instIn 47660001 306c0004 df255000 252d001d 47660001 306c0004 da255000 25210019 47660001 306c0004 dc204000 25210015 47660001 306c0004 d9204000 25210011
pcIncrementedOut 00000190 00000194 00000198 0000019c 000001a0 000001a4 000001a8 000001ac 000001b0 000001b4 000001b8 000001bc 000001c0 000001c4 000001c8 000001cc
instOut 252d0021 47660001 306c0004 df255000 252d001d 47660001 306c0004 da255000 25210019 47660001 306c0004 dc204000 25210015 47660001 306c0004 d9204000
IDLATCH
clk
reset
flush
stall
pcIncrementedIn 00000190 00000194 00000198 0000019c 000001a0 000001a4 000001a8 000001ac 000001b0 000001b4 000001b8 000001bc 000001c0 000001c4 000001c8 000001cc
regData1In 00000000 0000000d f0000000 00000022 00000000 0000000e f0000000 00000022 00000001 0000000f f0000000 fffffffb0 00000001 00000010 f0000000 fffffffb0
regData2In 00000000 fffffffb0 0000000e 00000022 00000000 fffffffb0 0000000f 00000022 00000001 fffffffb0 00000010 0000004b 00000001 fffffffb0 00000011 0000004b
immvalIn 00000021 00000001 00000004 00005000 0000001d 00000001 00000004 00005000 00000019 00000001 00000004 00004000 00000015 00000001 00000004 00004000
regWriteNoIn 2 6 2 6 2 6 2 6 2
opcodeIn 2 4 3 d 2 4 3 d 2 4 3 d 2 4 3 d
allowBrIn
brBaseMuxSelIn
alu2MuxSelIn 0 1 0 1 0 1 0 1 0
aluOpIn 6 7 6 7 6 7 6 7 6
cmpOpIn 5 0 f 5 0 a 5 0 c 5 0 9
wrMemIn
0.00165 us
0.0017 us
0.00175 us
0.0018 us
0.00185 us
0.0019 us


wrRegIn
dstRegMuxSelIn
pcIncrementedOut
regData1Out
regData2Out
immvalOut
regWriteNoOut
opcodeOut
allowBrOut
brBaseMuxSelOut
alu2MuxSelOut
aluOpOut
cmpOpOut
wrMemOut
wrRegOut
dstRegMuxSelOut
EXLATCH
clk
reset
pcIncrementedIn
aluResultIn
condRegResultIn
regData2In
regWriteNoIn
wrMemIn
wrRegIn
dstRegMuxSelIn
pcIncrementedOut
aluResultOut
0.00165 us
0.0017 us
0.00175 us
0.0018 us
0.00185 us
0.0019 us


condRegResultOut
regData2Out
regWriteNoOut
0110
0010
0110
0010
0110
0010
0110
0010
0110
wrMemOut
wrRegOut
dstRegMuxSelOut
00
11
00
11
00
11
00
11
00
MEMLATCH
clk
reset
wrRegDataIn
regWriteNoIn
0110
0010
0110
0010
0110
0010
0110
0010
0110
wrRegIn
wrRegDataOut
regWriteNoOut
0110
0010
0110
0010
0110
0010
0110
0010
wrRegOut
0.00165 us
0.0017 us
0.00175 us
0.0018 us
0.00185 us
0.0019 us


LEDR 16 17 18 19 20
clk
reset
IFLATCH
clk
reset
flush
stall
pcIncrementedIn 000001d4 000001d8 000001dc 000001e0 000001e4 000001e8 000001ec 000001f0 000001f4 000001f8 000001fc 00000200 00000204 00000208 0000020c 00000210
instIn 47660001 306c0004 d6204000 252d000d 47660001 306c0004 d5204000 25210009 47660001 306c0004 df204000 252d0005 47660001 306c0004 da204000 252d0001
pcIncrementedOut 000001d0 000001d4 000001d8 000001dc 000001e0 000001e4 000001e8 000001ec 000001f0 000001f4 000001f8 000001fc 00000200 00000204 00000208 0000020c
instOut 25210011 47660001 306c0004 d6204000 252d000d 47660001 306c0004 d5204000 25210009 47660001 306c0004 df204000 252d0005 47660001 306c0004 da204000
IDLATCH
clk
reset
flush
stall
pcIncrementedIn 000001d0 000001d4 000001d8 000001dc 000001e0 000001e4 000001e8 000001ec 000001f0 000001f4 000001f8 000001fc 00000200 00000204 00000208 0000020c
regData1In 00000001 00000011 f0000000 fffffffb0 00000000 00000012 f0000000 fffffffb0 00000001 00000013 f0000000 fffffffb0 00000000 00000014 f0000000 fffffffb0
regData2In 00000001 fffffffb0 00000012 0000004b 00000000 fffffffb0 00000013 0000004b 00000001 fffffffb0 00000014 0000004b 00000000 fffffffb0 00000015 0000004b
immvalIn 00000011 00000001 00000004 00004000 0000000d 00000001 00000004 00004000 00000009 00000001 00000004 00004000 00000005 00000001 00000004 00004000
regWriteNoIn 2 6 2 6 2 6 2 6 2
opcodeIn 2 4 3 d 2 4 3 d 2 4 3 d 2 4 3 d
allowBrIn
brBaseMuxSelIn
alu2MuxSelIn 0 1 0 1 0 1 0 1 0
aluOpIn 6 7 6 7 6 7 6 7 6
cmpOpIn 5 0 6 5 0 5 0 f 5 0 a
wrMemIn
0.00195 us
0.002 us
0.00205 us
0.0021 us
0.00215 us
0.0022 us

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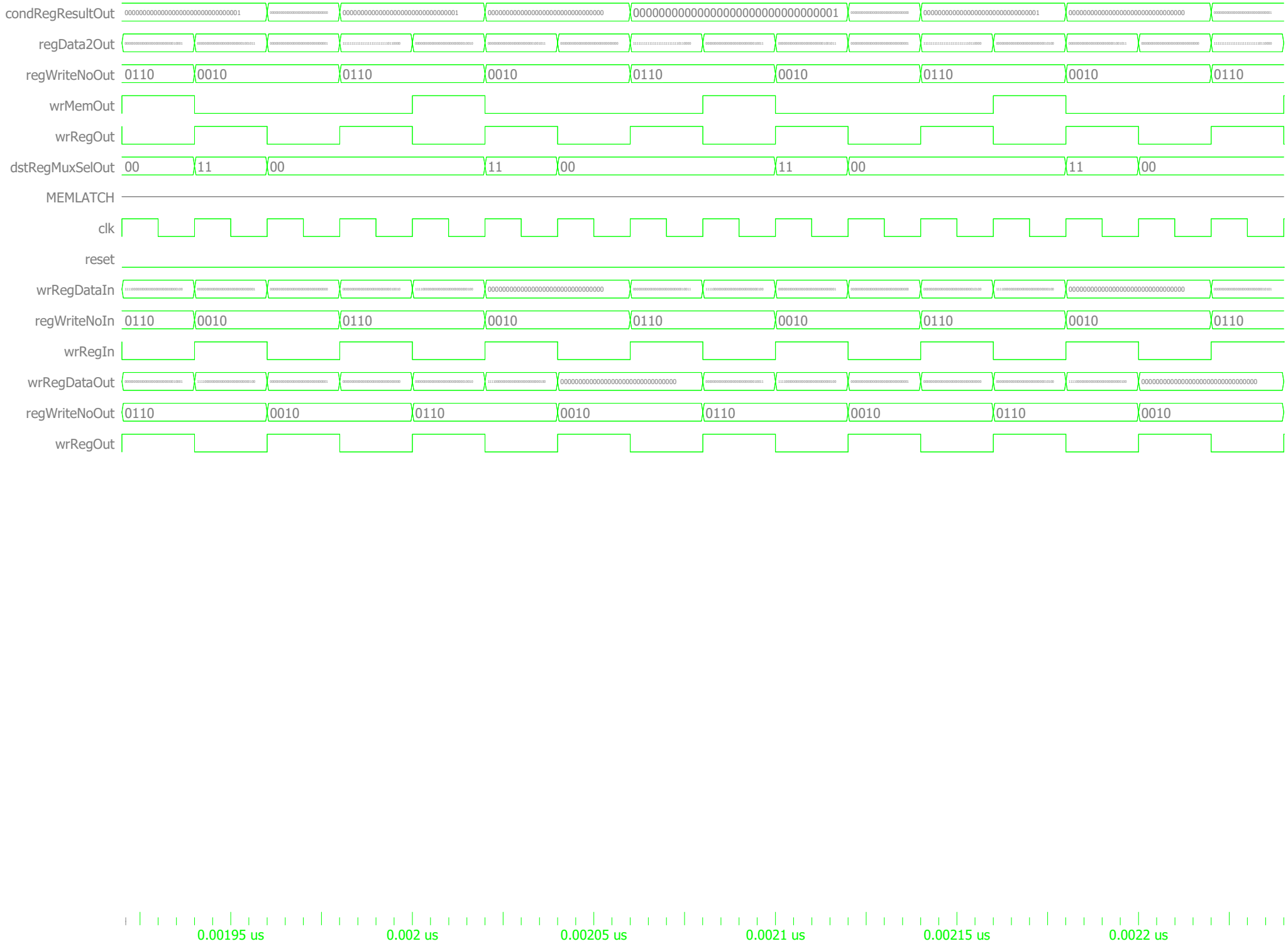
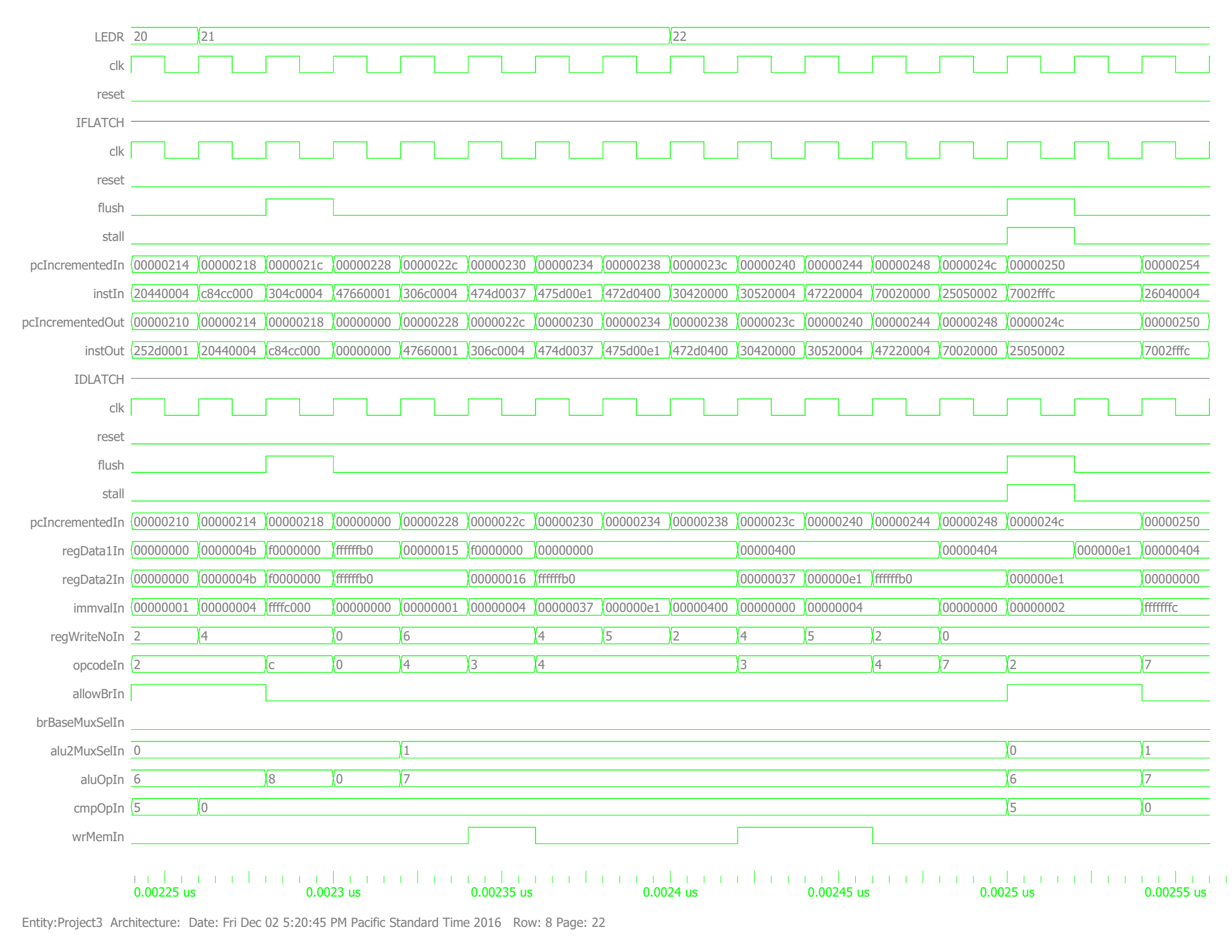

condRegResultOut
regData2Out
regWriteNoOut
0110
0010
0110
0010
0110
0010
0110
0010
0110
wrMemOut
wrRegOut
dstRegMuxSelOut
00
11
00
11
00
11
00
11
00
MEMLATCH
clk
reset
wrRegDataIn
regWriteNoIn
0110
0010
0110
0010
0110
0010
0110
0010
0110
wrRegIn
wrRegDataOut
regWriteNoOut
0110
0010
0110
0010
0110
0010
0110
0010
wrRegOut
0.00195 us
0.002 us
0.00205 us
0.0021 us
0.00215 us
0.0022 us



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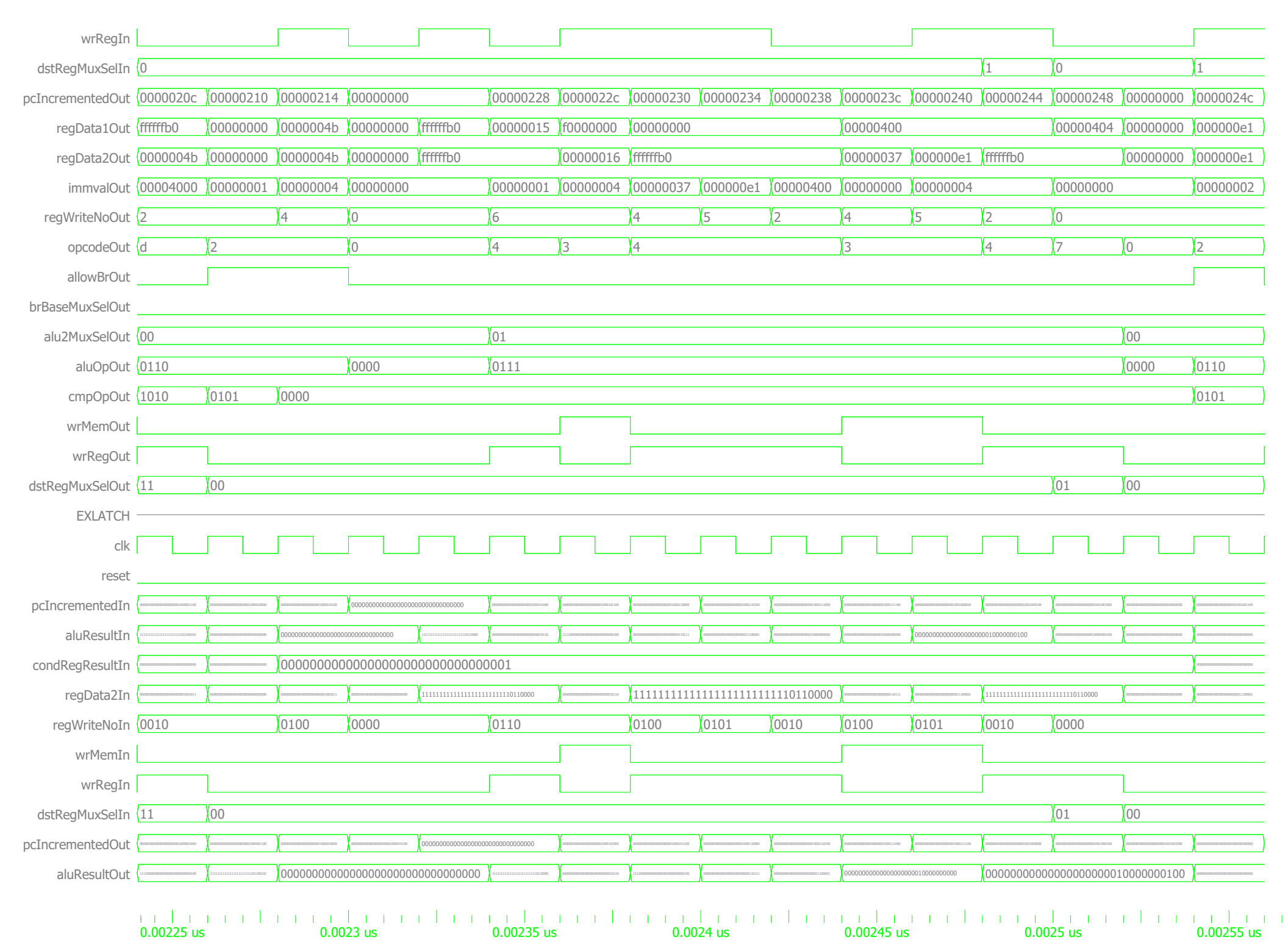

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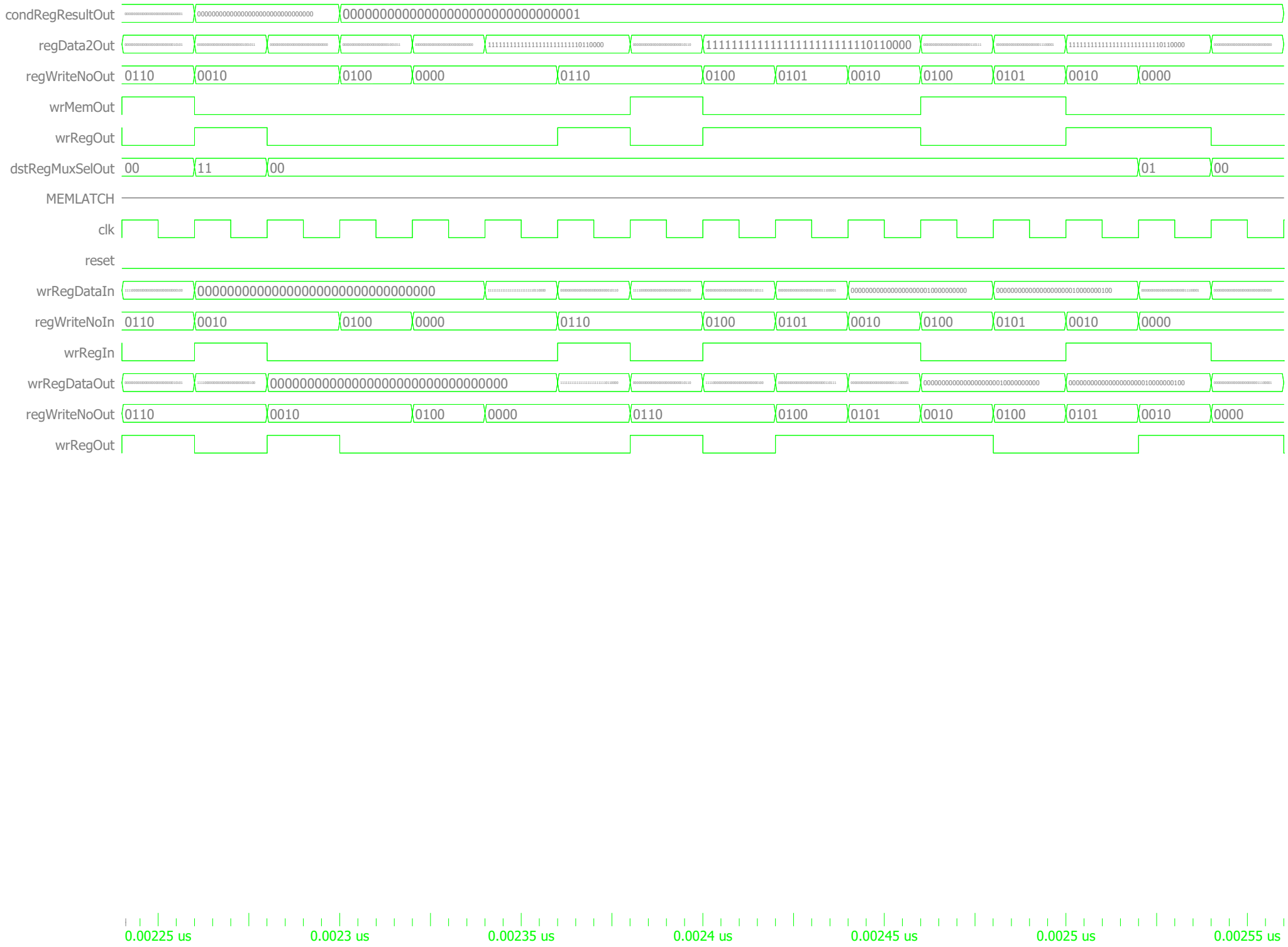
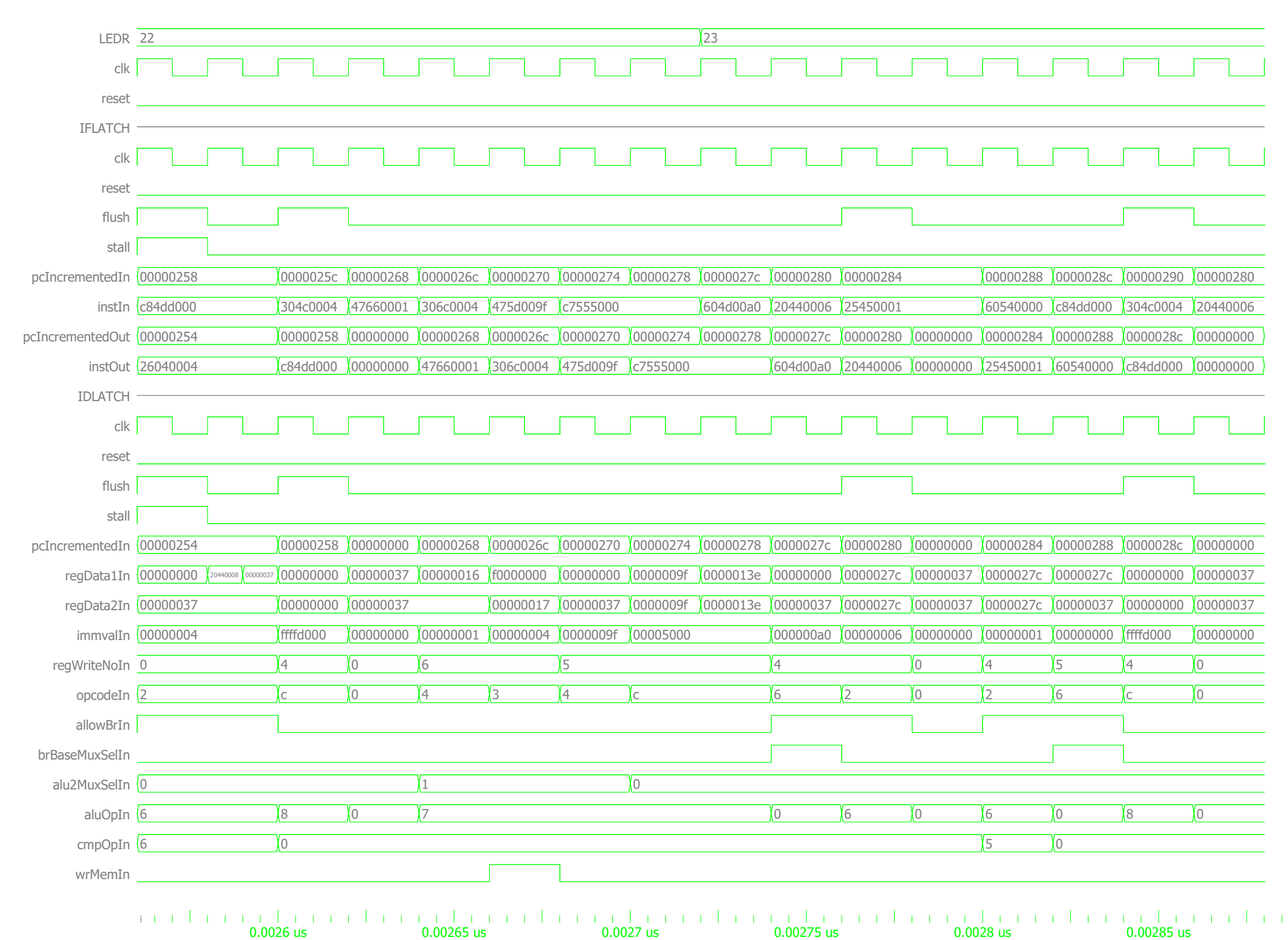

condRegResultOut
regData2Out
regWriteNoOut
wrMemOut
wrRegOut
dstRegMuxSelOut
MEMLATCH
clk
reset
wrRegDataIn
regWriteNoIn
wrRegIn
wrRegDataOut
regWriteNoOut
wrRegOut
0110
0010
0100
0000
0110
0100
0101
0010
0100
0101
0010
0000
00
11
00
01
00
0.00225 us
0.0023 us
0.00235 us
0.0024 us
0.00245 us
0.0025 us
0.00255 us



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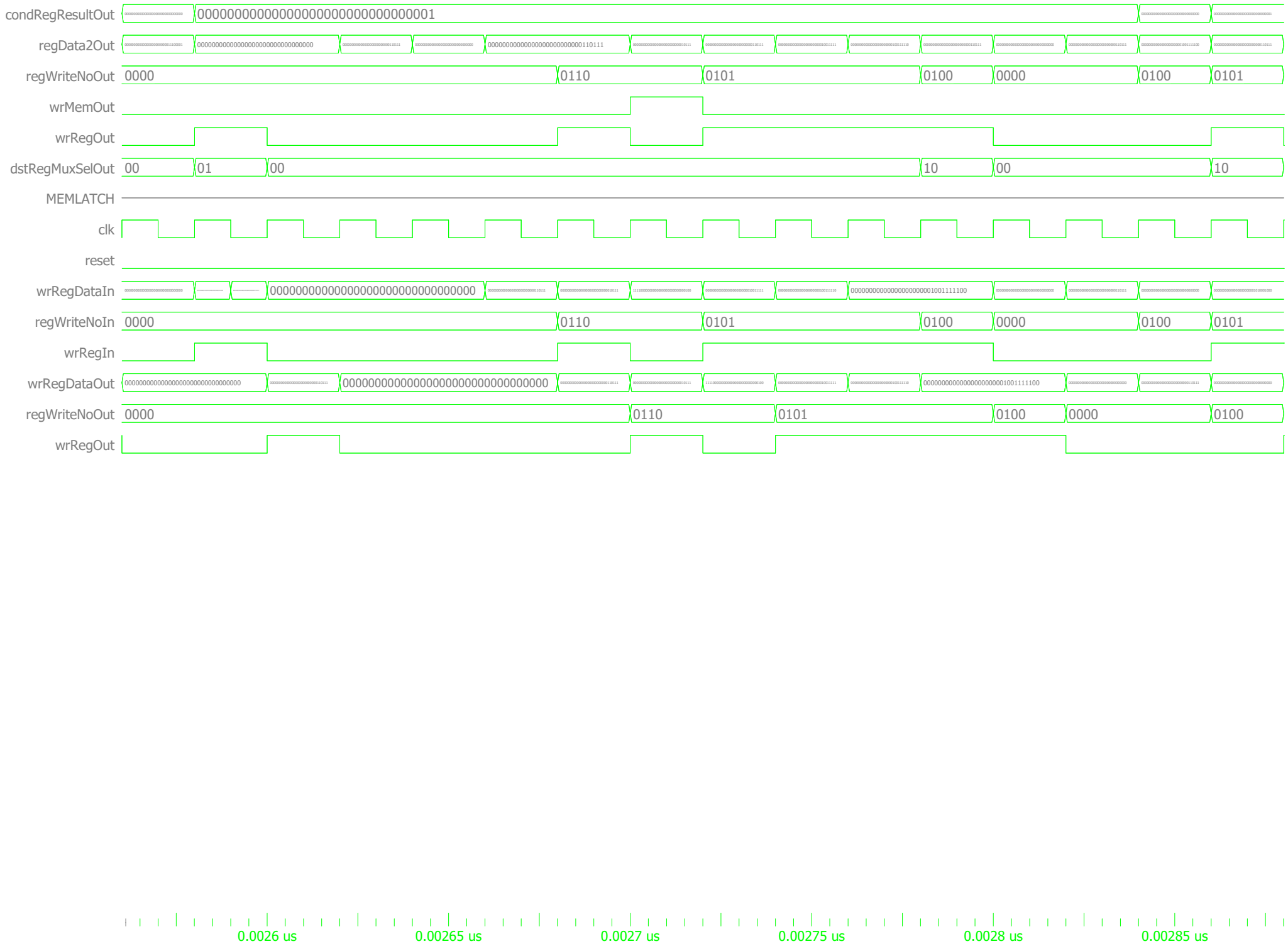
wrRegIn
dstRegMuxSelIn
pcIncrementedOut
regData1Out
regData2Out
immvalOut
regWriteNoOut
opcodeOut
allowBrOut
brBaseMuxSelOut
alu2MuxSelOut
aluOpOut
cmpOpOut
wrMemOut
wrRegOut
dstRegMuxSelOut
EXLATCH
clk
reset
pcIncrementedIn
aluResultIn
condRegResultIn
regData2In
regWriteNoIn
wrMemIn
wrRegIn
dstRegMuxSelIn
pcIncrementedOut
aluResultOut
0.0026 us
0.00265 us
0.0027 us
0.00275 us
0.0028 us
0.00285 us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regData2Out
00000000000000000000000000000000
00000000000000000000000000110111
regWriteNoOut
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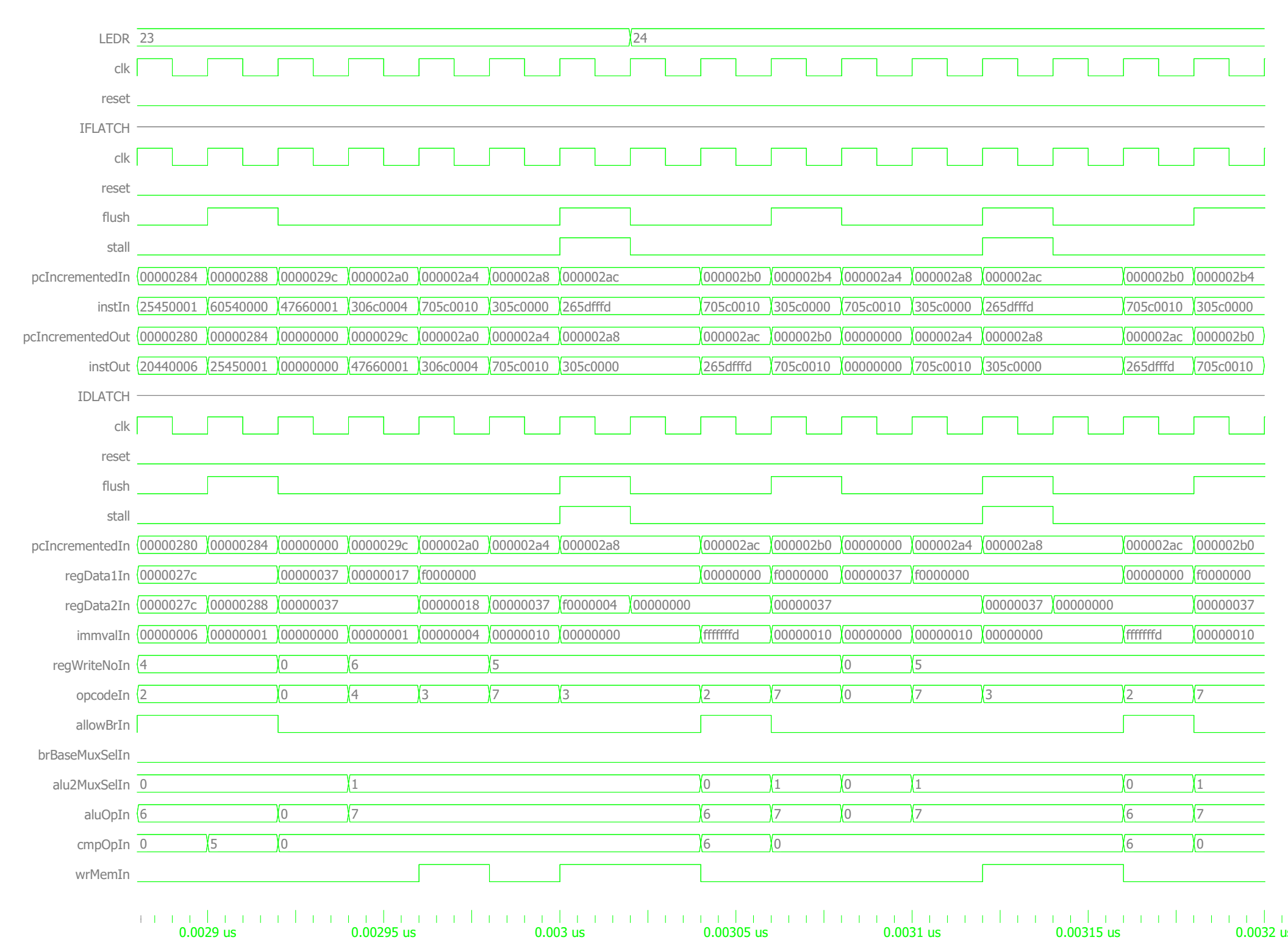
0110
0101
0100
0000
0100
0101
wrMemOut
wrRegOut
dstRegMuxSelOut
00
01
00
10
00
10
MEMLATCH
clk
reset
wrRegDataIn
00000000000000000000000000000000
00000000000000000000001001111100
regWriteNoIn
0000
0110
0101
0100
0000
0100
0101
wrRegIn
wrRegDataOut
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000001001111100
regWriteNoOut
0000
0110
0101
0100
0000
0100
wrRegOut
0.0026 us
0.00265 us
0.0027 us
0.00275 us
0.0028 us
0.00285 us


LEDR 23 24
clk
reset
IFLATCH
clk
reset
flush
stall
pcIncrementedIn 00000284 00000288 0000029c 000002a0 000002a4 000002a8 000002ac 000002b0 000002b4 000002a4 000002a8 000002ac 000002b0 000002b4
instIn 25450001 60540000 47660001 306c0004 705c0010 305c0000 265dfffd 705c0010 305c0000 705c0010 305c0000 265dfffd 705c0010 305c0000
pcIncrementedOut 00000280 00000284 00000000 0000029c 000002a0 000002a4 000002a8 000002ac 000002b0 00000000 000002a4 000002a8 000002ac 000002b0
instOut 20440006 25450001 00000000 47660001 306c0004 705c0010 305c0000 265dfffd 705c0010 00000000 705c0010 305c0000 265dfffd 705c0010
IDLATCH
clk
reset
flush
stall
pcIncrementedIn 00000280 00000284 00000000 0000029c 000002a0 000002a4 000002a8 000002ac 000002b0 00000000 000002a4 000002a8 000002ac 000002b0
regData1In 0000027c 00000037 00000017 f0000000 00000000 f0000000 00000037 f0000000 00000000 f0000000
regData2In 0000027c 00000288 00000037 00000018 00000037 f0000004 00000000 00000037 00000037 00000000 00000037
immvalIn 00000006 00000001 00000000 00000001 00000004 00000010 00000000 fffffffd 00000010 00000000 00000010 00000000 fffffffd 00000010
regWriteNoIn 4 0 6 5 0 5
opcodeIn 2 0 4 3 7 3 2 7 0 7 3 2 7
allowBrIn
brBaseMuxSelIn
alu2MuxSelIn 0 1 0 1 0 1 0 1
aluOpIn 6 0 7 6 7 0 7 6 7
cmpOpIn 0 5 0 6 0 6 0
wrMemIn
0.0029 us
0.00295 us
0.003 us
0.00305 us
0.0031 us
0.00315 us
0.0032 us

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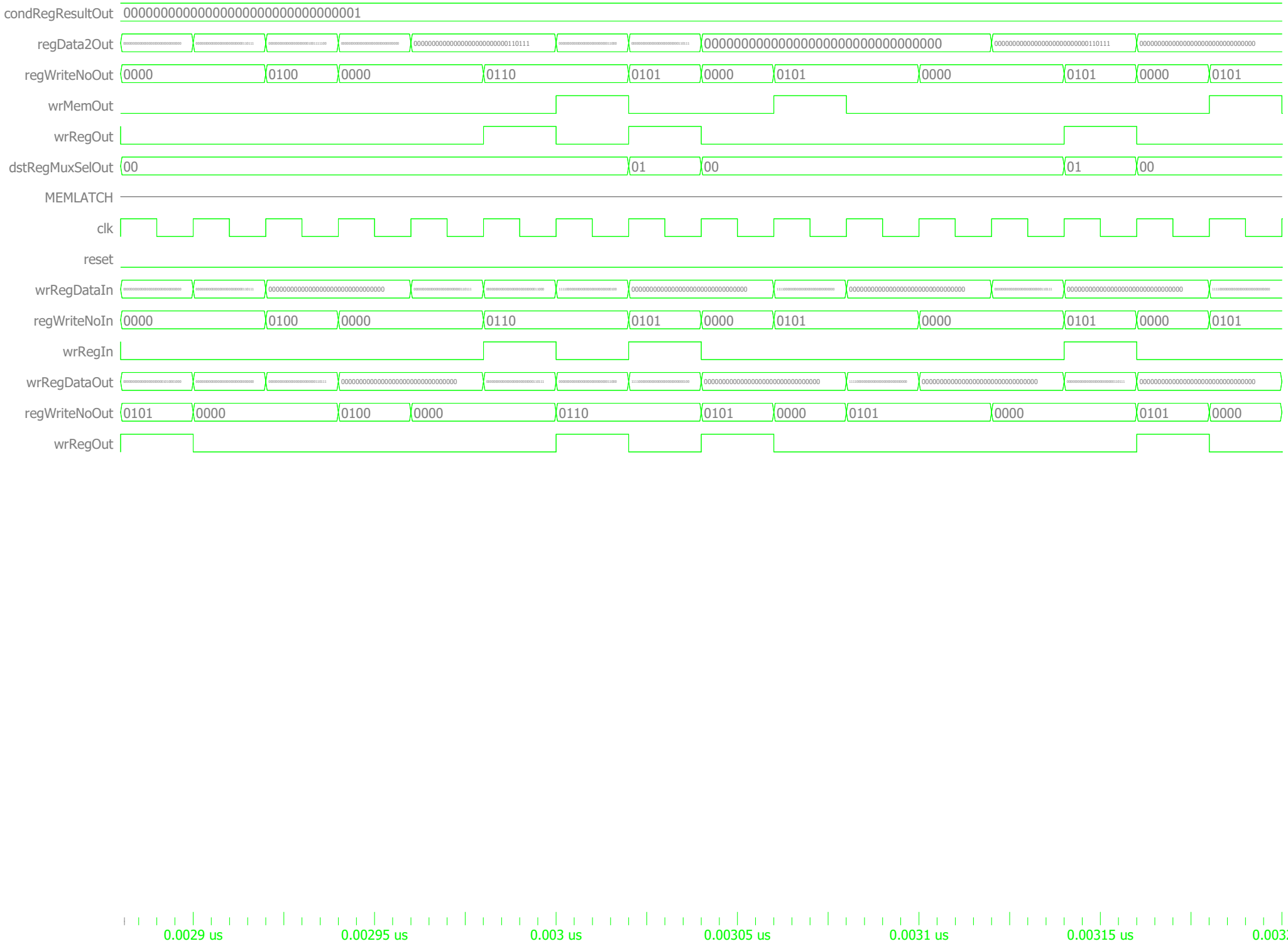
condRegResultOut
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regData2Out
00000000000000000000000000110111
00000000000000000000000000000000
00000000000000000000000000110111
00000000000000000000000000000000
regWriteNoOut
0000
0100
0000
0110
0101
0000
0101
0000
0101
0000
0101
wrMemOut
wrRegOut
dstRegMuxSelOut
00
01
00
01
00
MEMLATCH
clk
reset
wrRegDataIn
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
regWriteNoIn
0000
0100
0000
0110
0101
0000
0101
0000
0101
0000
0101
wrRegIn
wrRegDataOut
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
regWriteNoOut
0101
0000
0100
0000
0110
0101
0000
0101
0000
0101
0000
wrRegOut
0.0029 us
0.00295 us
0.003 us
0.00305 us
0.0031 us
0.00315 us
0.0032 us