Joon Kyung Kim

https://jkim796.github.io/

RESEARCH II	NTERESTS	
Computer Architecture • Compiler Optimizations • Operating Systems • Machine Learning		
EDUCATION		
Georgia Ir	nstitute of Technology	
M.S. i Area	n Computer Science Computing Systems	Expected May 2018
Advis		
_	nstitute of Technology	
B.S. ir Advis	n Computer Science or Dr. Hadi Esmaeilzadeh	May 2016
HONORS AN	D AWARDS	
_	shed Paper Award in IEEE Symposium on High Performance A Unified Template-based Framework for Accelerating Statis	-
•	ech President's Undergraduate Research Award	2015
	ed a salary award (\$1,500) for the TABLA project	10044
	orr Dingwall Foundation orean Ancestry Grant Scholarship Recipient	2011
PUBLICATIO		
Conferen	-	
Learn	$\log^{2} 50^{th}$ International Symposium on Microarchitecture (MICRO),	
[P2] H. Sha	ırma, J. Park, D. Mahajan, E. Amaro, J. Kim , C. Shao, and H. Esmaeilza	
Mode	Is to FPGAs" 49^{th} International Symposium on Microarchitecture (I	adeh, "From High-Level Deep Neural
[P1] D. Ma Templ		edeh, " From High-Level Deep Neural MICRO), October 2016. Esmaeilzadeh, " TABLA: A Unified ng ," 22 nd IEEE Symposium on High
[P1] D. Ma Templ	Is to FPGAs" 49 th International Symposium on Microarchitecture (I hajan, J. Park, E. Amaro, H. Sharma, A. Yazdanbakhsh, J. Kim , and H. I ate-based Framework for Accelerating Statistical Machine Learning Computer Architecture (HPCA), March 2016. (Distinguisher	edeh, " From High-Level Deep Neural MICRO), October 2016. Esmaeilzadeh, " TABLA: A Unified ng ," 22 nd IEEE Symposium on High
[P1] D. Ma Templ Perfor Technical	Is to FPGAs" 49 th International Symposium on Microarchitecture (I hajan, J. Park, E. Amaro, H. Sharma, A. Yazdanbakhsh, J. Kim , and H. I ate-based Framework for Accelerating Statistical Machine Learning Computer Architecture (HPCA), March 2016. (Distinguisher	adeh, "From High-Level Deep Neural MICRO), October 2016. Esmaeilzadeh, "TABLA: A Unified ng," 22 nd IEEE Symposium on High ed Paper Award)

[P1] D. Mahajan, J. Kim, A. Ardalan, A. Kumar, and H. Esmaeilzadeh, "In-RDBMS Hardware Acceleration of Advanced **Analytics**" 44^{th} International Conference on Very Large Data Bases (VLDB 2018).

2017

In Progress

PROFESSIONAL EXPERIENCE

AMAZON WEB SERVICES | SOFTWARE DEVELOPMENT ENGINEER INTERN

SUMMER 2017 | SEATTLE, WA TEAM: AWS AURORA POSTGRES

MENTOR: Arun Sudhir • MANAGER: Ashutosh Galande

• Designed and implemented a client authentication mechanism for AWS Aurora Postgres and RDS Postgres customers by integrating the AWS IAM (Identity and Authentication Management) service.

DELL SECUREWORKS | SOFTWARE DEVELOPER CO-OP SPRING 2015, SUMMER 2014, FALL 2013 | ATLANTA, GA

TEAM: CUSTOMER PORTAL TEAM

MENTOR: Veera Rayala • MANAGER: Chris Phillips

 Developed the customer web portal system and a company internal tool for visualizing server performance metrics.

ARTIFACTS

■ TABLA: An accelerator generator for statistical machine learning algorithms | http://act-lab.org/artifacts/tabla

■ DNNWEAVER: Framework for accelerating Deep Neural Networks

http://act-lab.org/artifacts/dnnweaver

TEACHING EXPERIENCE

Teaching Assistant

Course | Design and Analysis of Algorithms (CS 3510)

Instructor | Dr. Richard Peng

Location | Georgia Institute of Technology

Semester | Fall 2017

Head Teaching Assistant

Course | Design and Analysis of Algorithms (CS 3510)

Instructor | Dr. Merrick Furst

Location | Georgia Institute of Technology

Semester | Spring 2017

Teaching Assistant

Course | Design and Analysis of Algorithms (CS 3510)

Instructor | Dr. Richard Peng

Location | Georgia Institute of Technology

Semester | Fall 2016

SKILLS

PROGRAMMING LANGUAGES

■ C, C++, Python, Java, Bash

FRAMEWORKS

LLVM