***Activity-3***

To study and verify the truth table of the basic logic gates (AND,OR,NOT,XOR,XNOR) and the universal gates (NAND,NOR).

***Truth Table with Diagrams :-***

***\**NOT Gate**

|  |  |  |
| --- | --- | --- |
| **A** | **Diagram** | **F** |
| 0 | A picture containing text, game  Description automatically generated | 1 |
| 1 | Chart, line chart  Description automatically generated | 0 |

**\*AND Gate**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **Diagram** | **F** |
| 0 | 0 | **Diagram, schematic  Description automatically generated** | 0 |
| 0 | 1 | **Diagram, schematic  Description automatically generated** | 0 |
| 1 | 0 | **Diagram, schematic  Description automatically generated** | 0 |
| 1 | 1 | **A picture containing game  Description automatically generated** | 1 |

**\*OR Gate**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **Diagram** | **F** |
| 0 | 0 | **Diagram, schematic  Description automatically generated** | 0 |
| 0 | 1 | **Diagram  Description automatically generated** | 1 |
| 1 | 0 | **Diagram  Description automatically generated** | 1 |
| 1 | 1 | **Diagram  Description automatically generated** | 1 |

**\*NAND Gate**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** |  | **F** |
| 0 | 0 | **Diagram, schematic  Description automatically generated** | 1 |
| 0 | 1 | **Diagram, schematic  Description automatically generated** | 1 |
| 1 | 0 | **Diagram, schematic  Description automatically generated** | 1 |
| 1 | 0 | **Diagram, schematic  Description automatically generated** | 0 |

**\*NOR Gate**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** |  | **F** |
| 0 | 0 | **Diagram, schematic  Description automatically generated** | 1 |
| 0 | 1 | **Diagram  Description automatically generated** | 0 |
| 1 | 0 | **Diagram, schematic  Description automatically generated** | 0 |
| 1 | 1 | **Diagram  Description automatically generated** | 0 |

**\*XOR Gate**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** |  | **F** |
| 0 | 0 | **Diagram, schematic  Description automatically generated** | 0 |
| 0 | 1 | **Diagram  Description automatically generated** | 1 |
| 1 | 0 | **A picture containing game, text  Description automatically generated** | 1 |
| 1 | 1 | **Diagram  Description automatically generated** | 0 |

**\*XNOR Gate**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** |  | **F** |
| 0 | 0 | **Diagram  Description automatically generated** | 1 |
| 0 | 1 | **Diagram  Description automatically generated** | 0 |
| 1 | 0 | **Diagram, schematic  Description automatically generated** | 0 |
| 1 | 1 | **Diagram  Description automatically generated** | 1 |

**Result :-**

I had verified the truth table of the logic gates (AND,OR,NOT,XOR,XNOR) and Universal Gates(NAND,NOR).