LAB #7: SUBWAY SIGNAL CONTROL LOGIC II (Cadence & Verilog)

Objective:

- The objective of this lab is to expand the subway signal control logic by adding a sequential logic to it.

Lab Description and Specs:

- **Function:**
  This is the continuation of Lab 3. In Lab 3, the direction signal D is given as a primary input signal. Now, let's design a finite state machine to generate signal D. Let's assume that the traffic pattern for the track is such when two consecutive left-to-right trains passed by, the next train must go from right-to-left. After that, there will be two more left-to-right trains, etc.

  To detect the train direction through the station, we set up two light beams just above the rail track and place two photocells, P1 and P2, some distance apart. Assume the train can fit inside of the two beams. When the beam shines on a photocell, it produces a 0, and when the beam is blocked, it produces a 1. The train may stop at the middle of the photocells. If this happens, no change is made to signal D. If the train stopping at the middle and then back to the direction it came from, then this train does not count as a passing train. Design a logic circuit to generate D. Make sure the location of the train can be tracked when it is passing the station.

- **Inputs:**
  - *P1, P2*: Two photocell outputs
  - *Reset*: Global reset

- **Outputs:**
  - *D*

Recommended Procedures:

- For this lab you will use the Cadence to design and verify your circuit.

  a. Construct a state transition diagram.
  b. Perform state minimization and encoding.
  c. Design the sequential logic in Verilog.
  d. Synthesize the Verilog model to the gate level schematic
  e. Run Cadence to verify the functionality.

Prelab:

1. State Transition Diagram
2. Boolean Equations

Questions:

- Compare and contrast a Moore Finite State Machine (FSM) with a Mealy FSM.