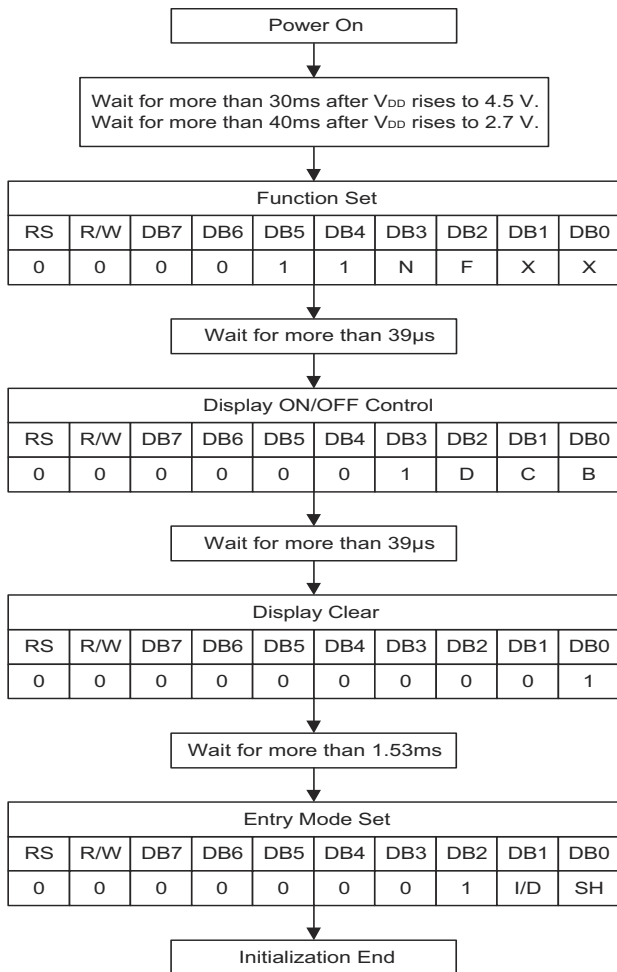


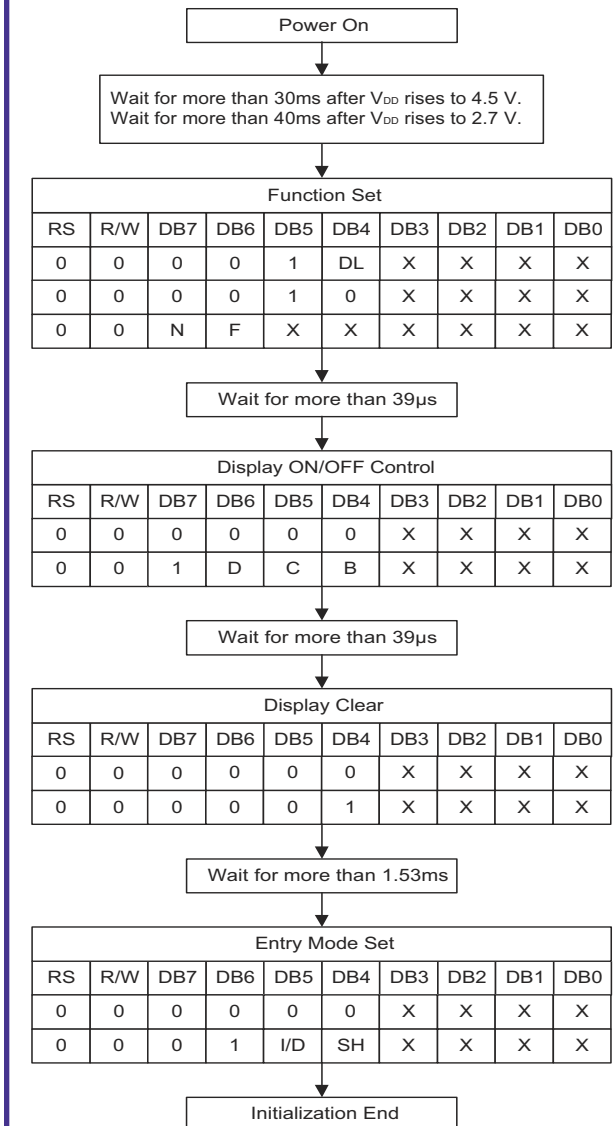
## LCD Modules ~ Initialization Instructions

## 4 and 8 Bit Interface

### 8- Bit Interface



### 4- Bit Interface



D/L	0	4-bit mode
	1	8-bit mode

D	0	Display off
	1	Display on

I/D	0	Decrement mode
	1	Increment mode

N	0	1-line mode
	1	2-line mode

C	0	Cursor off
	1	Cursor on

SH	0	Entire shift off
	1	Entire shift on

F	0	Display off
	1	Display on

B	0	Blink off
	1	Blink on



## LCD Modules ~ Initialization Instructions

## Instruction Codes

Instruction	Instruction Code										Description Instruction Code	Execution time (fsoc=270kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC.	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and make shift of entire display enable.	39μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	39μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	39μs
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length (DL : 4-bit/8-bit), numbers of display line (N : 1-line/2-line), display font type(F : 5 X 8 dots/ 5 X 11 dots)	39μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43μs

NOTE: When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc is necessary for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "LOW".



# LCD General Information



## LCD Modules ~ Graphic

## Instructions

Class		CODE												Command Description	Number of Read Bytes																				
		RD	WR	AO	D7	D6	D5	D4	D3	D2	D1	D0	Hex																						
System Control	SYSTEM SET	1	0	1	0	1	0	0	0	0	0	0	40	Initialize device and display	8																				
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode	0																				
Display Control	DISPLAY ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58 59	Enable and disable display and display flashing (D = 0: Display OFF, D = 1: Display ON)	1																				
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions	10																				
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type	2																				
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM	2																				
	CSRDIR	1	0	1	0	1	0	0	1	1	C2	C1	4C to 4F	<table><tr><td>C</td><td>C2</td><td>C1</td><td>Shift Direction</td></tr><tr><td>4CH</td><td>0</td><td>0</td><td>Right</td></tr><tr><td>4DH</td><td>0</td><td>1</td><td>Left</td></tr><tr><td>4EH</td><td>1</td><td>0</td><td>Up</td></tr><tr><td>4FH</td><td>1</td><td>1</td><td>Down</td></tr></table>	C	C2	C1	Shift Direction	4CH	0	0	Right	4DH	0	1	Left	4EH	1	0	Up	4FH	1	1	Down	0
	C	C2	C1	Shift Direction																															
	4CH	0	0	Right																															
	4DH	0	1	Left																															
	4EH	1	0	Up																															
4FH	1	1	Down																																
HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position	1																					
OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format	1																					
Drawing Control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address	2																				
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor address	2																				
Memory Control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory	-																				
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory	-																				

### [Notes]

- In general, the internal registers of the SED1330F are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged.
  - 2byte parameters (where two bytes are treated as 1 data item) are handled as follows:
    - CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.
    - SYSTEM SET, SCROLL, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.



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