

	Sample Programmi	ng: TURN ON/OFF LED
How to use? Like other microchip A	rduino, PIC, AVR We need t	o have 2 steps
Step 2: Set value ON/0		→ 2. Set value (R/W)
mov r1,#1 lsl r1,#3	; RI=I ; 3 times	For example: Defining GPIO35 is output
str r1,[r0,#32]	; [R0+32]=R1 <b>→</b> ON	<ul> <li>GPIO35 is 0x3F200020 to 0x3F200024 (or offset 32)</li> <li>Bit 3<sup>th</sup></li> </ul>
mov r1,#1 lsl r1,#3	; R1=1 ; 3 times	7 6 5 4 3 2 1 0 GPI039 GPI038 GPI037 GPI038 GPI035 GPI034 GPI033 GPI032 0 0 0 0 1 0 0 0
str r1,[r0,#44]	; [R0+44]=R1 <b>→</b> OFF	→ For set ON
		<ul> <li>GPIO35 is 0x3F20002C to 0x3F200030 (or offset 44)</li> <li>Bit 3<sup>th</sup></li> </ul>
		→ For set OFF
		ng: TURN ON/OFF LED
Full program for GPIO macro delay {	18	loop\$:
local .wait		mov rI,#I
mov r2,#0x3F0000		lsl r1,#18 str r1,[r0,#28] ; 28=LED ON; 40=LED OFF
.wait: sub r2,#I cmp r2,#0		delay
bne .wait		mov rl,#l
BASE = \$3F0000		lsl r1,#18 str r1,[r0,#40] ; 28=LED ON; 40=LED OFF
GPIO_OFFSET=\$2000 mov r0,BASE orr r0,GPIO_OFFSE		delay b loop\$
mov r1,#1 lsl r1,#24		
str r1,[r0,#4]; finish	ned select GPIO18	
	Sample Programmi	ng: TURN ON/OFF LED
	GPIO9 and GPIO18 (15 mins	
•	•	,

Sample Pi	ogramming: TURN ON/	OFF LED
Example: Blink LED in GPIO9 and GF	PIO18 (15 mins)	
macro delay {	mov r1,#1 lsl r1,#27	
local .wait mov r2,#0x3F0000 .wait:	loop\$: str r1,[r0,#0]; finis mov r1,#1 lsl r1,#18	shed select GP109
sub r2,#1 cmp r2,#0 bne .wait }	mov r3, #9 orr r1,r3 str r1,[r0,#28] ; ON delay	loop\$:  mov r1,#1  lsl r1,#18  mov r3,#1
BASE = \$3F000000 GPIO_OFFSET=\$200000 mov r0,BASE orr r0,GPIO_OFFSET	mov r1,#1 lsl r1,#18 mov r1, #1 lsl r3,#9 orr r1,r3	lsl r3, #9 orr r1,r3 str r1,[r0,#28] ; ON delay
mov r1,#1  sl r1,#24  str r1,[r0,#4] ; finished select GPIO18	str r1.[r0,#40] ; OFF delay b loop\$	str r1,[r0,#40] ; OFF delay b loop\$

Sample Programming: TURN ON/OFF LED						
Example: Blink LED in GPIO5 and GPIO6 (5 mins)						

Sample Programming: TURN ON/OFF LED					
How to use?					
Like other microchip Arduir	no, PIC, AVR We need	to have 2 steps			
Step 2: Set value ON/OFF	for GPIO	→ 2. Set value (R/W)			
lsl r1,#3 ; str r1,[r0,#32] ;	$R1=1$ 3 times $[R0+32]=R1 \Rightarrow ON$	For example: Defining GPIO35 is output GPIO35 is 0x3F200020 to 0x3F200024 (or offset 32) Bit 3th			
lsl r1,#3 ;	RI=1 3 times $[R0+44]=R1 \Rightarrow OFF$	7 6 5 4 2 1 0 GPIO39 GPIO38 GPIO37 GPIO36 GPIO35 GPIO34 GPIO33 GPIO32 0 0 0 0 1 0 0 0			
Need the delay time among 2 states Because it is very fast		→ For set ON  • GPIO35 is 0x3F20002C to 0x3F200030 (or offset 44)  Bit 3 <sup>th</sup> → For set OFF			

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# Sample Programming: TURN ON/OFF LED How to code the delay function/delay code macro delay { local .wait mov r2, #0x3F0000; [r2] = 0x3F0000 .wait: sub r2,#1 ; [r2]=[r2]-1 cmp r2,#0 ; compare [r2] and zero bne .wait ; if not equal then goto .wait }

NEW COMMAND				
For details				
• Command: cmp				
→ Compare a register with a value (register), and store result to Application Program Status Register (APSR)  Example: cmp r1, #20				
Command: b				
→ unconditional branch				
Example: b loop\$ → goto loop\$ label				
Command: beq				
→ Branch if equal				
Example:				
$cmp \ r1, r2$				
beq loop\$ $\rightarrow$ goto loop if $r1 == r2$ . (Access APSR to get result of cmp)				
Command: bge				
→ Branch if greater equal Example:				
$cmp \ rl, r2$				
bge loop\$ → goto loop if r1>=r2. (Access APSR to get result of cmp)				

### NEW COMMAND For details Command: bgt Branch if greater than Example: cmp r1, r2 bgt loops goo loop if r1 > r2. (Access APSR to get result of cmp) Command: ble Branch if lesser equal than Example: cmp r1, r2 ble loops goto loop if r1 <= r2. (Access APSR to get result of cmp) Command: blt Branch if less than Example: cmp r1, r2 blt loops goto loop if r1 < r2. (Access APSR to get result of cmp)

	N	EW COMM	AND
Su	uffix	Flags	Meaning
EG	Q	Z set	Equal
N	E	Z clear	Not equal
CS	S or HS	C set	Higher or same (unsigned >= )
CC	C or LO	C clear	Lower (unsigned < )
м	11	N set	Negative
PI	L	N clear	Positive or zero
V	S	V set	Overflow
V	c	V clear	No overflow
Н	í.	C set and Z clear	Higher (unsigned >)
LS	5	C clear or Z set	Lower or same (unsigned <=)
G	E	N and V the same	Signed >=
u	Г	N and V differ	Signed <
G	Т	Z clear, N and V the same	Signed >
LE	E	Z set, N and V differ	Signed <=

	NEW COMMAND			
For exam	nple			
mov r2,3 loop1:	#0			
,	add r2,#1 cmp r2,#10	;1,2,3,4,5,6,7,8,9,10		
bne loop		;this counts to 10		

NEW COMMAND			
; second method loops; mov r1,#1 Isl r1,#18 str r1,fr0,#28] ; 28=LED ON; 40=LED OFF mov r2,#0x3F0000 .wait: sub r2,#1 cmp r2,#0			
bne_wait mov_r1,#1  sl r1,#18  str_r1,[r0,#40] ; 28=LED ON; 40=LED OFF mov_r2,#0x3F0000			
wait: sub r2.#1 cmp r2.#0 bne wait b loop\$	→ .wait → delay time → get 100% of CPU → Not accuracy → → How to replace?		

# TIMER (Remind) 5. LDR Idr r0, [r1] → Load r0 with the value pointed to by r1; Herein, the r0 and r1 are the 32bit register (4 bytes) 6. LDRD Idrd r6, r7, [r3] → [r3] points to a address 64bit (8 bytes) → r6= 4 lower bytes and r7= 4 higher bytes 7. Sub sub r8, r6, r5 → r8 = r6-r5

### TIMER

- RPi has a dedicated timer register:
- Independent of clock speed.
- Housed inside the same chip as the ARM CPU, the GPIO, GPU, RAM and most other things.
- This chip is called the SoC (System on a Chip).
- The Timer registers start at BASE address  $+\,0x3000$
- Timer counts 1 microsecond intervals (10-6 second)

			TIMER REGISTE	K.
Byte offset (from BASE)	Size / Bytes	Name	Description	Read or Write
0x3000	4	Control / Status	Register used to control and clear timer channel comparator matches.	RW
0x3004	8	Counter	A counter that increments at 1MHz.	R
0x300C	4	Compare 0	Oth Comparison register.	RW
0x3010	4	Compare 1	1st Comparison register.	RW
0x3014	4	Compare 2	2nd Comparison register.	RW
0x3018	4	Compare 3	3rd Comparison register.	RW

### TIMER REGISTER

- ARM (Raspberry) uses timer with 16 bit and prescale 1:8
- **→**8.2<sup>16</sup>= 524288 (microsecond)
  - = 0.524 (second)
- → hexa: \$80000

It may be used for a variety of purposes, including measuring the pulse lengths of up to two input signals (input capture) or generating up to two output waveforms (output campare and PWM).

This description overs one or two 16-bit timers. In ST7 devices with two timers, register names are prefixed with TA (Timer 4) or TB (Timer 8). The Programmable prescaler: f<sub>crit</sub> divided by 2, 4 or 8. Overflow status flag and maskable interrupt. External relocations.

- Overflow status flag and maskable interrupt External clock incur (must ba at least 4 times, slower than the CPU clock speed) with the choice, of active edge Cutput compare functions with: —2 dedicated 19-bit registers —2 dedicated 19-bit registers —2 dedicated status flags —1 dedicated status flags —1 dedicated status flags —1 dedicated status flags —2 dedicated status flags —2 dedicated status flags —2 dedicated status flags —3 dedicated status flags —4 dedicated status flags —4 dedicated status flags —5 dedicated status flags —6 dedicated status flags —7 dedica

When reading an input signal on a non-bonded pri, the value will always be 1".

12.3.1 Counter Description
The anni block of the Programmable Timer is a 1-b-bit feer numbin guocuntier and its associated for the registers. The counter displaces are made up Counter Register Counter Registers (CHR) is seen to see the counter Register (CHR)

— Counter High Register (CHR) is the most significant type (MS Syeu).

nificant byte (MS Byte).

Counter Low Register (CLR) is the least significant byte (LS Byte).

emate Counter Register (ACR).

Alternate Counter High, Register (ACHR) is the most significant byte (MS Byte).

the most significant byte (MS Byte).

Alternate Counter Low Register (ACLR) is the least significant byte (LS Byte). Those two readonly 16-bit registers contain the same yaloe but with the difference that reading the ACLR register does not clear the TOF bit (Timer overflow flag), located in the Status register (SR). See note at the end of paragraph titled 16-bit read writing in the CLR register or ACLR register resets the free running counter to the FFFCh value.

Both counters have a reset value of FFFCh (this is the only value which is reloaded in the 16-bit tim-er). The reset value of both counters is also FFFCh in One Pulse mode and PWM mode. FFFCI in One Pulse mode and FWM mode. The timer clock depends on the clock control bits of the CR2 register, as illustrated in Table 1. The value in the counter register repeats every 131072, 262144 or \$24286 CPU clock sydes depending on the CC[1:0] bits.

The timer frequency can be f<sub>CPU</sub>/2, f<sub>CPU</sub>/4, f<sub>CPU</sub>/8 or an external frequency.

w.st.com/resource/en/datasheet/st72215g2.pdf

### HOW TO USE THE TIMER?

BASE = \$3F000000

mov r3,BASE

;store base address of timer (r3)

mov r4,\$80000 store delay (r4) 0.524 second

Idrd r6,r7,[r3,#4]

timerloop:

sub r8,r6,r5

cmp r8,r4

;read currenttime (r6)

;compare remainingtime (r8), delay (r4)

TIMER OFFSET = \$3000

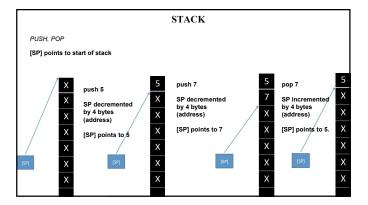
orr r3,TIMER\_OFFSET

;mov starttime (r5)(=currenttime (r6))

Idrd r6,r7,[r3,#4]

;remainingtime (8)= currenttime (r6) - starttime (r5)

;loop if LE (reaminingtime <= delay)



STACK - ASM	
Using keyword: push and pop	
Example:  push{r2}  push{r5}	
push(r6,r7) pop(r2)	
pop{r7}	