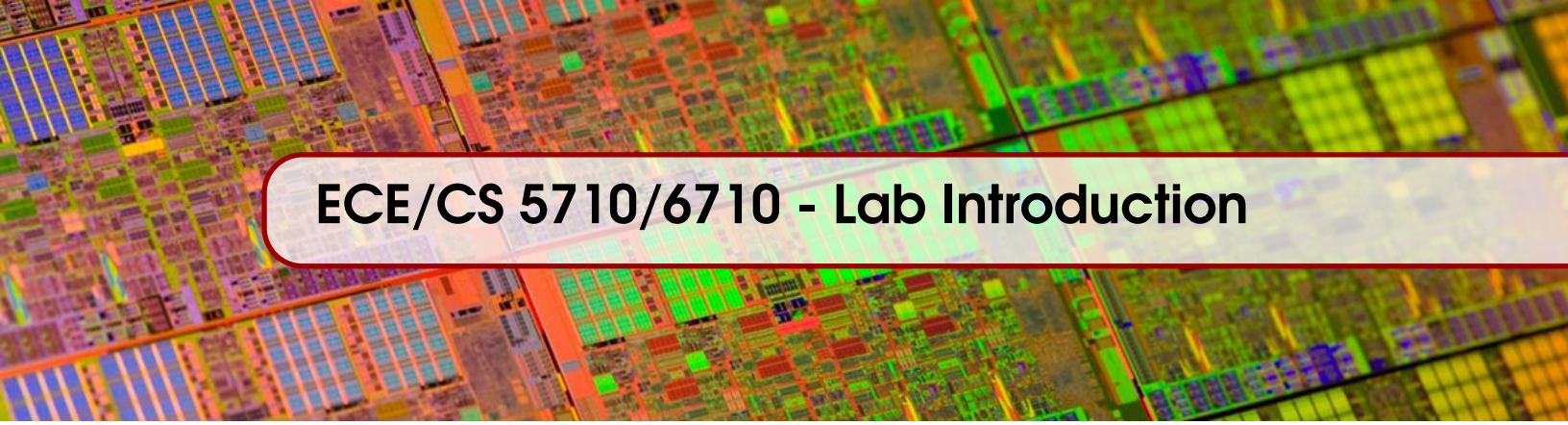

ECE/CS 5710/6710 - Lab Introduction

1 Assignments Deadlines

The pre-lab report have to be submitted through Canvas as a **.pdf** file on Monday at 12pm (noon), the same week of the lab.
The lab report have to be submitted through Canvas as a **.pdf** file on Sunday at 11.59pm, the same week of the lab.

2 Lab Schedule

You will be guided through the tools through complete lab manuals and you will receive the aid of the TA in the labs and project (**every week, the TAs will be available at least one hour every day of the week to answer your questions - check out their hours on Canvas**). However, there is no specific lab class that you are required to attend. You can perform the labs and your project at your own convenience, either in the CADE lab at the University, or across the network. Remember that nothing can replace taking the time to read the CAD tool documentation. The lab activities for the semester will be as follows:

- Lab 1: CMOS Inverter - Schematic and Circuit Simulation
- Lab 2: CMOS Inverter - Physical Design
- Lab 3: Design and Characterization of a D Flip-Flop
- Lab 4: Logic Synthesis and Front-end Flow
- Lab 5: Floorplanning and Back-end Flow
- Project

3 CADE Machine and CAD Tools Setup

1. For the labs, since you are using Windows machines, you need to connect to the CADE lab machines via remote access. If this is your first time connecting to the CADE machines, follow the tutorial here: CADE Lab Remote Access.
2. Once connected to the CADE machine, you will need several files and scripts to properly setup the CADE tools using the TSMC 180nm design kit. The first step to setup the tools automatically is to modify the startup script for the shell you are using. Go to your home directory and open the appropriate shell startup file (note that those files start with a dot so you need to run $ls - a$ to see them) with a text editor such as gedit or vi (or create it if the file does not exist):
   - .tcshrc – startup for the tcsh shell (used by default on the CADE machines),
   - .cshrc – startup for the csh shell,
   - .bashrc – startup for the bash shell.

   Add the following line to the *.tcshrc* (if you use the default shell) file:

```
source /research/ece/lnis-teaching/5710_6710_F20/Setup_scripts/setup_tools
```

Please check that your shell startup file does not contain commands from previous files (such as other path definition) since it could cause conflicts with the EDA tools. If it does, remove those commands.

3. Create a new folder in your personal space for this class. This will be your working directory. It is important to work in a new directory to have a clean working environment since some conflict might appear if you worked with other process design kits in the past in the same directory.

```
mkdir name_of_your_folder_for_the_labs
```

4. Go to the directory you just created by running the following command:

```
cd name_of_your_folder_for_the_labs
```

5. Run the following command to install all the files (this step has to be done only the first time):

```
source /research/ece/lnis-teaching/5710_6710_F20/Setup_scripts/setup_directories
```

The installation script created a design project directory containing different subdirectories. The necessary files for using the different tools are installed in appropriate project subdirectories. The main project subdirectories are organized as follows:

- The *virtuoso* directory contains all files required for editing transistor-level schematics, simulations and layouts using the Cadence Virtuoso®, Spectre® and Mentor Calibre® tools with the TSMC 180*nm* design kit.
- The *innovus* directory contains all files required to do the standard cell Place & Route steps using the Cadence Innovus® tool.
- The *design_compiler* directory contains all files required to perform *Register Transfert Level* (RTL) synthesis using the Synopsys Design Compiler® tool.
- The *HDL* directory the VHDL and/or Verilog source files created by the user or generated by the tools. The RTL netlists will be placed in the *HDL/RTL* subdirectory while the gate-level netlists will be placed in the *HDL/GATE* directory.
- The *modelsim* directory will be used to perform Verilog/VHDL simulations using the Mentor Modelsim® tool.

Each tool has to be run in its own subdirectory, otherwise it may not work properly. Each tool subdirectory contains important files such as setup, configuration, and library files so launching the tool in another directory may not work. Another reason to have one subdirectory per tool is to keep the many generated files whose output cannot be always (easily) controlled in well-defined places so the project structure is better organized.

4 TSMC Non Disclosure Agreement

As you will use commercial data from TSMC, a *Non Disclosure Agreement* (NDA) has to be signed where you agree not to disclose any file/data from TSMC you will use during the labs. **Please print, read careffully and sign the Individual NDA for University Account and bring it to the TAs during a lab hour office**. Without signing it, you are not legally authorized to use the TSMC data and hence do the labs.

5 Tools Versions

The following tool versions have been used when writing the labs:

- Synopsys Design Compiler® 2015.06-SP5
- Cadence IC® 6.1.8.070
- Cadence Spectre® 19.10.162
- Cadence Innovus® 19.12
- Mentor Calibre® 2018.2_15.10
- Mentor Modelsim® 10.7b