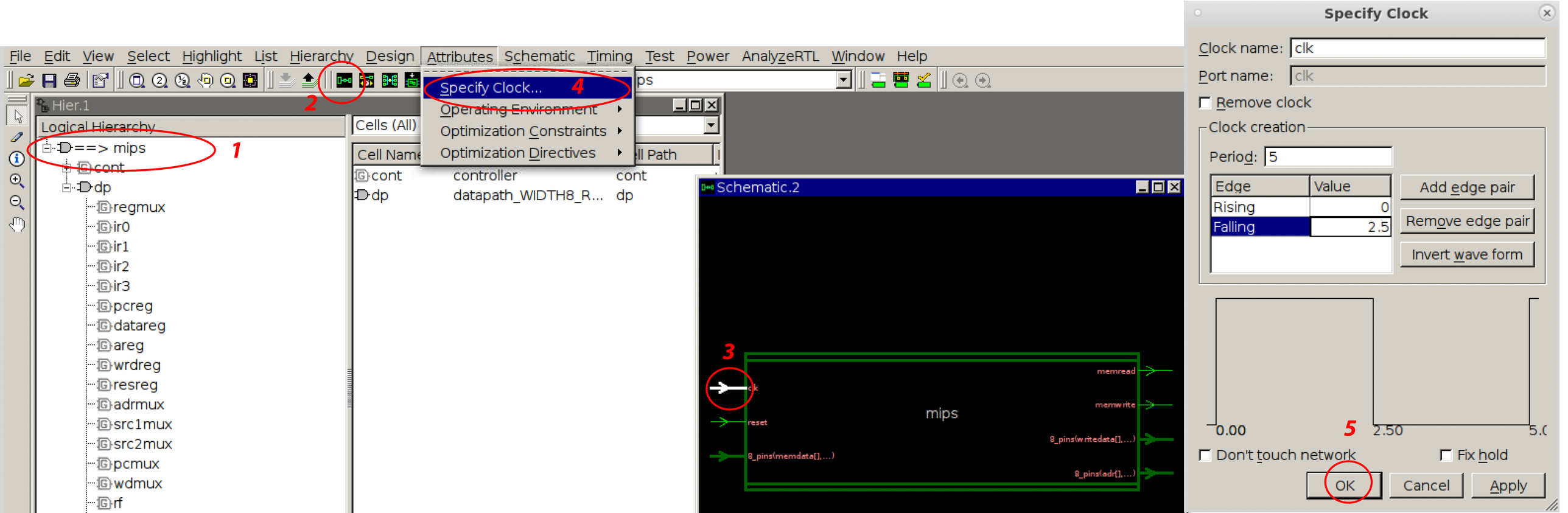
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
Specify Clock... 4
Operating Environment
Optimization Constraints
Optimization Directives
2
Hier.1
Logical Hierarchy
==> mips
1
cont
dp
regmux
ir0
ir1
ir2
ir3
pcreg
datareg
areg
wrdreg
resreg
adrmux
src1mux
src2mux
pcmux
wdmux
rf
Cells (All)
Cell Name
Path
cont controller cont
dp datapath_WIDTH8_R... dp
Schematic.2
3
clk
reset
8_pins(memdata[],...)
mips
memread
memwrite
8_pins(writedata[],...)
8_pins(adr[],...)
Specify Clock
Clock name: clk
Port name: clk
Remove clock
Clock creation
Period: 5
Edge
Value
Rising 0
Falling 2.5
Add edge pair
Remove edge pair
Invert wave form
0.00
5
2.50
Don't touch network
Fix hold
OK
Cancel
Apply