

```
giacomini@lnissrv2:synopsys_dc
File Edit View Search Terminal Help
DC Util
DFTMA
Power Cor
Design
DC Exp
Design V
HDL Comp
VHDL Cor
DFT C
Design C

Version M-2016.12-SP3 for

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ry to Synopsys,
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se, reproduction,
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ited.
Initializing...
Initializing gui preferences from file
s_dv_prefs.tcl
design_vision> 4.1
design_vision>
```

Console terminal

Design Vision - TopLevel.1 - [Hier.1]

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help

Logical Hierarchy

Cells (Hierarchical)

| Cell Name | Ref Name | Cell Path | Dont Touch |
|-----------|----------|-----------|------------|
|-----------|----------|-----------|------------|

Initializing gui preferences from file /home/giacomini/.synopsys_dv_prefs.tcl
dc_shell> gui_start
4.1
design_vision>

Log History

design_vision>

Ready

Hierarchy view

Design view

Log view

Command line