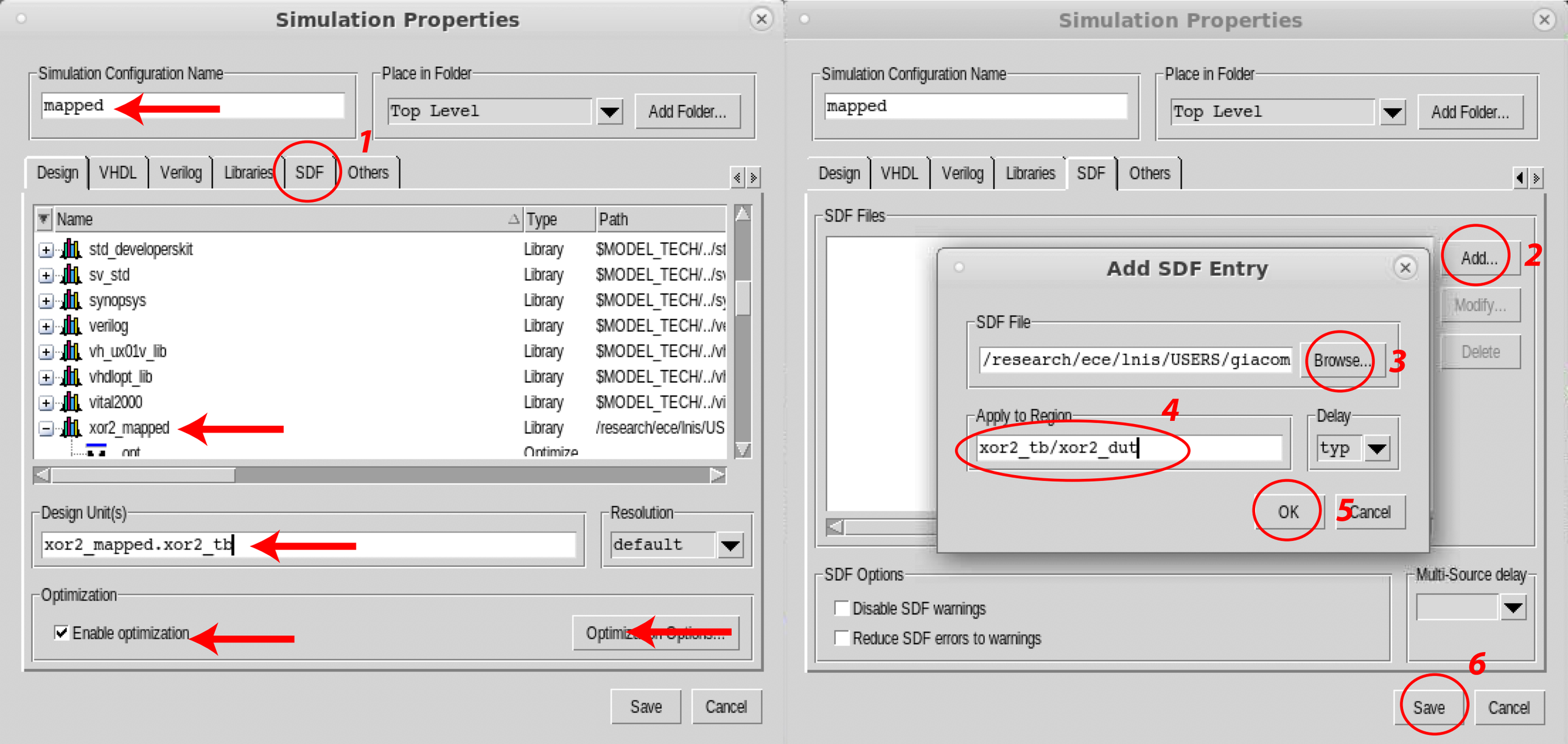
Simulation Properties
Simulation Configuration Name
mapped
Place in Folder
Top Level
Add Folder...
1
Design
VHDL
Verilog
Libraries
SDF
Others
Name
Type
Path
std_developerskit
Library
$MODEL_TECH/../st
sv_std
Library
$MODEL_TECH/../sv
synopsys
Library
$MODEL_TECH/../sy
verilog
Library
$MODEL_TECH/../ve
vh_ux01v_lib
Library
$MODEL_TECH/../vl
vhdlopt_lib
Library
$MODEL_TECH/../vl
vital2000
Library
$MODEL_TECH/../vi
xor2_mapped
Library
/research/ece/lnis/US
Optimize
Design Unit(s)
xor2_mapped.xor2_tb
Resolution
default
Optimization
Enable optimization
Optimization Options...
Save
Cancel
Simulation Properties
Simulation Configuration Name
mapped
Place in Folder
Top Level
Add Folder...
Design
VHDL
Verilog
Libraries
SDF
Others
SDF Files
Add...
2
Modify...
Delete
Add SDF Entry
SDF File
/research/ece/lnis/USERS/giacom
Browse...
3
Apply to Region
4
xor2_tb/xor2_dut
Delay
typ
OK
5
Cancel
SDF Options
Disable SDF warnings
Reduce SDF errors to warnings
Multi-Source delay
6
Save
Cancel