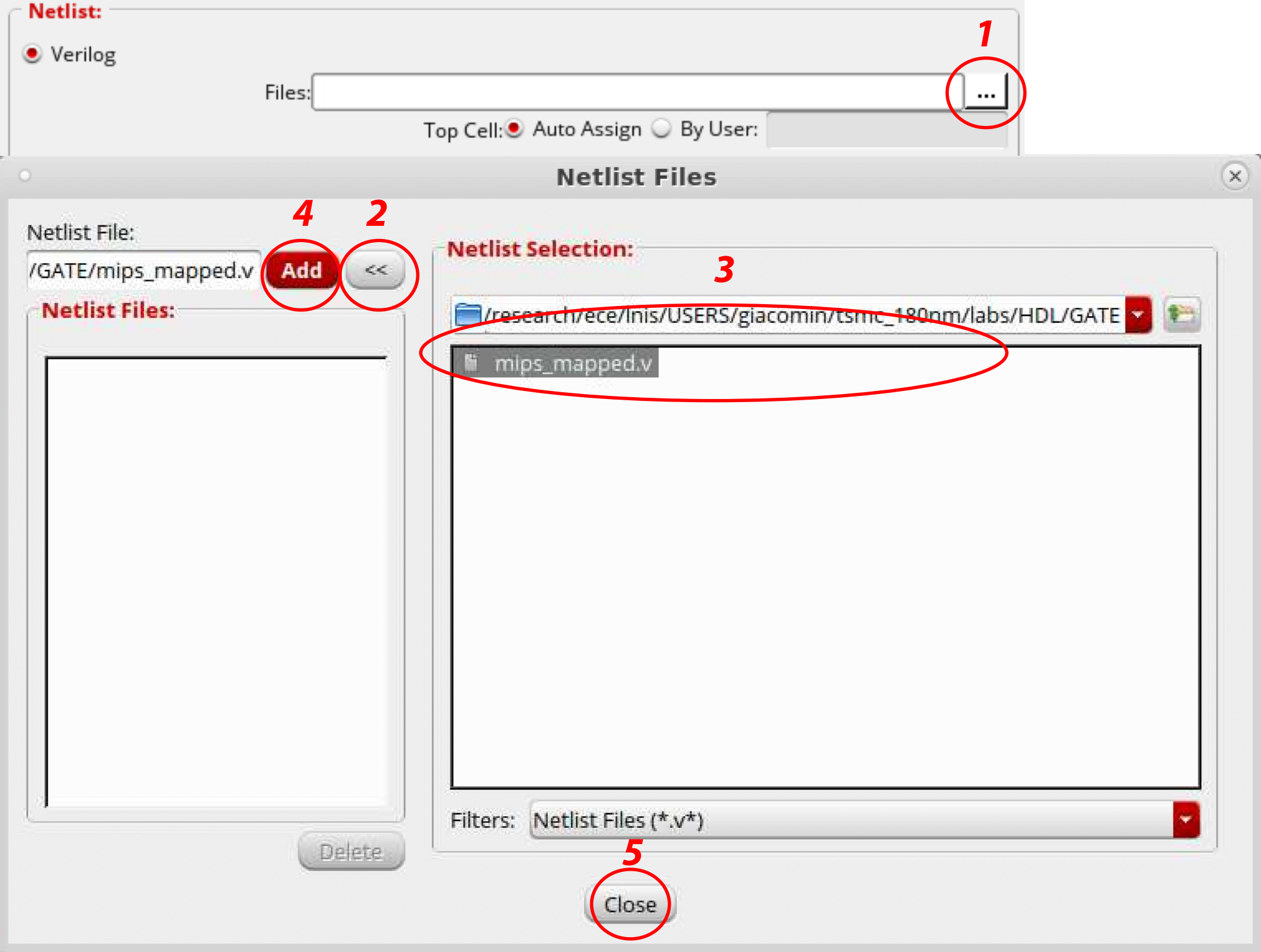
Netlist:
Verilog
Files:
...
1
Top Cell:
Auto Assign
By User:
Netlist Files
Netlist File:
/GATE/mips_mapped.v
Add
<<
4
2
Netlist Files:
Delete
Netlist Selection:
3
/research/ece/lnis/USERS/giacomin/tsmc_180nm/labs/HDL/GATE
mips_mapped.v
Filters:
Netlist Files (*.v*)
5
Close