



# ECE/CS 5710/6710 - Lab 3

## Design and Characterization of a D Flip-Flop

**Pre-lab Assignment:** Check for the date on Canvas.

**Lab Report:** Check for the date on Canvas.

### 1 Objective

In this lab, you will design a sequential circuit: a positive-edge triggered D flip-flop which is commonly used to build registers. You could use this cell in the future to design larger register banks such as an 8-bit register or a 16-word, 8-bit wide register. As for the previous lab, you will use industry standard tools (Cadence Virtuoso® for schematic and electrical simulations).

### 2 Pre-lab Assignment

Answer the following questions and submit a **.pdf** file through Canvas:

1. What is sequential logic and how different it is from combinational logic?
2. What is the difference between a latch and a flip-flop?
3. What is the difference between a positive and negative edge triggered flip-flop?
4. What are the setup and hold times for a sequential cell?

### 3 Specifications

Your DFF should have the following inputs:  $D$ ,  $CLK$ , the following output:  $Q$  as well as the  $vdd$  and  $gnd$  supply signals. It should be non-inverting: a 1 on D should result in a 1 on Q after the clock edge. The register should be positive-edge triggered. Remember that the goal here is to minimize the delay and the area of your cell (since it will be used in larger register banks) so some topologies might not be of interest.

**The goal of this lab is to have a DFF cell having a clock-to-Q delay (between signals  $CLK$  and  $Q$ ) less than **200ps**. We will also examine the effects of voltage scaling on a digital system.** Thus, you will need to optimize your design in order to meet timing constraints. Your final grade will depend on your report.

## 4 Lab Assignment

### 4.1 D Flip-Flop Electrical Characterization

In this first part, you will create the schematic, symbol and layout view of the DFF following the specifications. The DFF architecture to follow is the one from the textbook (figure 1.32 from Chapter 1 of the VLSI book), as shown below. You will then perform some electrical simulation to study its propagation delay and setup/hold times.

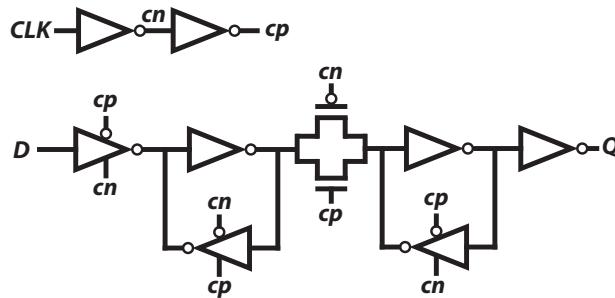


Figure 1: Schematic of the positive-edge triggered DFF.

1. Launch Virtuoso® and create a new schematic cell for your DFF. Do not forget to use the *nmos2v* and *pmos2v* cells from the *tsmc18* library for your transistors.
2. Create a new schematic cell for the testbench of your DFF. Keep in mind that you need to test the functionality of your DFF, how it latches its data and how it clears its value. Don't forget that since you need both *CLK* and *CLKB* signals, but only *CLK* is a pin of your cell, you will need an internal inverter in your DFF schematic. Don't forget to use a variable (*V<sub>DD</sub>*) when defining all your inputs (*D*, *CLK*) and power supply voltage sources, as was explained in Lab 2.
3. With complex cells, it is generally a good practice to set initial conditions in your testbench. In the DFF case, due to the feedback loop, the output *Q* may have an unknown value at the beginning of the simulation since no initial condition is set. As a result, you could observe a weird voltage value (which can be *V<sub>DD</sub>*/2 for instance). To avoid this and set an initial condition:
  - From the ADE window, go to: *Simulation -> Convergence Aids -> Initial Conditions...*
  - A new window should pop up, as shown in Fig. 2.
  - Simply click on the signal you want to set an initial condition on on your schematic (here *Q*) and click OK.

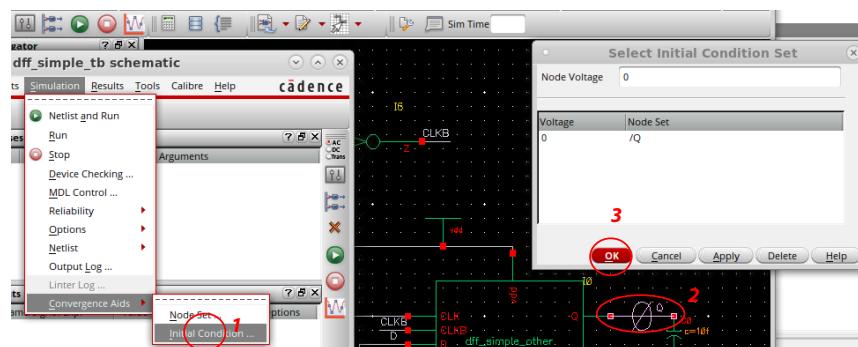


Figure 2: Specifying an initial condition for ADE.



For your testbenches, consider a period time of  $2n$  s, an output load for  $Q$  of  $10fF$  and an input slop of  $0.01 * \text{period}$ , as in the first lab.

### Assignment

- (a) Show the correct waveforms of your DFF demonstrating its correct functionality.
- (b) Report the propagation delay (between  $CLK$  and  $Q$  for both edges) as well as the falling and rising times of your DFF.

4. The next step is to measure the setup and hold times of your FF. The setup time is the propagation delay between  $D$  and  $CLK$  for which the propagation delay between  $CLK$  and  $Q$  starts increasing. The hold time is

- (a) Go back to your DFF testbench and make sure the  $D$  voltage source is parametrized. For instance, you can use the *vpwl* cell from the *analogLib* where you can define each point of the voltage pulse. In this example, we assume  $D$  is rising before  $CLK$  (so we only need to define 3 points for the  $d$  voltage source, as shown in Fig. 3). Here, we use the  $d_{delay}$  variable as the time at which input  $D$  will be rising.
- (b) Go back (or relaunch) to the ADE L window. Do not forget to re-import your design variable since you defined a new one ( $d_{delay}$ ). Set the  $d_{delay}$  value to 1ns.
- (c) Define 2 new expressions, as explained in the previous labs:  $t\_D\_CLK$  for the propagation delay between  $D$  and  $CLK$  and  $t\_CLK\_Q$  for the propagation delay between  $CLK$  and  $Q$ .
- (d) Launch the simulation and make sure that your setup is correct (it should look like Fig. 4).
- (e) For the setup time, assume that the  $CLK$  is fixed and is the reference time. The signal  $D$  arrives infinitely early and you measure the  $t\_CLK\_Q$  delay. Now, you need to increase the time at which  $D$  is rising (meaning  $t\_D\_CLK$  will decrease) and see when for which  $t\_D\_CLK$  (this will be your setup time) the  $t\_CLK\_Q$  delay starts increasing. To do so, launch a parametric analysis, and sweep the  $d_{delay}$  value from  $1.5n$  to  $2n$ , with 10 steps.
- (f) You should obtain something like Fig. 5. As you can see, when the delay between  $D$  and  $CLK$  decreases too much (this is the setup time), the delay between  $CLK$  and  $Q$  increases.

CDF Parameter	Value
Frequency name for 1/period	
Number of pairs of points	3
Time 1	0 s
Voltage 1	0 V
Time 2	$d_{delay}$ s
Voltage 2	0 V
Time 3	$d_{delay}+0.01*\text{period}$ s
Voltage 3	VDD V
Noise file name	
Number of noise/freq pairs	0
DC voltage	

Figure 3:  $D$  voltage source parameters for setup time measurement.

- (g) Do a similar analysis for the hold time. It is suggested create a new testbench for the hold time so you don't mix things (you can simply copy the setup for the hold time and changes things accordingly). Define 2 new expressions:  $t_{CLK\_D}$  for the propagation delay between  $CLK$  and  $D$  and  $t_{CLK\_Q}$  for the propagation delay between  $CLK$  and  $Q$ . The hold time is the dual of the setup time. For this case, you assume that signal  $D$  arrives infinitely early before the rising edge of  $CLK$  (to make sure there is no setup time violation). Signal  $D$  switches again after the rising edge of  $CLK$  and you can measure  $t_{CLK\_Q}$ , as shown in Fig. 4. Then, you need to decrease the time after which  $D$  switches (meaning  $t_{CLK\_D}$  is decreasing since  $D$  is moved closer to the rising edge of  $CLK$ ). The  $t_{CLK\_D}$  for which  $t_{CLK\_Q}$  starts increasing is your hold time. Keep in mind that you need to modify the source voltage for  $D$  accordingly.

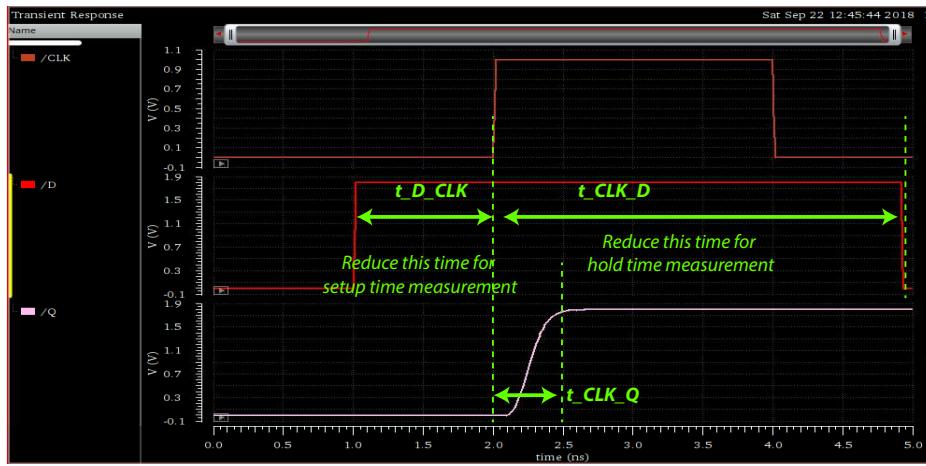


Figure 4: DFF output curves for setup and hold time measurements.

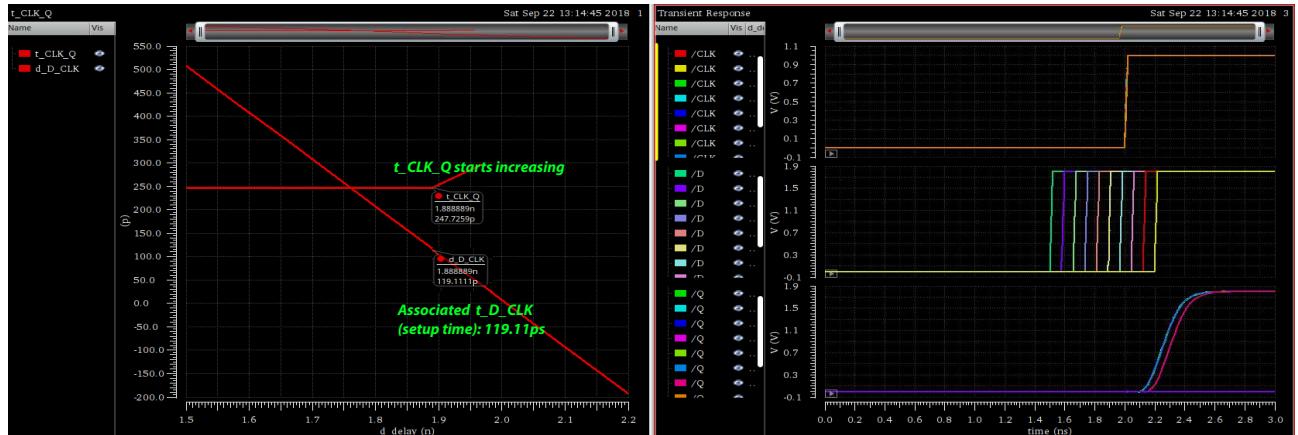


Figure 5: Parametric analysis for setup time measurement.

### Assignment

Report the setup and hold times of your DFF as well as the associated curves.

5. Now, we will examine how voltage scaling impacts  $t_{CLK\_Q}$ . In either of your setup time or hold time testbenches, create a parametric sweep for  $V_{DD}$ . To measure  $t_{CLK\_Q}$ , you might need to modify its equation to ensure that the threshold values are not defined as 0.9V but as a variable dependent on  $V_{DD}$ , as shown in Fig. 6.



Figure 6: Setting threshold values as a function of  $V_{DD}/2$  in the calculator.

### Assignment

- Plot  $t_{CLK\_Q}$  vs  $V_{DD}$ . Note down the  $V_{DD}$  value where  $t_{CLK\_Q}$  becomes 20% longer than  $t_{CLK\_Q}$  at 1.8 V.
- Repeat step 4 with the  $V_{DD}$  value where  $t_{CLK\_Q}$  becomes 20% longer. Comment on the changes you saw on the setup and hold times.
- How does an increase in  $t_{CLK\_Q}$  impact a sequential circuit (for example the counter shown in homework 1)?

## 4.2 4-bit Register Simulation

Create a new schematic and symbol for an 4-bit register. You will need to simulate the shift register with a clock speed of 500 MHz, a pulse data input similar to figure 4, voltage supply of 1.8V and the voltage found in previous exercise.

### 4.2.1 Power Consumption Calculation

To calculate the power of a circuit in ADE®, we can use the current information from transient and DC analyses. To do so:

- In your ADE L® window, create a new DC analysis. Select *DC*, and check *Save DC Operating Point* and click *OK*, as shown in Fig. 7 (a). You now should have 2 analyses in your ADE L® window (*trans* and *dc*), as illustrated in Fig. 7 (b).
- Then, define an equation to multiply  $V_{DD}$  by the average of the current draining from the power supply. To do so, choose *it* from the calculator and click on the top terminal (red square) of the power supply voltage source on your schematic. You should see *IT('/V1/PLUS')* in the calculator.
- In *function panel*, choose the *average* function and send it to the calculator to calculate the average of the current.
- Then, choose *vdc* from the calculator and click on the net connected to the power supply on the schematic.
- Finally, choose multiply (\*) from the key pad to multiply the average of current and the  $V_{DD}$  voltage which was stored in the stack. Your final equation should look like *VDC('/vdd!')\*average(IT('/V1/PLUS'))*. These steps are illustrated in Fig. 8.

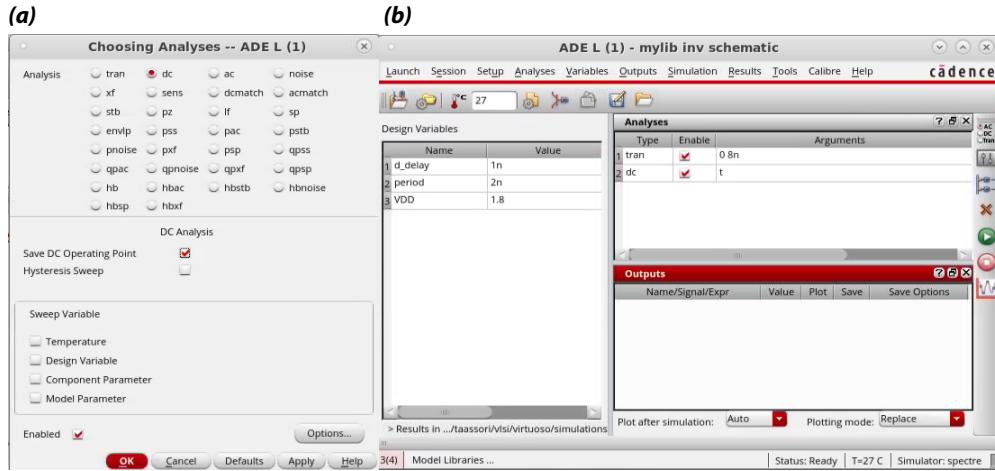


Figure 7: (a) Choosing the DC analysis; (b) ADE windows after choosing DC and AC analysis.

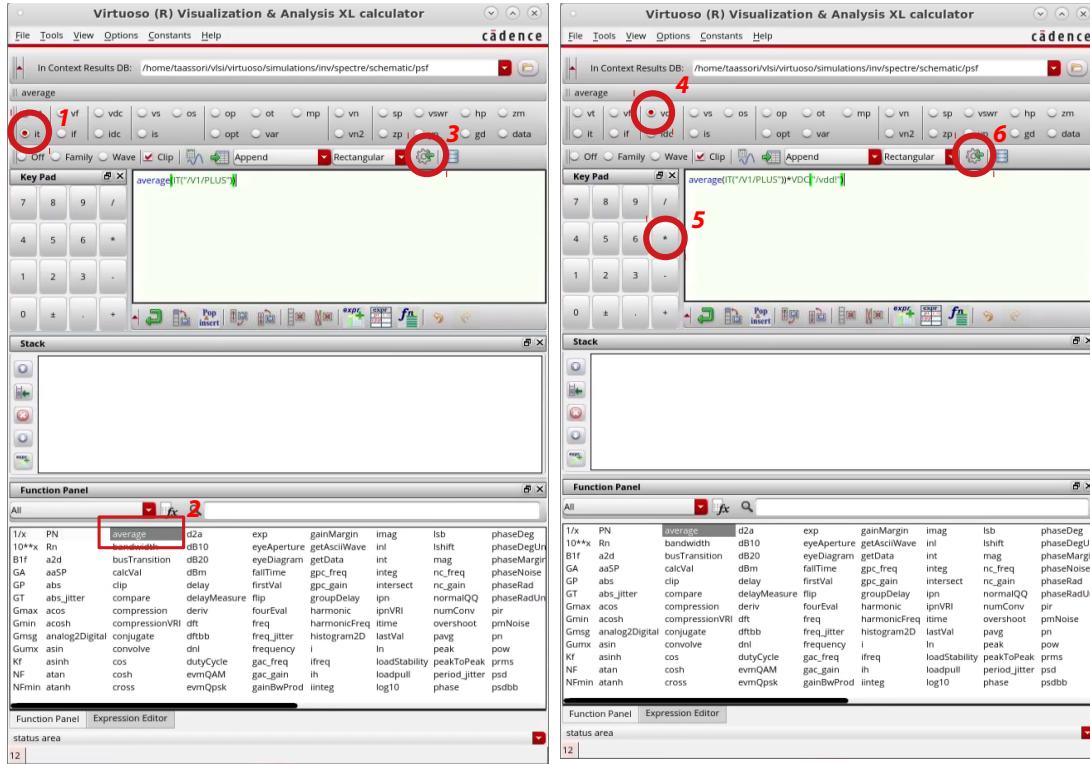


Figure 8: Adding the power equation into the calculator.

## Assignment

- Provide a screenshot of your 4-bit register outputs.
- Compare the power consumption using two different  $V_{DD}$  values.

3. Comment on the advantages and disadvantages of using a lower voltage supply in a system. Is it possible to use multiple power supply in a large system? Justify your answer.

## 5 Assignment Summary

Write a report and answer the assignments asked during the lab, which are summarized below.

### Assignments

1. Show the correct waveforms of your DFF demonstrating its correct functionality.
2. Report the propagation delay (between  $CLK$  and  $Q$  for both edges) as well as the falling and rising times of your DFF.
3. Report the setup and hold times of your DFF as well as the associated curves.
4. Plot  $t_{CLK\_Q}$  vs  $VDD$ . Note down the  $VDD$  value where  $t_{CLK\_Q}$  becomes 20% longer than  $t_{CLK\_Q}$  at 1.8 V.
5. Repeat step 4 with the  $VDD$  value where  $t_{CLK\_Q}$  becomes 20% longer. Comment on the changes you saw on the setup and hold times.
6. How does an increase in  $t_{CLK\_Q}$  impact a sequential circuit (for example the counter shown in homework 1)?
7. Provide a screenshot of your 4-bit register outputs.
8. Compare the power consumption using two different  $VDD$  values.
9. Comment on the advantages and disadvantages of using a lower voltage supply in a system. Is it possible to use multiple power supply in a large system? Justify your answer.