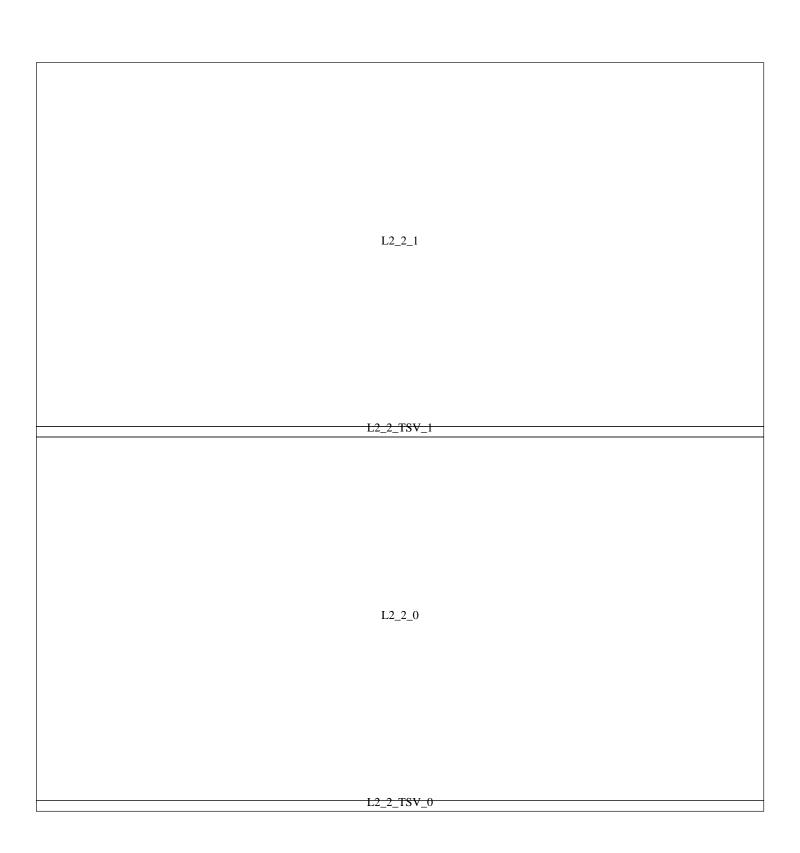
L2	_1_1
12.1	TSV_1
L2_1_	157_1
1.2.	_1_0
L2	_1_0
1.2.	_1_0
L2	_1_0
L2	_1_0
L2.	_1_0
L2	_1_0
L2.	_1_0
	_1_0

TIM_unit_1
TIM_tsv_1
111/1_13/_1
111/1_6/_1
111/1_6/_1
111/1_63/_1
111V1_03V_1
THV_6,1
THV_6, 1
THV_6, 1
THV_6, V_1
THV_60V_1
THV_0,
TIM_unit_0



TIM_unit_1
TIM_tsv_1
111/1_13/_1
111/1_6/_1
111/1_6/_1
111/1_63/_1
111V1_03V_1
THV_6,1
THV_6, 1
THV_6, 1
THV_6, V_1
THV_60V_1
THV_0,
TIM_unit_0

	FPMap_0_2		IntMap_2	IntQ_2	IntReg_0	_2ntReg_1_2	FPMap_0_3		IntMap_3	IntQ_3	IntReg_0	_3ntReg_1_3	
FF	FPMul_0_2 RegFORegFF FPAdd_0_2	RegFT Reg	3_2 FPQ_2	LdStQ_2		IntExec_2 FP		FPMul_1_3 RegFPReg_ FPAdd_1_3	FPQ_3	LdStQ_3		IntExec_3	
	Bpred_0_2	Bpred_1_2			DTB_1_2	DTB_2_2	Bpred_0_3	Bpred_1_3		DTB_0_3	DTB_1_3	DTB_2_3	
	Icache_2 Dcache_2				Icache_3			Dcache_3					
		T	TS	V_2				ı	TS	V_3			
	FPMap_0_0 FPMul_0_0		IntMap_0	IntQ_0	IntReg_0	_0ntReg_1_0	FPMul 0 1	FPMap_1_1 FPMul_1_1	_IntMap_1	IntQ_1	IntReg_0	_IntReg_1_1	
FP	RegF@RegFI FPAdd_0_0	RegFP Reg	3_0 FPQ_0	LdStQ_0		Exec_0 FF	RegFØRegFI		3_1 FPQ_1	LdStQ_1		Exec_1	
	Bpred_0_0	Bpred_1_0	Bpred_2_0	DTB_0_0	DTB_1_0	DTB_2_0	Bpred_0_1	Bpred_1_1	Bpred_2_1	DTB_0_1	DTB_1_1	DTB_2_1	
		Icache_0	TS	Dcache_0 		Icache_1			Dcache_1				

