88W8782

WLAN SoC

IEEE 802.11n/a/g/b

Datasheet

SDK Use Only

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Document Conventions

	**Note:** Provides related information or information of special importance.
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PRODUCT OVERVIEW

The Marvell® 88W8782 is a highly integrated wireless local area network (WLAN) system-on-chip (SoC), specifically designed to support high throughput data rates for next generation WLAN products. The device is designed to support IEEE 802.11a/g/b and 802.11n payload data rates.

The device provides the combined functions of Direct Sequence Spread Spectrum (DSSS) and Orthogonal Frequency Division Multiplexing (OFDM) baseband modulation, Medium Access Controller (MAC), CPU, memory, host interfaces, and direct conversion WLAN RF radio on a single integrated chip.

For security, the 88W8782 supports 802.11i security standards through implementation of the Advanced Encryption Standard (AES)/Counter Mode CBC-MAC Protocol (CCMP), Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP), Advanced Encryption Standard (AES)/Cipher-Based Message Authentication Code (CMAC), and WLAN Authentication and Privacy Infrastructure (WAPI) security mechanisms.

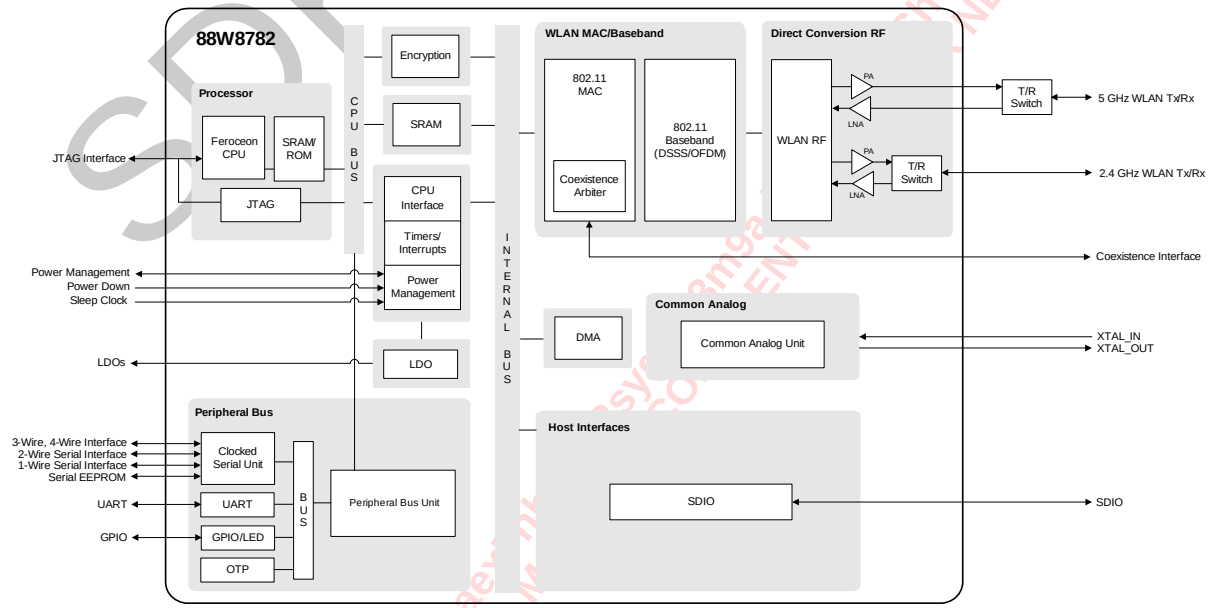
For video, voice, and multimedia applications, 802.11e Quality of Service (QoS) is supported. Also supported are 802.11h Dynamic Frequency Selection (DFS) for detecting radar pulses when operating in the 5 GHz range.

The device is also equipped with a coexistence interface for external, co-located 2.4 GHz radios.

The 88W8782 supports a SDIO interface for connecting WLAN activity to the host processor. The device is available in a QFN package option.

Figure 1 shows an overall block diagram of the device.

Figure 1: Top Block Diagram



Applications

- Imaging platforms (printers, digital picture frames)
- Gaming platforms
- Consumer electronic devices (TV, DVD players, Blu-ray players, etc.)

General Features

- Single-chip integration of 802.11 wireless radio, baseband, MAC, CPU, memory, host interface
- CMOS and low-swing sinewave input clock
- 26, 38.4, 40, and 44 MHz crystal clock support with auto-frequency detection if external sleep clock is available
- Low power operation supporting deep sleep and standby modes
- Power management with external sleep clock support for near zero deep sleep power
- Option to power directly from battery or to use 3.3V/1.8V/1.2V pre-regulated supplies
- One time programmable (OTP) memory to eliminate need for external EEPROM
- Fully compatible with Marvell Power Management device(s)

IEEE 802.11/Standards

- 802.11 data rates of 1 and 2 Mbps
- 802.11b data rates of 5.5 and 11 Mbps
- 802.11a/g data rates 6, 9, 12, 18, 24, 36, 48, and 54 Mbps for multimedia content transmission
- 802.11g/b performance enhancements
- 802.11n compliant, with maximum data rates up to 72 Mbps (20 MHz channel) and 150 Mbps (40 MHz channel)
- 802.11d international roaming
- 802.11e QoS block acknowledgement (with support for 802.11n extension)
- 802.11h transmit power control
- 802.11h DFS radar pulse detection
- 802.11i enhanced security
- 802.11k radio resource measurement
- 802.11r fast hand-off for AP roaming
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode
- Wi-Fi Direct connectivity

Packaging

- QFN

Processor

CPU

- Integrated Marvell Feroceon® CPU (ARMv5TE-compliant)
- 128 MHz maximum CPU clock speed

DMA

- Independent 2-Channel Direct Memory Access (DMA)

Memory

- Internal SRAM for Tx frame queues/Rx data buffers
- Boot ROM
- ROM patching capability

WLAN MAC

- Ad-Hoc and Infrastructure Modes
- RTS/CTS for operation under DCF
- Hardware filtering of 32 multicast addresses and duplicate frame detection for up to 32 unicast addresses
- On-chip Tx and Rx FIFO for maximum throughput
- Open System and Shared Key Authentication services
- A-MPDU Rx (de-aggregation) and Tx (aggregation)
- 20/40 MHz coexistence
- Reduced Inter-Frame Spacing (RIFS) bursting
- Management information base counters
- Radio resource measurement counters
- Block acknowledgement with 802.11n extension
- Dynamic frequency selection (DFS)
- Transmit beamformee support
- Transmit rate adaptation
- Transmit power control
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames
- Marvell Mobile Hotspot

WLAN Baseband

- 802.11n 1x1 SISO (on-chip Marvell SISO RF radio)
- Backward compatibility with legacy 802.11a/g/b technology
- PHY data rates up to 150 Mbps
- 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz bandwidth in 40 MHz channel, and 20 MHz duplicate legacy bandwidth in 40 MHz channel mode operation
- Modulation and Coding Scheme (MCS)—0~7 and 32 (duplicate 6 Mbps)
- Enhanced radar detection for long and short pulse radar
- Enhanced AGC scheme for DFS channel
- Japan DFS requirements for W53 and W56
- Radio resource measurement
- Optional 802.11n SISO features:
  - 20/40 MHz coexistence
  - 1-stream STBC reception
  - Short guard interval
  - RIFS on receive path
  - Beamformee function and hardware acceleration
  - Greenfield Tx/Rx
- Power save features

WLAN Radio

- Integrated direct conversion radio
- 20 and 40 MHz channel bandwidths
- Integrated T/R switch, PA, and LNA for 2.4 GHz path
- Integrated PA and LNA for 5 GHz path

WLAN Rx Path

- Direct conversion architecture eliminates need for external SAW filter
- On-chip gain selectable LNAs with optimized noise figure and power consumption
- High dynamic range AGC function in receive mode

WLAN Tx Path

- Integrated power amplifiers with power control
- Closed/open loop power control (0.5 dB increments)
- Optimized Tx gain distribution for linearity and noise performance

WLAN Local Oscillator

- Fractional-N for multiple reference clock support
- Fine channel step, AFC (adaptive frequency control)

WLAN Encryption

- WEP 64- and 128-bit encryption with hardware TKIP processing (WPA)
- AES-CCMP hardware implementation as part of 802.11i security standard (WPA2)
- Enhanced AES engine performance
- AES-Cipher-Based Message Authentication Code (CMAC) as part of the 802.11w security standard
- WLAN Authentication and Privacy Infrastructure (WAPI)

Coexistence

- Coexistence interface for external, co-located 2.4 GHz radio
  - Marvell 3/4-wire interface
  - WL_ACTIVE 3/4-wire interface
  - WL_ACTIVE 2-wire interface

Host Interface

- SDIO device interface (SPI, 1-bit SDIO, 4-bit SDIO transfer modes at full clock range up to 50 MHz)

Peripheral Bus Interfaces

- Clocked Serial Unit (CSU)
  - 3-Wire, 4-Wire Serial Interface
  - 2-Wire Serial Interface
  - 1-Wire Serial Interface
  - SPI EEPROM Interface
- 16550 UART
- General Purpose Input Output (GPIO)
- OTP memory to eliminate need for external EEPROM

Test

- On-chip diagnostic information

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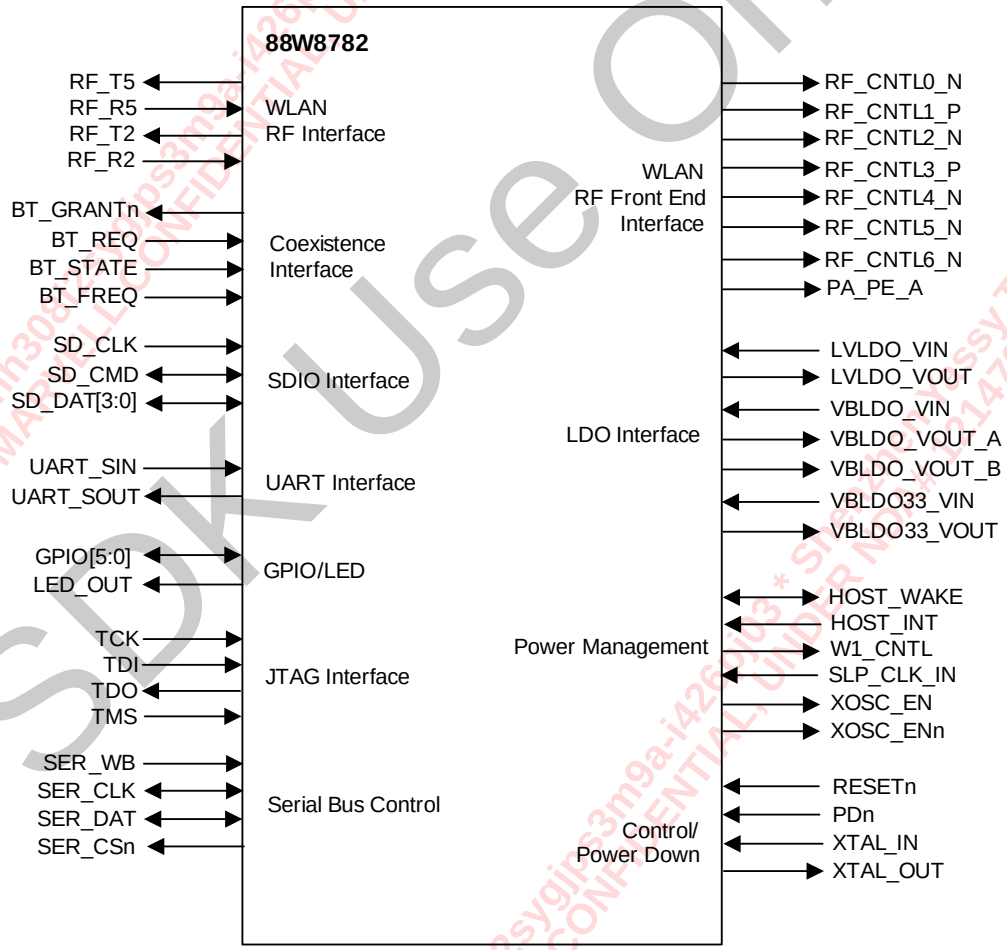
1 Package and Power

1.1 Signal Diagram

Figure 1 shows a list of the functional signals for the device.

Figure 1: Signal Diagram[1]

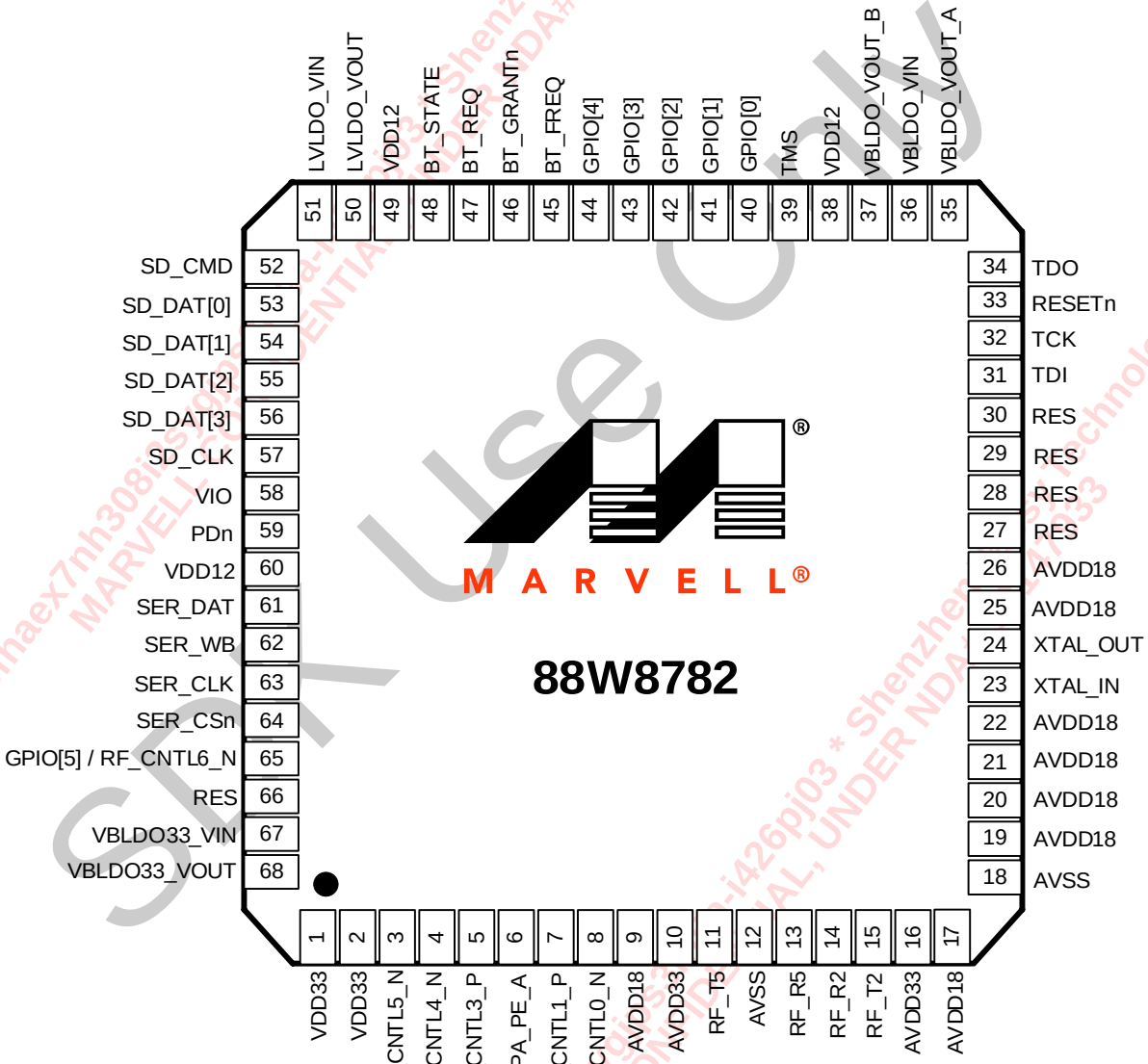


1. See Section 1.2, Pinout, on page 18 for dedicated signal and pin descriptions.

1.2 Pinout

1.2.1 Pinout—QFN

Figure 2: Pinout—QFN



1.2.2 Mechanical Drawing—QFN

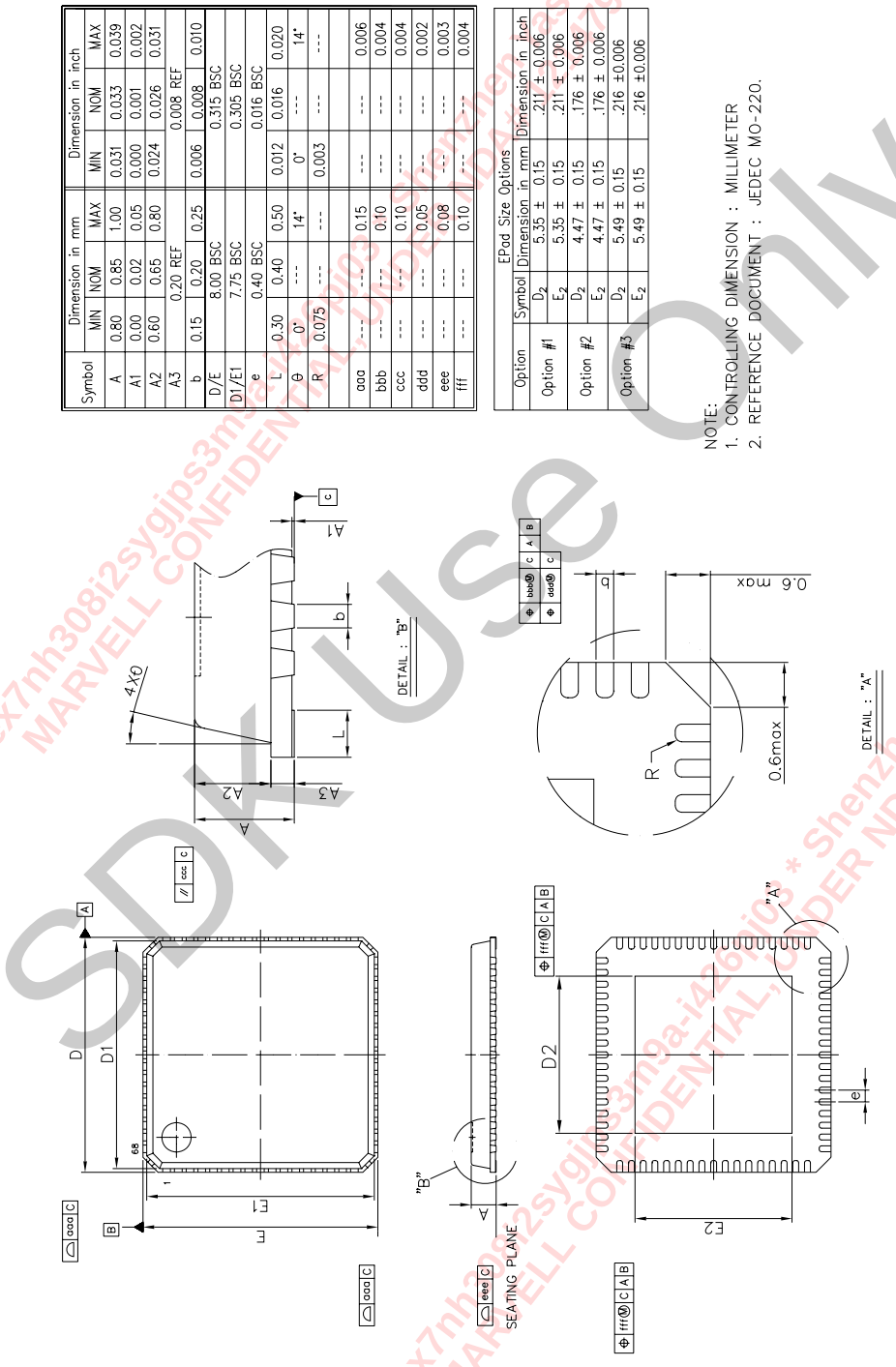


Figure 3: Mechanical Drawing—QFN[1]

1. QFN package uses Epad size Option #3 only.

1.3 Pin Description

Table 1: Pin Types

Pin Type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A, O	Analog output

Table 2: WLAN RF Interface

QFN Pin No.	Pin Name	Type	Supply	Description
11	RF_T5	A, O	AVDD33	Transmitter RF Output—5 GHz Baseband output data
13	RF_R5	A, I	AVDD18	Receiver RF Input—5 GHz Baseband input data
15	RF_T2	A, O	AVDD33	Transmitter RF Output—2.4 GHz Baseband output data
14	RF_R2	A, I	AVDD18	Receiver RF Input—2.4 GHz Baseband input data

Table 3: WLAN RF Front-End Control Interface

QFN Pin No.	Pin Name	Supply	No Pad Power State	RESET State	HW[1] State	PD[2] State	Internal PU	PU[3]	PD[3]
8	RF_CNTL0_N	VDD33	tristate	output	output	output low	weak PU enable	no	no
RF Control 0— Power Down Output Low									
7	RF_CNTL1_P	VDD33	tristate	input	output	output high	weak PU enable	no	no
RF Control 1—Power Down Output High									
6	RF_CNTL2_N/ PA_PE_A	VDD33	tristate	output	output	output low	weak PU enable	no	no
RF Control: RF Control 2—Power Down Output Low **PA Power Enable**: 5 GHz Controls the power amplifier enable input. 0 = disable 1 = enable									
5	RF_CNTL3_P	VDD33	tristate	input	output	output high	weak PU enable	no	no
RF Control 3—Power Down Output High									
4	RF_CNTL4_N	VDD33	tristate	input	output	output low	weak PU enable	no	no
RF Control 4—Power Down Output Low									
3	RF_CNTL5_N	VDD33	tristate	input	output	output low	weak PU enable	no	no
RF Control 5—Power Down Output Low									
65	GPIO[5]/ RF_CNTL6_N								
RF Control: RF Control 6—Power Down Output Low **GPIO**: GPIO[5]—see Table 7, p. 24 for pin state/supply information.									

1. Hardware default state after reset
2. Power down
3. Programmable pull-up/pull-down

Table 4: Power Down Interface

QFN Pin No.	Pin Name	Supply	No Pad Power State	RESET State	HW[1] State	PD[2] State	Internal PU	PU[3]	PD[3]
33	RESETn	VIO	tristate	input low	input high	tristate	nominal PU enable	no	no
Reset (active low)									
59	PDn	VIO	tristate	input high	input high	input low	none	n/a	n/a
Full Power Down (active low) 0 = full power down mode 1 = normal mode • Connect to power down pin of host or 1.8V • External host required to drive this pin high for normal operation • No internal pull-up on this pin									

1. Hardware default state after reset
2. Power down
3. Programmable pull-up/pull-down

Table 5: Clock Interface

QFN Pin No.	Pin Name	Type	Supply	Description
23	XTAL_IN	A, I	AVDD18	Crystal / Crystal Oscillator / System Clock Input Accepts 26/38.4/40/44 MHz clock signals from a crystal oscillator (frequency stability ±20 ppm). See Section 7.6, Clock Specifications, on page 98.
24	XTAL_OUT	A, O	AVDD18	Crystal / Crystal Oscillator Output **NOTE: Connect this pin to ground when an external oscillator is used.**

Table 6: Host Interface

QFN Pin No.	Pin Name	Supply	No Pad Power State	RESET State	HW[1] State	PD[2] State	Internal PU	PU[3]	PD[3]
57	SD_CLK	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
SDIO 4-bit Mode: Clock input **SDIO 1-bit Mode**: Clock input **SDIO SPI Mode**: Clock input									
52	SD_CMD	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
SDIO 4-bit Mode: Command/response (input/output) **SDIO 1-bit Mode**: Command line **SDIO SPI Mode**: Data input									
53	SD_DAT[0]	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
SDIO 4-bit Mode: Data line Bit[0] **SDIO 1-bit Mode**: Data line **SDIO SPI Mode**: Data output									
54	SD_DAT[1	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
SDIO 4-bit Mode: Data line Bit[1] **SDIO 1-bit Mode**: Interrupt **SDIO SPI Mode**: InterruptSDO is tristate when SCSn is inactive. Enables multiple devices driving SDO line.									
55	SD_DAT[2	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
SDIO 4-bit Mode: Data line Bit[2] or read wait (optional) **SDIO 1-bit Mode**: Read wait (optional) **SDIO SPI Mode**: Reserved									
56	SD_DAT[3]	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
SDIO 4-bit Mode: Data line Bit[3] **SDIO 1-bit Mode**: Reserved **SDIO SPI Mode**: Card select (active low)									

1. Hardware default state after reset
2. Power down
3. Programmable pull-up/pull-down

Table 7: Multi-Purpose Interface

QFN Pin No.	Pin Name	Supply	No Pad Power State	RESET State	HW[1] State	PD[2] State	Internal PU	PU[3]	PD[3]
65	GPIO[5]/ RF_CNTL6_N	VIO	tristate	input	output	tristate	weak PU enabled	no	no
GPIO Mode: GPIO[5] **Functional Mode**: W1_CNTL (output) Power management device programming interface control. **Oscillator Mode**: XOSC_ENn (output, active low) 0 = enable external oscillator 1 = disable external oscillator **RF Mode**: RF_CNTL6_N									
44	GPIO[4]	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
GPIO Mode: GPIO[4] GPIO interrupt input **Host Wakeup**: Host-to-SoC Wakeup (input)									
43	GPIO[3]	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
GPIO Mode: GPIO[3] **UART Mode**: UART_SIN (input) **Functional Mode**: W1_CNTL (output) Power management device programming interface control. **Interrupt:** Host Interrupt (input) **Power Management**: Sleep Clock Input (SLP_CLK_IN) External sleep clock of 32.768 KHz must be used for auto reference clock calibration.									
42	GPIO[2]	VIO	tristate	input	output	tristate	weak PU enable	no	no
GPIO Mode: GPIO[2] **UART Mode**: UART_SOUT (output) **Host Wakeup**: SoC-to-Host Wakeup (output)									
41	GPIO[1]	VIO	tristate	input	input	tristate	weak PU enable	no	no
GPIO Mode: GPIO[1] **LED Mode**: LED_OUT (output)									
40	GPIO[0]	VIO	tristate	output	output	output low	disabled	no	no
GPIO Mode: GPIO[0] **Oscillator Mode**: XOSC_EN (output, active high) 0 = disable external oscillator 1 = enable external oscillator									

1. Hardware default state after reset
2. Power down

3. Programmable pull-up/pull-down

Table 8: EEPROM/TWSI Interface

QFN Pin No.	Pin Name	Supply	No Pad Power State	RESET State	HW[1] State	PD[2] State	Internal PU	PU[3]	PD[3]
62	SER_WB	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
SPI EEPROM Mode: Serial Interface Data (input) Serial data from EEPROM to SoC **TWSI EEPROM Mode**: Not used									
63	SER_CLK	VIO	tristate	input	output	tristate	weak PU enable	no	no
SPI EEPROM Mode: Serial Interface Clock (output) Serial clock from SoC to EEPROM **TWSI EEPROM Mode**: Serial interface clock (input/output)									
61	SER_DAT	VIO	tristate	output	output	tristate	nominal PU enable	yes	yes
SPI EEPROM Mode: Serial Interface Data (output) Serial data from SoC to EEPROM **TWSI EEPROM Mode**: Serial interface data (input/ouput)									
64	SER_CSn	VIO	tristate	input	output	tristate	weak PU enable	no	no
SPI EEPROM Mode: EEPROM Chip Select (output) Chip select from SoC to EEPROM **TWSI EEPROM Mode**: Not used									

1. Hardware default state after reset
2. Power down
3. Programmable pull/up-pull-down

Table 9: Bluetooth Coexistence Interface

QFN Pin No.	Pin Name	Supply	No Pad Power State	RESET State	HW[1] State	PD[2] State	Internal PU	PU[3]	PD[3]
46	BT_GRANTn	VIO	tristate	input	input	tristate	weak PU enable	no	no
47	BT_REQ	VIO	tristate	input	input	tristate	disabled	yes	yes
48	BT_STATE	VIO	tristate	input	input	tristate	disabled	yes	yes
45	BT_FREQ	VIO	tristate	input	input	tristate	disabled	yes	yes

1. Hardware default state after reset
2. Power down
3. Programmable pull-up/pull-down

Table 10: JTAG Interface

QFN Pin No.	Pin Name	Supply	No Pad Power State	RESET State	HW[1] State	PD[2] State	Internal PU	PU[3]	PD[3]
32	TCK	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
31	TDI	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
34	TDO	VIO	tristate	input	input	tristate	weak PU enable	no	no
39	TMS	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes

1. Hardware default state after reset
2. Power down
3. Programmable pull-up/pull-down

Table 11: Power and Ground

QFN Pin No.	Pin Name	Type	Description
38 60	VDD12	Power	1.2V Digital Core Power Supply
58	VIO	Power	1.8/2.6V/3.3V Digital I/O Power Supply
1 2	VDD33	Power	3.0/3.3V Digital I/O Power Supply
9 17 19 20 21 22 25 26	AVDD18	Power	1.8V Analog Power Supply
10 16	AVDD33	Power	3.3V Analog Power Supply
51	LVLDO_VIN	Power	1.8V LV LDO Voltage Input
50	LVLDO_VOUT	Power	1.2V LV LDO Voltage Output
36	VBLDO_VIN	Power	3.3V VBAT Voltage Input
35	VBLDO_VOUT_A	Power	1.8V VBAT Voltage Output
37	VBLDO_VOUT_B	Power	1.8V VBAT Voltage Output
67	VBLDO33_VIN	Power	3.6V VBAT Voltage Input
68	VBLDO33_VOUT	Power	3.3V VBAT Voltage Output
12 18	AVSS	Ground	Ground
27 28 29 30 66	RES	--	Reserved Do not connect these pins. Leave these pins floating.

1.3.1 Power Options

The 88W8782 can be powered from the following:

- Power Option A—Internal 1.2V, External 1.8V, External 3.3V, LDOs Enabled: LVLDO
  - VIO connected from host
  - VIO is 3.3V
  - Internal 1.2V supply
  - External 1.8V supply
  - External 3.3V supply (from SDIO host)
  - LDOs enabled—LVLDO
- Power Option B—Internal 1.2V, External 1.8V, Internal 3.3V, LDOs Enabled: LVLDO, VBLDO33
  - VIO connected from host
  - Internal 1.2V supply
  - External 1.8V supply
  - Internal 3.3V supply
  - LDOs enabled—LVLDO, VBLDO33
- Power Option C—Internal 1.2V, Internal 1.8V, Internal 3.3V, LDOs Enabled: LVLDO, VBLDO, VBLDO33
  - VIO connected from host
  - Internal 1.2V supply
  - Internal 1.8V supply
  - Internal 3.3V supply
  - LDOs enabled—LVLDO, VBLDO, VBLDO33

Each of these options have requirements that must be met, as outlined in the following sections. If these requirements cannot be met, see Section 1.3.2, Alternate Power Up Sequence, on page 35 for an alternative power up sequence.

- Figure 10, Alternate Option A—Internal 1.2V, External 1.8V, External 3.3V, LDOs Enabled: LVLDO, on page 35
- Figure 11, Alternate Option B—Internal 1.2V, External 1.8V, Internal 3.3V, LDOs Enabled: LVLDO, VBLDO33, on page 36
- Figure 12, Alternate Option C—Internal 1.2V, Internal 1.8V, Internal 3.3V, LDOs Enabled: LVLDO, VBLDO, VBLDO33, on page 37

1.3.1.1 Power Option A—Internal 1.2V, External 1.8V, External 3.3V, LDOs Enabled: LVLDO

The following requirements must be met for correct power up:

- External 3.3V supply (EXT_VDD33) to VIO, VDD33, and AVDD33 must be stable before external 1.8V supply (EXT_VDD18) starts ramping up
- Ramp-up time of EXT_VDD18 T1 must be less than 240 µs
- Output load on VDD12 should be 1–10 µF. Ramp-up time of VDD12 T2 will be at least 100 µs for this load condition.
- If an external oscillator is used, XTAL_IN must be stable before VDD12 starts ramping up
- If an external sleep clock is used, clock frequency of 32.768 KHz must be used and must be stable before VDD12 starts ramping up
- PDn and RESETn are deasserted
- VBLDO and VBLDO33 must be powered down to save leakage power
- Figure 4 shows the LDO connections
- Figure 5 shows the power up sequence

Figure 4: Power Option A—LDO Connections

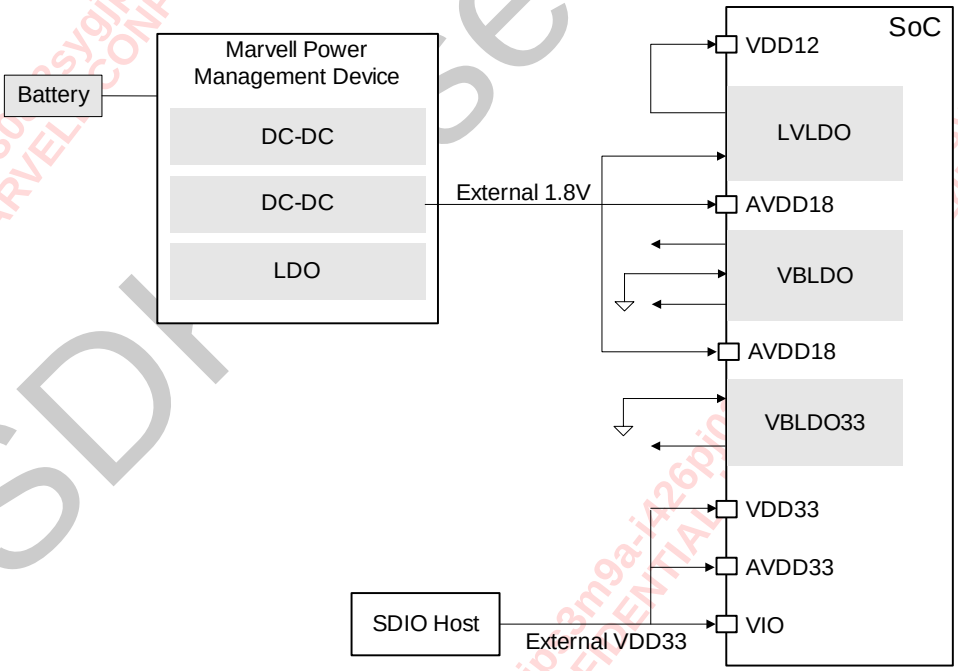
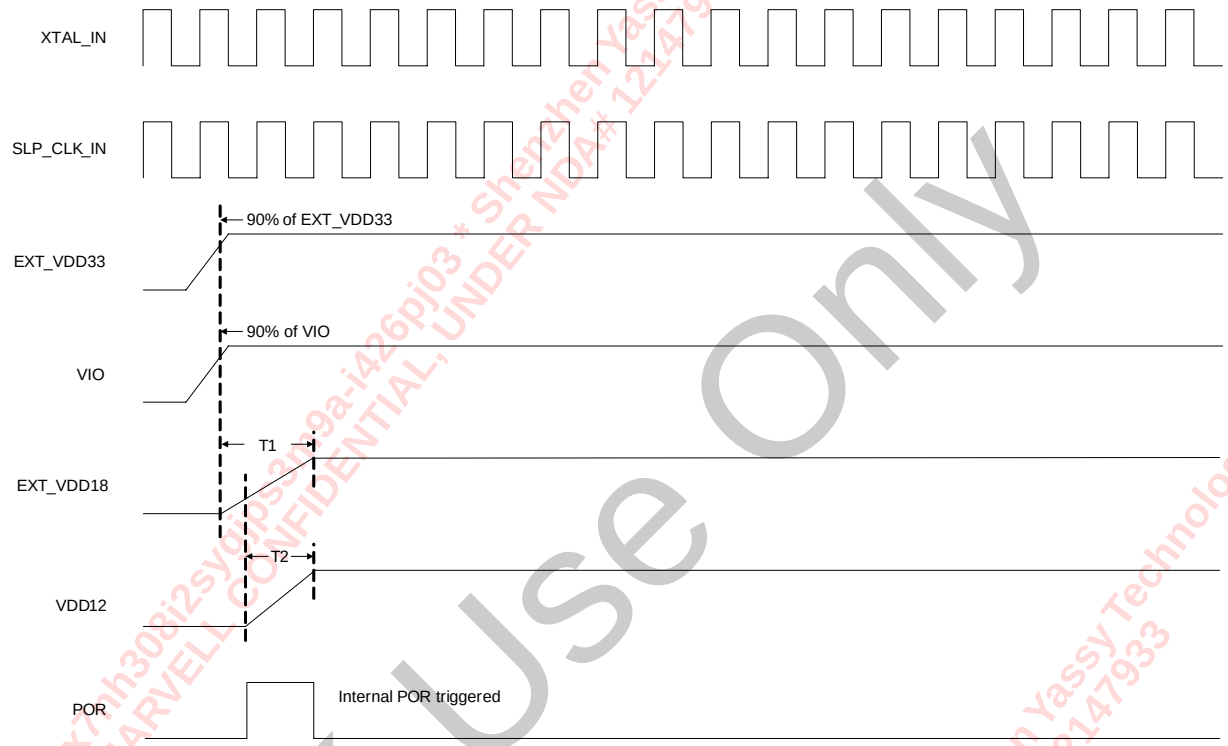


Figure 5: Power Option A—Power Sequence



1.3.1.2 Power Option B—Internal 1.2V, External 1.8V, Internal 3.3V, LDOs Enabled: LVLDO, VBLDO33

The following requirements must be met for correct power up:

- Host VIO supply and internal 3.3V supply from VBLDO33 must be stable before external 1.8V supply (EXT_VDD18) starts ramping up
- External VBAT supply must be at least 3.0V before EXT_VDD18 starts ramping up
- Output load on VDD33 must be 1–2.2 µF. Output load on AVDD33 must be 1–10 µF. Ramp-up time is ~50 µs for this load condition.
- Ramp-up time of EXT_VDD18 T1 must be less than 240 µs
- Output load on VDD12 should be 1–10 µF. Ramp-up time of VDD12 T2 will be at least 100 µs for this load condition.
- If an external oscillator is used, XTAL_IN must be stable before VDD12 starts ramping up
- If an external sleep clock is used, clock frequency of 32.768 KHz must be used and must be stable before VDD12 starts ramping up
- PDn and RESETn are deasserted
- VBLDO must be powered down to save leakage power
- Figure 6 shows the LDO connections
- Figure 7 shows the power up sequence

Figure 6: Power Option B—LDO Connections

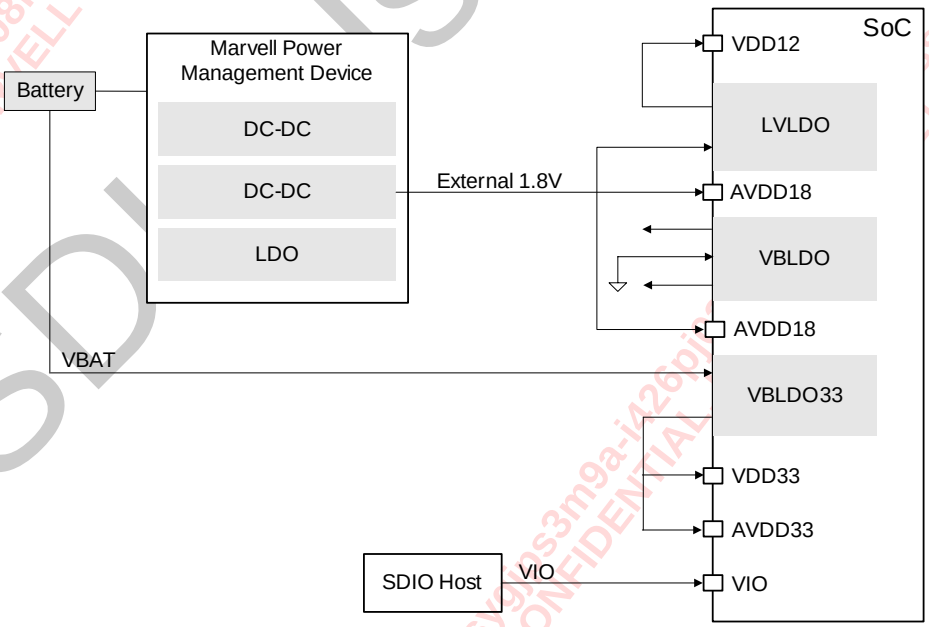
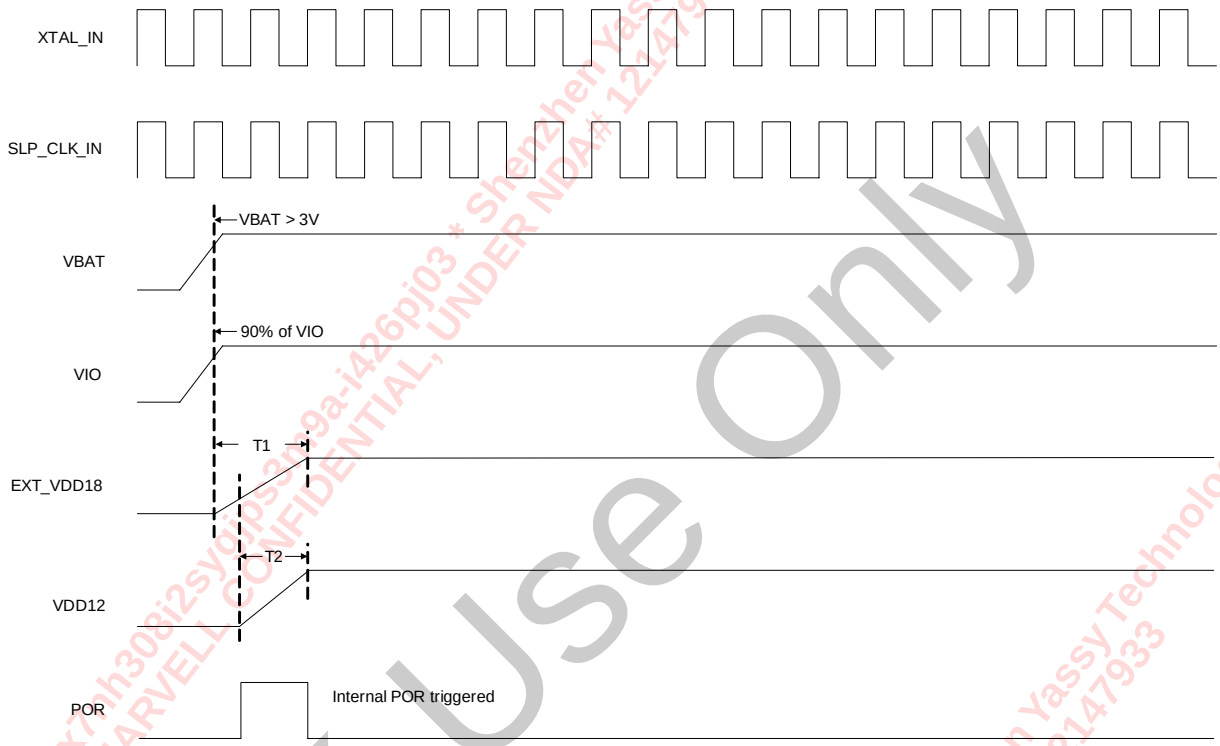


Figure 7: Power Option B—Power Sequence



1.3.1.3 Power Option C—Internal 1.2V, Internal 1.8V, Internal 3.3V, LDOs Enabled: LVLDO, VBLDO, VBLDO33

The following requirements must be met for correct power up:

- VIO must be stable before VBAT starts ramping up
- External VBAT must reach 3.6V within 270 µs (T1)
- Output load on VBLDO33 output must be 1–10 µF
- Output load on each VBLDO 1.8V output must be 1–2.2 µF. The ramp-up time of VDD18 T2 will be less than 200 µs for this load condition.
- Output load on VDD12 must be 1–10 µF. The ramp-up time of VDD12 T3 will be at least will be at least 100 µs for this load condition.
- If an external oscillator is used, XTAL_IN must be stable before VDD12 starts ramping up.
- If an external sleep clock is used, clock frequency of 32.768 KHz must be used and must be stable before VDD12 starts ramping up.
- PDn and RESETn are deasserted.
- Figure 8 shows the LDO connections
- Figure 9 shows the power up sequence

Figure 8: Power Option C—LDO Connections

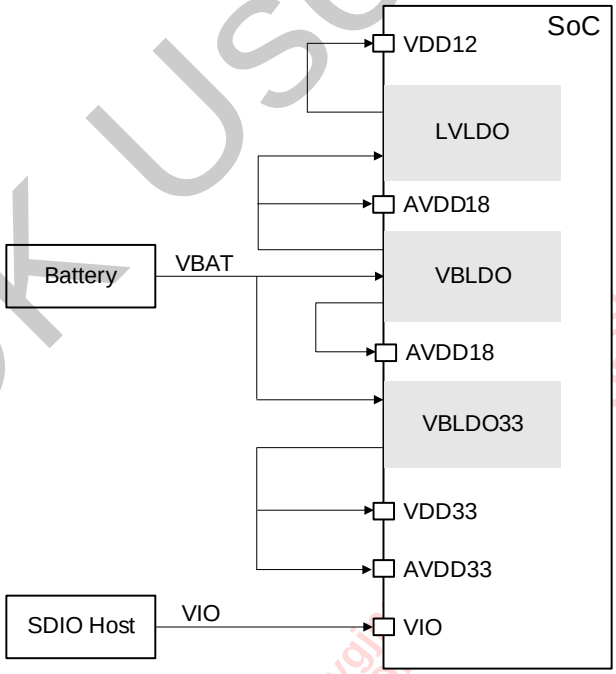
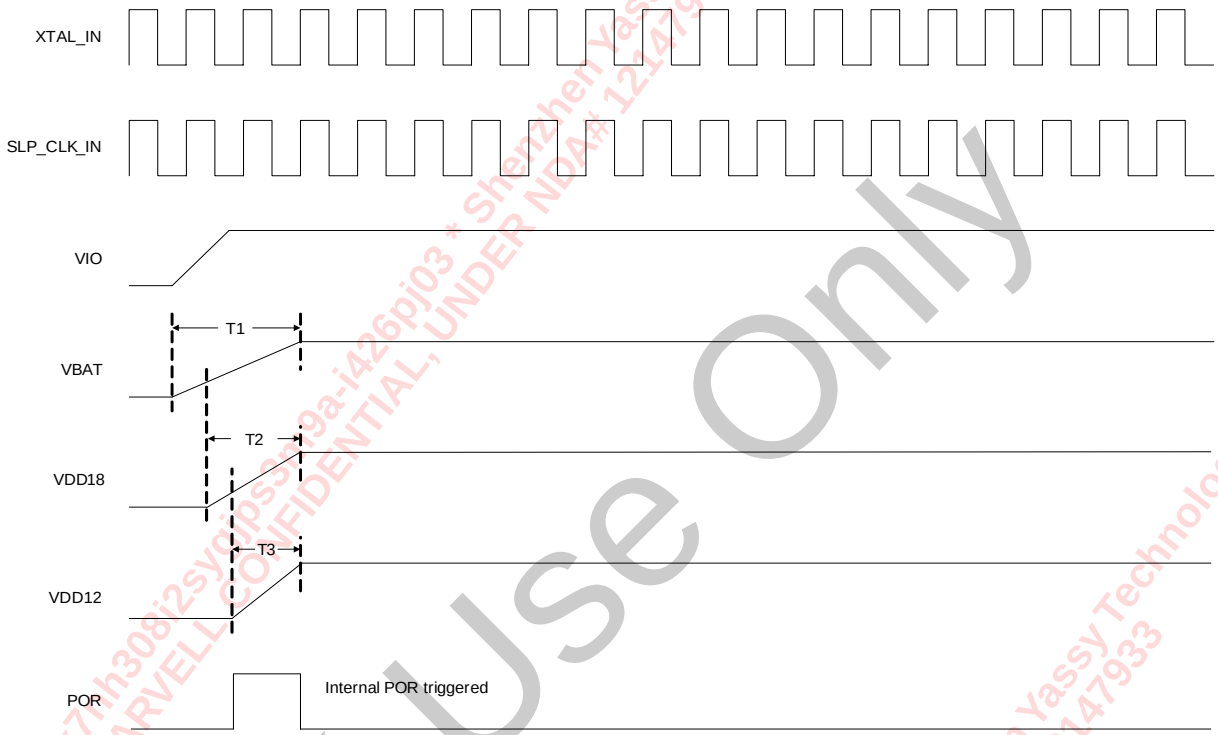


Figure 9: Power Option C—Power Sequence



1.3.2 Alternate Power Up Sequence

In cases where the power options outlined in Section 1.3.1, Power Options, on page 28 cannot be met, the PDn signal can be used. The PDn signal must be asserted low until all external supplies, external sleep clock, and XTAL_IN are stable. After that, PDn can be deasserted.

Figure 10–Figure 12 show the alternate power sequences.

Figure 10: Alternate Option A—Internal 1.2V, External 1.8V, External 3.3V, LDOs Enabled: LVLDO

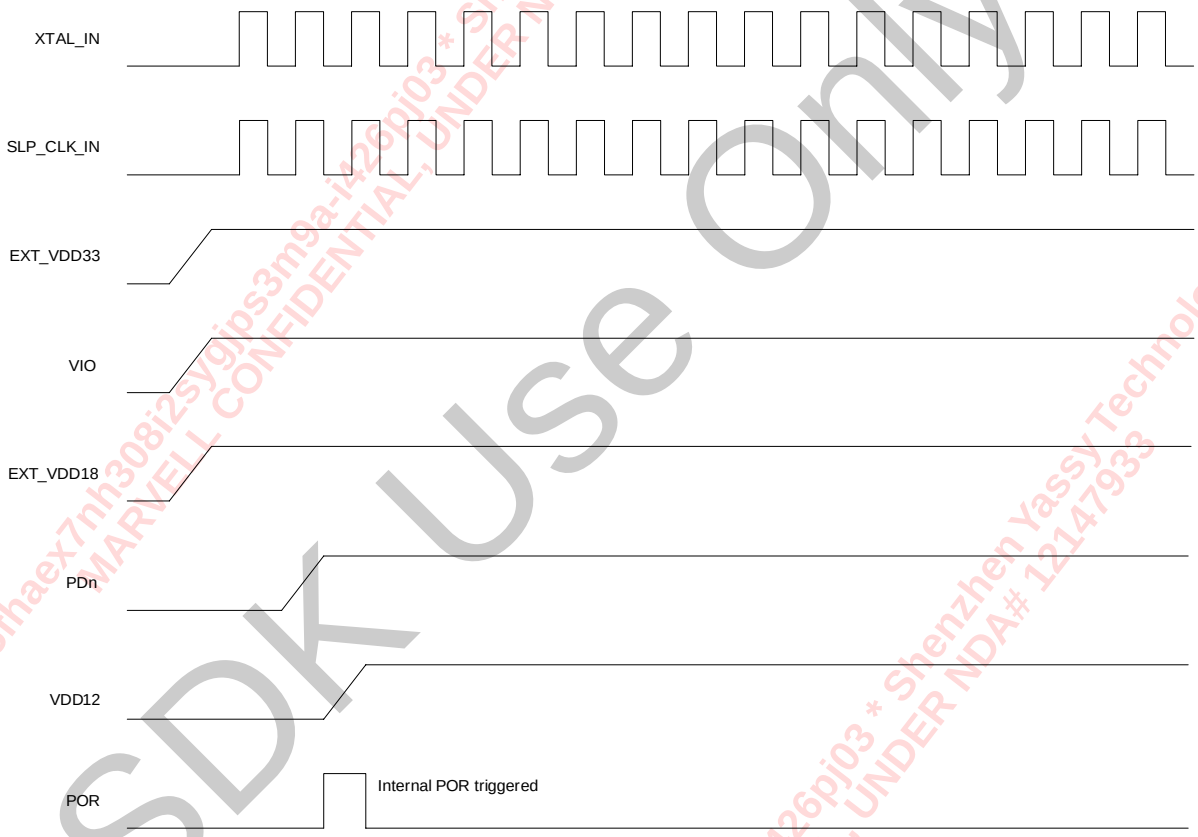


Figure 11: Alternate Option B—Internal 1.2V, External 1.8V, Internal 3.3V, LDOs Enabled: LVLDO, VBLDO33

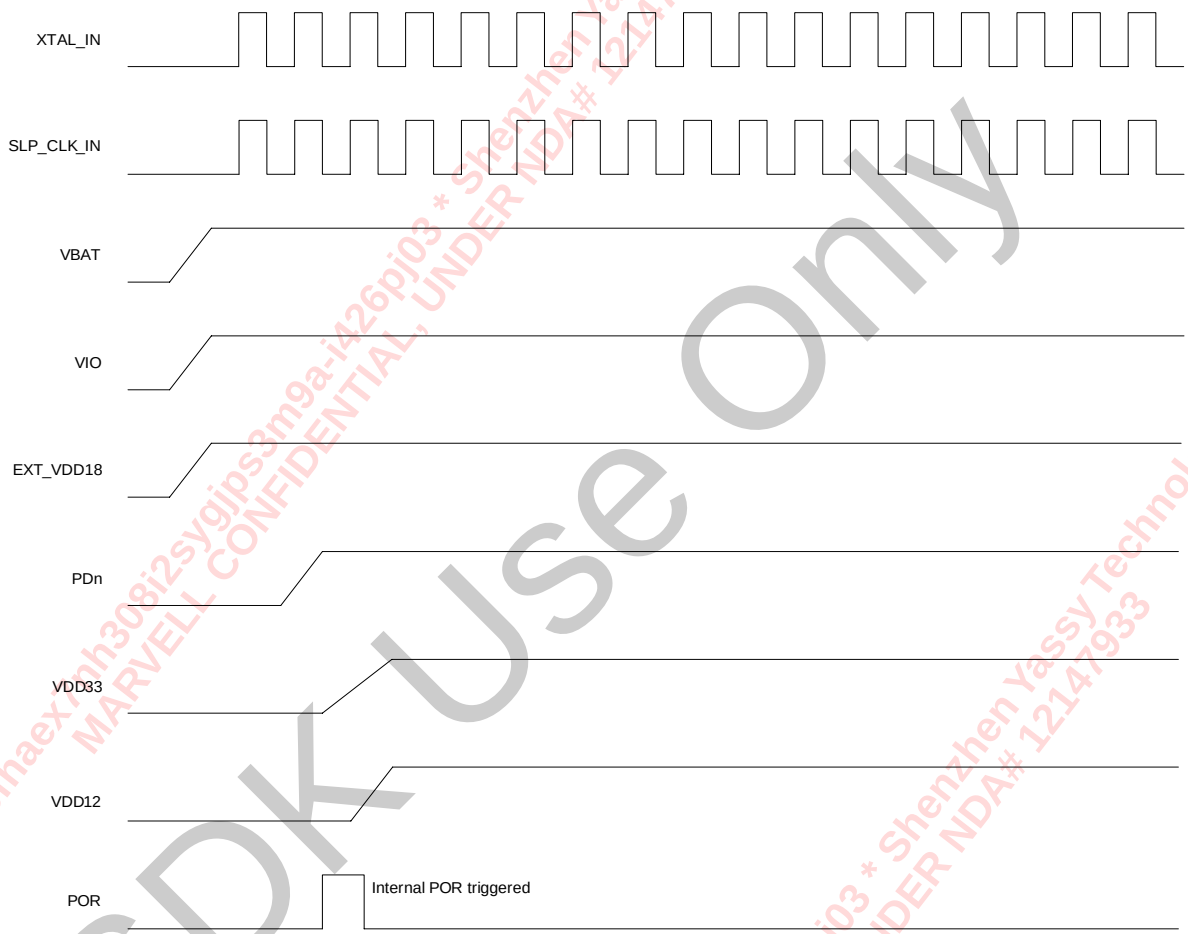
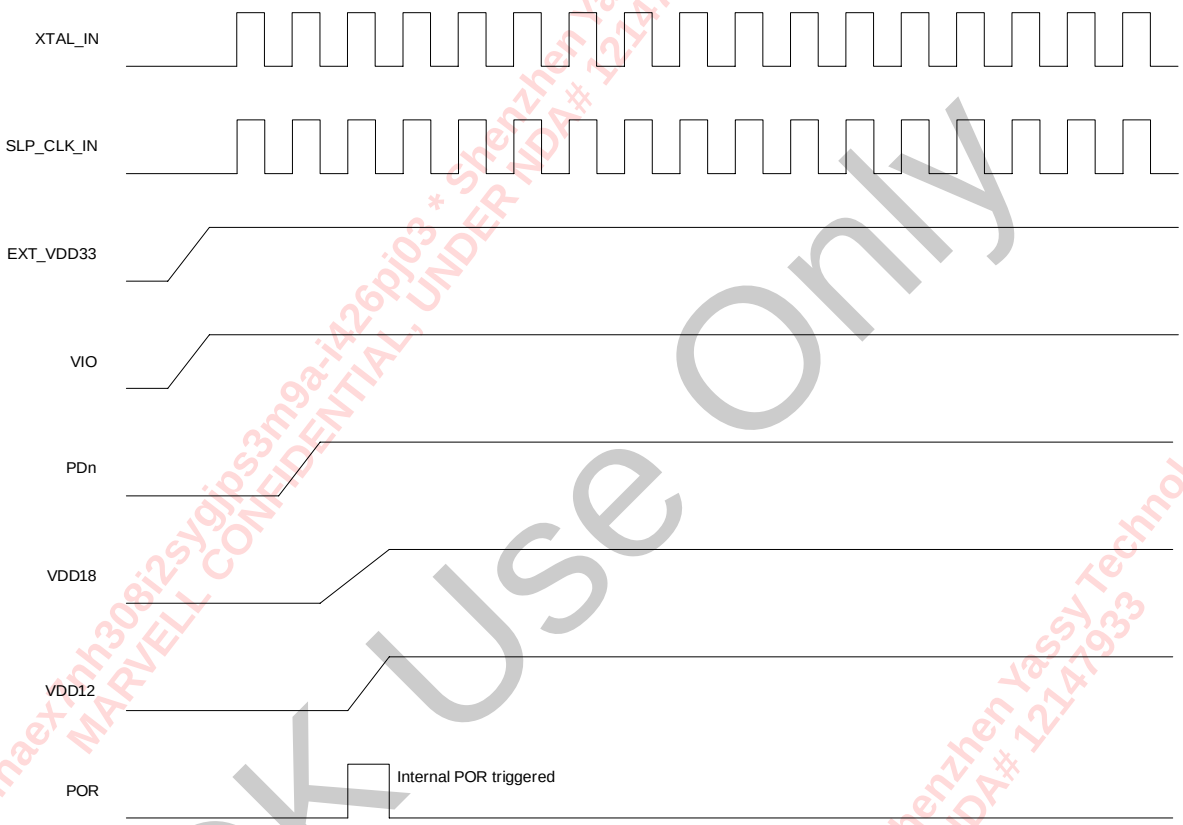


Figure 12: Alternate Option C—Internal 1.2V, Internal 1.8V, Internal 3.3V, LDOs Enabled: LVLDO, VBLDO, VBLDO33



1.3.3 Leakage Optimization

For applications not using Wi-Fi, the device can be put into a low-leakage mode of operation. Two methods are used to achieve this:

- Using PDn pin

The power down state provides the lowest leakage mode of operation. The following requirement must be met for entering power down state:

  - VIO rail must remain powered and stable before and during power down state
  - Assert PDn low to enter power down state

- All rails powered off

Alternatively, all power rails can be powered off. In this case, the state of the PDn pin is irrelevant.

1.4 Configuration Pins

Table 12 shows the pins used as configuration inputs to set parameters following a reset. The definition of these pins changes immediately after reset to their usual function. To set a configuration bit to 0, attach a 100 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1.

Table 12: Configuration Pins

Configuration Bits	Pin Name	Configuration Function
CON[10]	RF_CNTL5_N	Test Mode 0 = test mode 1 = normal mode (default)
CON[5]	RF_CNTL3_P	Oscillator Frequency Select If an external sleep clock is not present, use the reference clock group selection: Bits / Frequency 00 Group 0 (44 MHz) 01 Group 1 (38.4 MHz) 10 Group 2 (40 MHz) 11 Group 3 (26 MHz)
CON[4]	RF_CNTL1_P	
CON[2]	SER_CLK	Boot Options and Host Interface Selection 000 = reserved 001 = reserved 010 = reserved 011 = reserved 100 = reserved 101 = boot from EEPROM 110 = reserved 111 = SDIO host (default)
CON[1]	TDO	
CON[0]	SER_CSn	

2 Processor

The 88W8782 Processor blocks include:

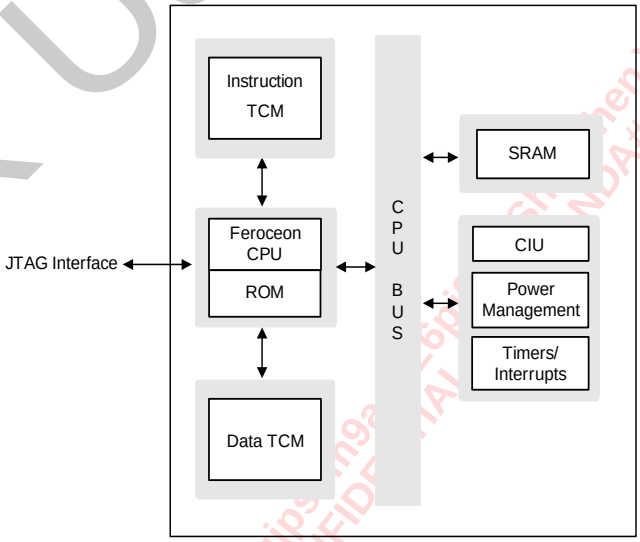
- Embedded CPU
- CPU Interrupts
- CPU Timers
- Reset Configuration

2.1 Embedded CPU

The 88W8782 contains an embedded high performance Marvell Feroceon® ARMv5TE-compliant processor. Features of the CPU include:

- Core processor implementing the Instruction Set Architecture (ISA) Version ARMv5TE
- Tightly Coupled Memory (TCM) for Instructions and Data
- 32-bit ARMv5TE-compliant instruction set
- 32-bit data buses between the processor core and the Instruction and Data TCM

Figure 13: Embedded CPU Architecture



The 88W8782 supports TCM to store instructions and data. The Instruction TCM stores the application code. When the CPU executes a command, it fetches the instruction from Instruction TCM memory first.

When an instruction or data is specified within the address range of the corresponding TCM, the CPU retrieves data from the TCM. When the instruction or data cannot be found in TCM, the CPU accesses the CPU bus or the internal bus.

2.1.1 ROM

The 88W8782 includes a ROM patch unit that capable of patching code to boot ROM. After boot-up, any section/function in boot ROM can be patched using firmware in RAM.

2.2 Two Channel DMA

The 88W8782 Direct Memory Access (DMA) controller has two independent DMA channels.

The DMA channels optimize system performance by moving large amounts of data without significant CPU intervention. Rather than having the CPU read data from one source and write it to another, the DMA channel can be programmed to automatically transfer data independent of the CPU. This frees the CPU and allows it to continue executing other instructions simultaneously with the movement of data.

The main features of the DMA controller include:

- Two independent DMA channels
- Simultaneous data transfer in different directions
- From 1 byte to 64 kB of data transfer per programmed operation
- Burst length of each transfer can be set from 1 to 32 bytes
- Non-word aligned data transfer
- Chained Mode (Scatter-Gather) DMA operation
- Firmware programmable DMA operation

2.2.1 DMA Transfers

Each DMA channel uses internal buffers for moving data. Data is transferred from the source device into an internal buffer and from the internal buffer to the destination device. The DMA channel can be programmed to move up to 64 kB of data per transaction. The burst length of each transfer of DMA can be set from 1 to 32 bytes.

Accesses can be non-aligned in both the source and the destination. Data can flow in different directions through different DMA channels. The DMA channels support chained mode of operation. The descriptors are stored in memory (on internal or host bus), and the DMA channel moves the data until the Null POINTER is reached. The DMA operation can be initiated only by the CPU or host when writing a register.

2.2.2 DMA Channel Arbitration

The DMA controller has a programmable arbitration scheme between both channels. Each channel can be programmed to have priority so that a selected channel has the higher priority or to have the same priority in an alternating fashion. The DMA arbiter control register can be reprogrammed any time, regardless of the status of the channel (active or not active).

2.3 Power Management

The 88W8782 processor supports external power management control.

2.3.1 Sleep Clock

The 88W8782 Power Management Unit (PMU) uses an external sleep clock of 32.768 KHz or an internal sleep clock of 320 kHz during power save modes.

2.3.2 Power Save Mode

The 88W8782 supports Power Save Mode (PSM). Implementation is achieved through the coordination of the driver, firmware, and hardware.

2.4 CPU Interrupts

The interrupt controller provides a simple firmware interface to the interrupt system. The internal CPU accepts two priorities of interrupt:

- Fast Interrupt Request (FIQ) for fast, low-latency interrupt handling
- Interrupt Request (IRQ) for standard interrupt handling

The IRQ and FIQ interrupts use the same interrupt source. However, two separate sets of enable set/enable clear registers are used.

The 88W8782 has a two-level interrupt scheme. In the first level of interrupt, the unit generating the event is indicated. Exceptions to this are the timers and DMA units, in which each individual timer and each DMA channel generate Level 1 interrupts.

The first level interrupt registers are located on the internal CPU bus for fast access. The second level of interrupt is located within each of the units, and is used to determine which interrupt event within the unit generated the interrupt.

All Level 2 (unit level) interrupt sources to the Level 1 interrupt controller are active high and level-sensitive. Each unit interrupt can be masked at the Level 1 interrupt controller, and each individual interrupt event can be masked at the Level 2 interrupt controller.

Figure 14 shows both Level 1 and Level 2 of the interrupt scheme with the details of Level 1.

Figure 15 also shows the detail of the Level 2 interrupt within most internal units. For information on the Level 2 interrupts for each host interface, contact Marvell FAEs.

Figure 14: Interrupt Diagram

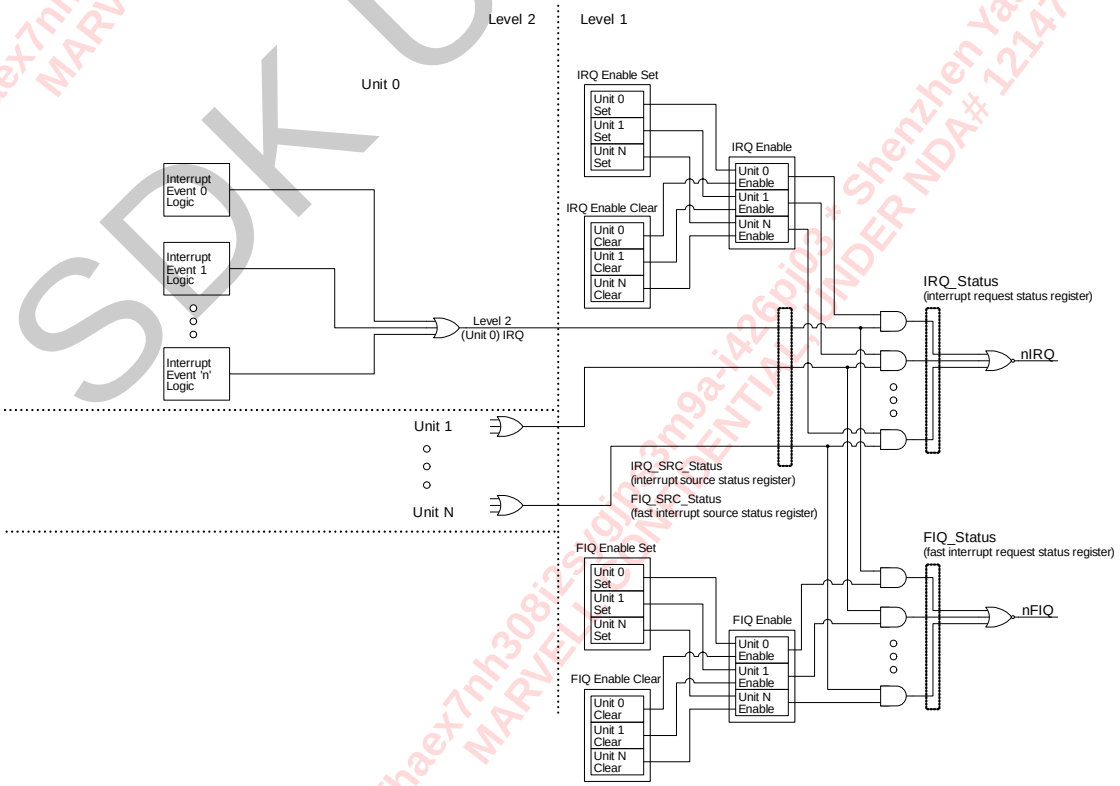


Figure 15: Level 2 Interrupt

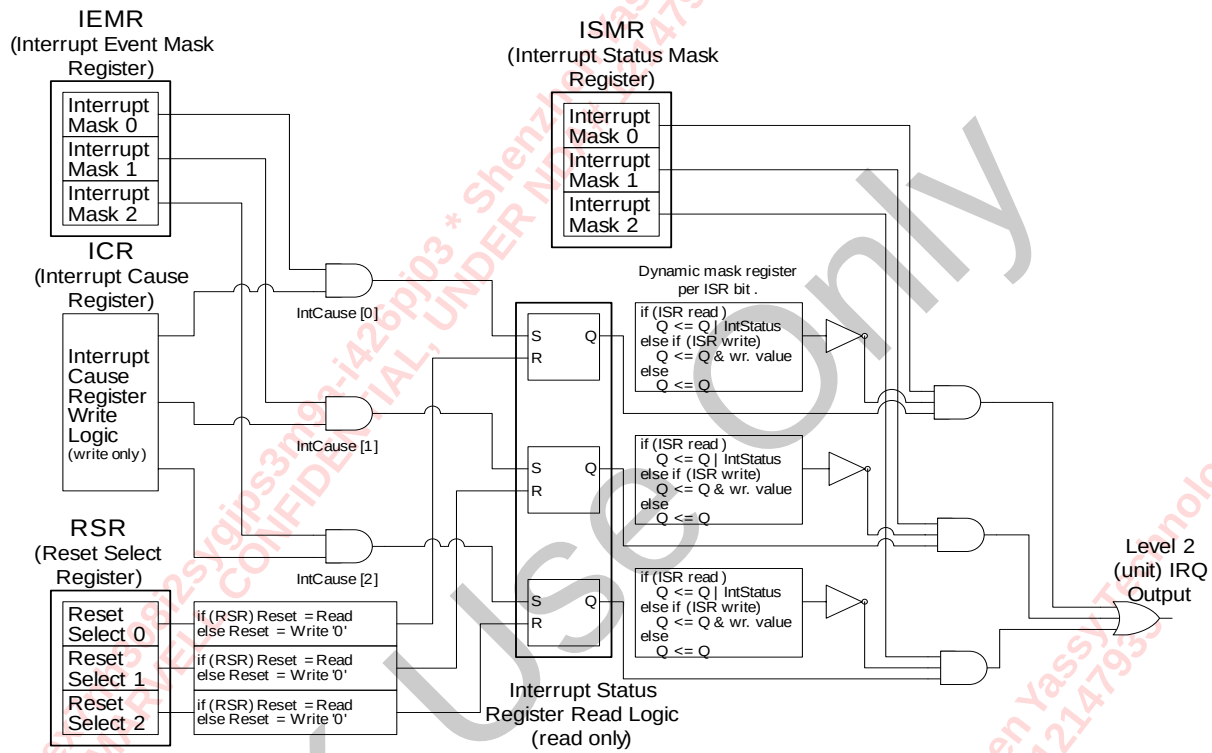


Table 13: Interrupt Register (IRQ and FIQ) Mapping in Interrupt Controller Unit

Interrupt	Interrupt Source
Intr[31:30]	Reserved
Intr[29]	Reserved
Intr[28]	WLAN Radio Interrupt
Intr[27:23]	Reserved
Intr[22]	CIU Interrupt
Intr[21:19]	Reserved
Intr[18]	TKIP/WEP Encryption Interrupt
Intr[17]	CCMP/CMAC/WAPI Encryption Interrupt
Intr[16]	DMA Channel 1 Interrupt
Intr[15]	DMA Channel 0 Interrupt
Intr[14]	Reserved
Intr[13]	Clocked Serial Unit Interrupt
Intr[12]	GPIO Interrupt
Intr[11]	UART Interrupt
Intr[10]	WLAN MAC Interrupt
Intr[9]	Reserved
Intr[8]	Host Interface Interrupt
Intr[7:4]	Timer 4–1 Interrupts • Bit[7] = Timer 4 • Bit[6] = Timer 3 • Bit[5] = Timer 2 • Bit[4] = Timer 1
Intr[3]	CommTx Interrupt
Intr[2]	CommRx Interrupt
Intr[1]	Firmware Enabled Programmed Interrupt
Intr[0]	FIQ Source Status Interrupt

2.5 CPU Timers

The 88W8782 includes the following timers for general use by the CPU:

- Timer 1—slow timer with 1 kHz input
- Timer 2, Timer 3, Timer 4—fast timers with 1 MHz input

Each timer is a 32-bit wide, down counter with an enable signal derived from either a 1 kHz clock or 1 MHz clock (with a resolution of 1 ms and 1 µs, respectively).

The reference clock to the timers is 8 MHz. Prescaler logic is used to generate 1 kHz and 1 MHz for internal timer usage.

Two modes of operation are available:

- Periodic—counter generates an interrupt at a constant interval
- One-shot—timer only generates one interrupt when it reaches 0

The interrupt signals also feed into the interrupt controller to produce FIQs and IRQs.

2.5.1 Timer Operation

Timer operation is described as follows:

1. Timer is loaded and, when enabled, counts down to 0.
2. Upon reaching 0, an interrupt is generated.
3. If timer is in the periodic mode after reaching a 0 count, it reloads its initial value and continues to decrement. Otherwise, it remains at 0 until a firmware reset is issued.

The interrupts can be masked.

2.6 Reset Configuration

The 88W8782 is reset to its default operating state under the following conditions:

- Power-on reset (POR)
- Software/Firmware reset

2.6.1 Internal Reset

The 88W8782 device is reset, and the internal CPU begins the boot sequence when any of the following internal reset events occur:

- Device receives power and VDDL supplies rise (triggers internal POR circuit)
- Host driver issues a soft reset

2.6.2 Calibration

The 88W8782 performs calibration when the device is powered up.

3 WLAN

3.1 WLAN MAC

The 88W8782 Wireless Media/Medium Access Controller (MAC) provides all the required functions and many optional features of the IEEE 802.11 standard.

The 88W8782 WLAN MAC provides:

- Frame Exchange at the MAC level to deliver data
- Received frame filtering and validation (Cyclic Redundancy Check (CRC))
- Generation of MAC header and trailer information (MAC Protocol Data Units (MPDUs))
- Fragmentation of data frames (MAC Service Data Units (MSDUs))
- Access Mechanism support for fair access to shared wireless medium through:
  - Distributed Coordination Function (DCF)
  - Enhanced Distributed Channel Access (EDCA)
- A-MPDU Aggregation/Deaggregation
- 20/40 MHz Channel Coexistence
- RIFS Bursting
- Management Information Base (MIB)
- Radio Resource Measurement
- Quality of Service (QoS) block acknowledgement with support for 802.11n extensions
- Dynamic Frequency Selection
- Transmit Beamformee Support
- Transmit Rate Adaptation
- Transmit Power Control

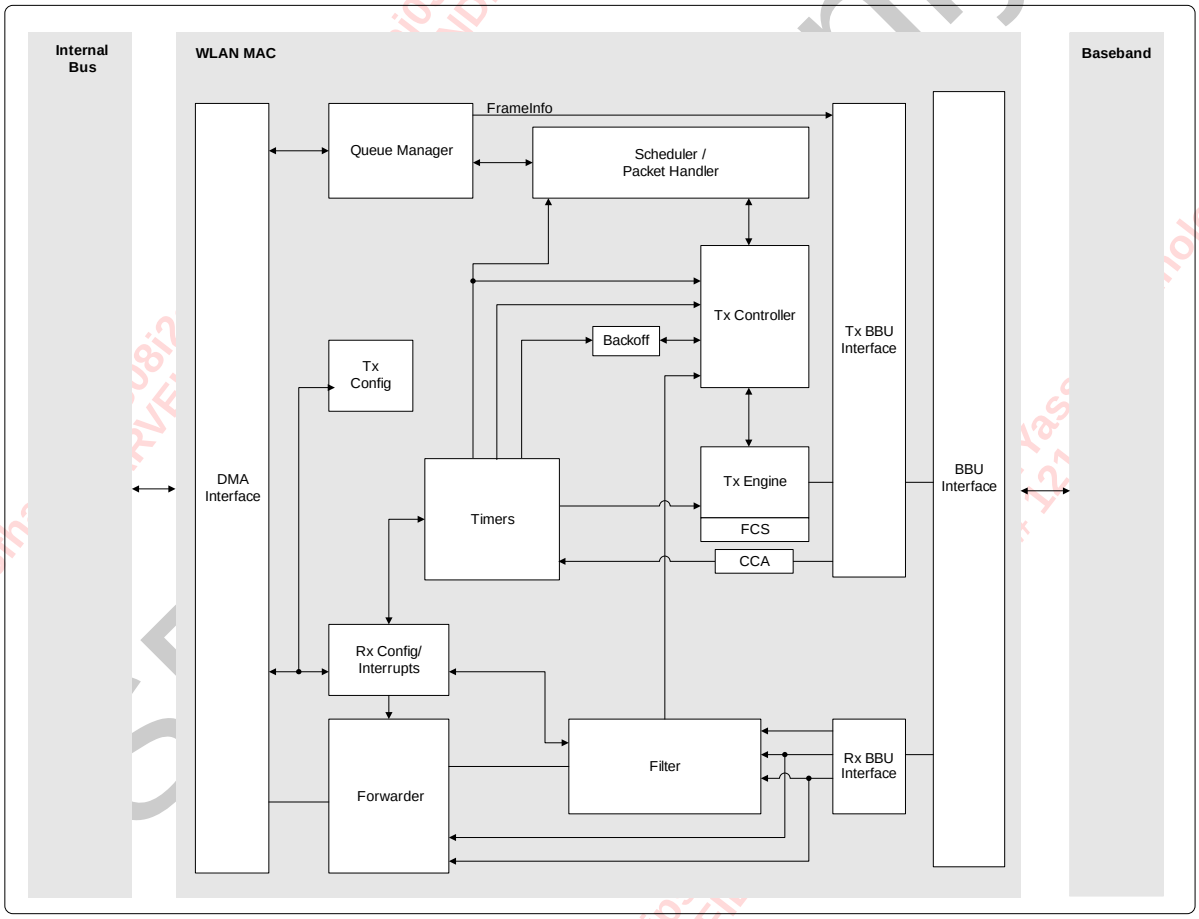
3.1.1 MAC Interface

Interfaces to the MAC include:

- **Baseband Interface**—utilized in the transmission and reception of MAC frames.
- **DMA Interface**—allows the MAC to access the shared memory for moving user data to and from the local host and to manage messages to and from the local CPU.
- **Configuration Registers**—allows access to programmable MAC functions.

Figure 16 shows the main interfaces to the MAC core.

Figure 16: MAC Architecture



3.1.1.1 Transmit Path

On the transmit path, data from the host system is queued in memory by the local CPU. The MAC retrieves data for transmission at the appropriate time.

- **Tx Baseband Interface**—implements transmit interface between WLAN MAC and baseband
- **Tx Controller**—implements logic necessary to support DCF and EDCA access methods (also responds to requests to transmit MAC frames over the wireless medium)
- **Tx Backoff**—implements backoff timer phase in which the device chooses a random backoff timer from a contention window of values
- **Tx Engine**—transmits frames to the baseband processor (as frames are transmitted, the FCS is computed and appended at the end of the frame; for beacons and probe responses, the Tx engine overwrites the timestamp in the frame header with the current time plus the PHY delay)
- **Tx Scheduler**—schedules transmission of queued frames in the Tx buffer based on status of the queues and the state of the transmitter
- **Tx Queue Manager**—fetches and processes data from memory
- **AMPDU Tx**—aggregate multiple MPDU into a single AMPDU

3.1.1.2 Receive Path

On the receive path, MAC frames received over the wireless medium are passed to the MAC through the baseband interface.

- **Rx Baseband Interface**—implements the receive interface between WLAN MAC and baseband.
- **Rx Filters**—extracts address, timing, and frame type information from received frames and notifies the appropriate blocks. It also performs validation of received frames.
- **Rx Forwarder**—enhanced descriptor-based buffer management scheme.
  The buffers are allocated by the CPU and managed through a descriptor array. Each descriptor points to a single memory buffer and contains all the relevant information relating to that buffer (i.e., buffer size, buffer pointer, etc.). Data is written to the buffer according to information contained in the descriptor. Whenever a new buffer is needed (end of buffer or end of packet), a new descriptor is automatically fetched. The data movement operation is then continued using the new buffer. A single MPDU can occupy multiple descriptor-buffers. Features include:
  - Hardware support for twelve separate queues
  - Three queues to track and de-fragment fragmented streams
  - Five programmable receive queues that filter according to the TID field in QoS frames
  - Automatic fetching and maintaining of hardware descriptors
  - Interrupt or polling driven approach through a queue status register
- **AMPDU Rx**—deaggregate incoming AMPDU into multiple MPDUs

3.1.1.3 Timers

The timers block generates the internal clocks that support MAC transmit and receive operations. It also supports the power down and low power modes.

3.1.2 Beaconing

For reliable communication to occur over the wireless medium, the stations (clients) in a Basic Service Set (BSS) must synchronize to a common time base. A Beacon frame is sent periodically to implement the Timing Synchronization Function (TSF) among the associated stations and to inform stations of impending traffic.

The Beacon frame is scheduled to occur regularly at the Target Beacon Transmission Time (TBTT). However, because the Beacon is a frame like all other frames, the Beacon frame must compete for the medium and may not be transmitted at the appointed TBTT.

3.1.2.1 Beaconing in an Independent BSS

In an Independent Basic Service Set (IBSS), the synchronization mechanism is distributed among the stations in the BSS. The mobile station that starts the BSS resets its TSF timer to 0 and transmits a Beacon, choosing a Beacon period. This process establishes the basic time base for the BSS.

When the TBTT is reached, each station in the IBSS attempts to send a Beacon frame. However, each station relies on a random delay value after the TBTT to transmit its Beacon frame.

If the station receives a Beacon frame from another station before the delay expires, the receiving station cancels its Beacon transmission. If the station does not receive a Beacon frame before the delay expires, the Beacon frame is transmitted as scheduled.

In an IBSS, a station updates its TSF timer from the received Beacon frame only when the received value is greater than the current value in the TSF timer station. This rule ensures that the faster timer value is spread throughout the BSS.

3.1.2.2 Beaconing in an Infrastructure BSS

In an infrastructure BSS, the AP (Access Point) is responsible for transmitting the Beacon frames regularly. The AP attempts to transmit the Beacon frame at the TBTT.

Since the Beacon frame must compete for the medium like other frames, it can be delayed beyond the TBTT due to other traffic and backoff delays. In addition, because the Beacon frame is sent to a broadcast address, it is not retransmitted in case of errors. Regardless of timing or transmission errors of a previous Beacon frame, the AP attempts to send the following Beacon frame at the next TBTT.

3.1.3 Frame Exchange

The 802.11 MAC frame exchange protocol requires the participation of all stations in the WLAN. This requirement means that all stations decode and react to the information in the MAC header of every frame they receive. The 802.11 MAC relies on a frame exchange protocol in which the source of the frame is allowed to determine whether the frame has been successfully received at the destination.

Although about thirty frames are defined for the 802.11 WLAN MAC, basic frame exchange is described below.

In environments with low demand for bandwidth, the minimum frame exchange consists of two frames:

- Frame sent
- Frame acknowledgement

If the source does not receive acknowledgement, the source attempts to retransmit the frame. The frame and its acknowledgement are an atomic unit of the MAC protocol. They are not to be interrupted by any other station.

In environments with high demands for bandwidth, four frames are used.

- Request to Send (RTS)
- Clear to Send (CTS)
- Frame sent
- Frame acknowledgement

The source sends an RTS to the destination, and the destination sends a CTS back to the source. When the source receives the CTS frame, it sends the frame pending following an SIFS interval. When the destination receives the frame correctly, the destination returns an acknowledgement. This 4-way exchange is an atomic unit of the MAC protocol.

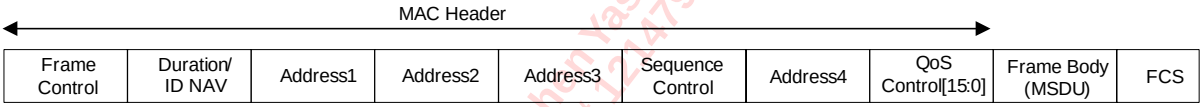
3.1.3.1 Frame Format

The IEEE 802.11g/b frame format requires up to four addresses depending on frame type. A particular frame type can contain one, two, three, or four address fields. The position of the address in the address fields determines its function. Addresses are specified according to the 802.11g/b standard as a collection of 6 bytes. The types of addresses defined for the WLAN are:

- **Transmitter Address** (TA)—identifies the MAC that transmitted the frame onto the wireless medium. The TA is used by stations to identify the MAC to which they need to send a response.
- **Receiver Address** (RA)—identifies the MAC receiving a frame over the wireless medium.
- **Source Address** (SA)—identifies the MAC that originated the frame. This address does not always match the TA address because of the indirection that is performed by the Distribution System. The SA field should be used to indicate that a frame has been received to higher layer protocols.
- **Destination Address** (DA)—identifies the final destination address where the frame is sent. This address does not always match the RA address because of the indirection that is performed by the Distribution System.
- **Basic Service Set ID** (BSSID)—in an infrastructure BSS, the MAC address of the AP is used as the BSSID. This is a unicast address.

Figure 17 shows the QoS frames supported as specified in the WMM and draft IEEE 802.11e standards.

Figure 17: IEEE 802.11 Frame Format



3.1.3.2 Lifetime and Retry Counters

Lifetime and retry counters limit the number of times that a frame can be retransmitted. When the MAC determines that it is no longer required to transmit a frame, the transmission of the frame is cancelled, and the host driver is notified by the local CPU.

3.1.4 Fragmentation

The MAC can fragment a frame to increase the probability that the frame is delivered without errors in the presence of interference.

A frame is divided into one or more fragments equal to the length of the fragmentation threshold. No more than one fragment smaller that the fragmentation threshold is generated. When a frame is fragmented, the sequence control field in the frame header indicates the placement of the individual fragment among the set of fragments.

The lowest numbered fragment is transmitted first. Subsequent fragments are transmitted immediately after acknowledgement of the previous fragment is received. This process is known as a fragment burst. If a fragment is not acknowledged, the normal rules of frame retransmission apply.

3.1.5 Access Mechanism

The 802.11 MAC is a Carrier Sense Multiple Address/Collision Avoidance (CSMA/CA) "listen before talk" access mechanism. It relies on the physical carrier sense from the Physical Layers (PHY) and the virtual carrier sense implemented in the Network Allocation Vector (NAV) of every frame to determine the state of the medium.

The decision of a station that the medium is idle is based on timing intervals. The timing intervals are kept current through the NAV and the physical CCA indication. The WLAN MAC recognizes the timing intervals. Table 14 shows the timing intervals.

Table 14: MAC Timing Intervals

Timing Interval	Description
SIFS	Short Interframe Space The SIFS is the shortest interval and is determined by the PHY.
Slot Time	Slot Time Slot time is determined by the PHY.
PIFS	Priority Interframe Space The PIFS is equal to the SIFS plus one slot time.
DIFS	Distributed Interframe Space The DIFS is equal to the SIFS plus two slot times.
EIFS	Extended Interframe Space The EIFS is larger than the other intervals. It allows the frame exchange to complete correctly when the received frame contains errors.
AIFS	Arbitration Interframe Space

3.1.5.1 DCF Operation

DCF operates during the contention-based period (CBP) when all stations are competing for access to the medium. The following steps describe a CBP session.

1. MAC receives a request to transmit a frame.
2. Physical and virtual carrier sense mechanisms are checked.
3. When both mechanisms indicate medium is idle for a DIFS or EIFS (in case of errors) interval, MAC begins transmission of frame. Transmitter must also make sure that backoff process, which was started at the end of previous transmission, is completed.
4. When MAC detects medium to be idle through both physical and virtual sensing mechanisms, MAC decrements backoff value by one slot time.
5. When transmission is not successful (no acknowledgement received), a new backoff interval is selected, and backoff countdown is begun again.
6. Once backoff interval has expired, MAC begins transmission.

This process continues until transmission is successful or is cancelled.

3.1.6 A-MPDU Aggregation/Deaggregation

The 88W8782 supports aggregation of MAC MPDU frames in the transmit direction to form A-MPDU frames, and deaggregation of MAC MPDU frames in the receive direction. This aggregation/deaggregation function is used in conjunction with the Block Ack feature.

3.1.7 20/40 MHz Channel Coexistence

The 88W8782 MAC supports the following 20/40 MHz coexistence modes:

- Control (channel) only mode—Ignore CCA-extension (i.e., CCA = CCA-control only).
- 40 MHz Abort mode—Consider CCA-control only for DIFS/backoff. Consider CCA-extension only when MAC is about to start 40 MHz transmission. If busy, packet transmission is abandoned and DIFS/backoff is redone.
- Conservative mode—CCA = CCA-control OR CCA-extension. For all packets transmissions, both CCA-control and CCA-extension are considered.

See Section 3.2.4, 802.11n Optional Features, on page 61.

3.1.7.1 Control (Channel) Only Mode

In this mode, packets are transmitted based on CCA-control only. CCA-extensions are ignored. If an extension channel is busy, there could be a packet collision on the 40 MHz channel.

3.1.7.2 40 MHz Abort Mode

For any packet, DIFS/backoff is performed based on CCA-control. CCA-extension is ignored until DIFS/backoff is complete.

When the MAC is ready to transmit a 40 MHz packet that starts a TXOP, it checks whether CCA-extension is idle during the PIFS interval preceding the transmit decision. If CCA-extension is busy during the PIFS interval preceding the transmit decision, the MAC abandons packet transmission and initiates DIFS/backoff again.

All 20 MHz packets will be transmitted without any check for CCA-extension.

3.1.7.3 Conservative Mode

In this mode, both CCA-control and CCA-extension are considered for DIFS/backoff, and packets are transmitted based on both CCAs.

3.1.7.4 20 MHz Duplicate Abort Mode

If a 20 MHz packet is programmed for transmission on duplicate sub-channels, the MAC checks whether CCA-extension is idle during the PIFS interval preceding the point of initiating a transmission that begins a TXOP. If CCA-extension is busy during the PIFS interval preceding the transmit decision, it will abort transmission and initiate DIFS/backoff again.

DIFS/backoff is performed based on CCA-control. CCA-extension is ignored until DIFS/backoff is complete.

3.1.7.5 RTS/CTS-to-Self Protection Scheme

Two schemes are available for RTS/CTS-to-Self protection.

- Protection mode 1—For both 20 MHz and 40 MHz packet protection, RTS/CTS-to-Self frame will be transmitted over the sub-channel(s) programmed in RTS Rate register.
- Protection mode 2—For a 20 MHz data packet protection, RTS/CTS-to-Self frame will be transmitted on the same sub-channel(s) as that of the data packet. For a 40 MHz data packet protection, RTS/CTS-to-Self frame will be transmitted over duplicate sub-channels.

3.1.8 RIFS Bursting

The 88W8782 supports reception of Reduced Interframe Space (RIFS) frame bursts.

See Section 3.2.4, 802.11n Optional Features, on page 61.

3.1.9 Management Information Base

The 88W8782 WLAN MAC supports management and troubleshooting operations for network infrastructure devices. The device constructs Management Information Base (MIB) parameters as defined in part 11.4 of the IEEE 802.11 specification.

3.1.10 Radio Resource Measurement

The 88W8782 WLAN MAC supports WLAN Radio Measurements. Radio measurements enable stations to understand the radio environment in which they exist by observing and gathering data on both the radio link performance and the radio environment. Measurement data is then made available to station management and upper protocol layers for use in a range of applications. The data can also be used to attain necessary performance levels.

The IEEE 802.11k Radio Resource Measurement (RRM) specification (draft) includes measurements that extend the capability, reliability, and maintainability of WLANs by providing standard measurements across vendors and providing the resulting measurement data to upper layers in the communications stack.

See Section 3.2.3, 802.11k Radio Resource Measurement, on page 60.

3.1.11 Quality of Service

In addition to the Contention-Free Queue (CFQ) to support the IEEE 802.11e QoS function, the 88W8782 includes the queues shown in Table 15. The queue priority is listed in descending order, which is observed during the CFP. During a CFP, the CFQ has the highest priority.

Table 15: QoS Queues

Queue	Description
CMQ	Control/Management Queue
BWQ	Bandwidth Allocation/Request Queue
TCQ[7]	Traffic Category Queue 7
TCQ[6]	Traffic Category Queue 6
TCQ[5]	Traffic Category Queue 5
TCQ[4]	Traffic Category Queue 4
TCQ[3]	Traffic Category Queue 3
TCQ[2]	Traffic Category Queue 2
TCQ[1]	Traffic Category Queue 1
TCQ[0]	Traffic Category Queue 0

3.1.11.1 Backoff

During the contention-based periods, backoff periods are invoked, each using its set of CWMin, CWMax, and AIFS periods as specified in clause 9.2.5.2 of IEEE 802.11e. The CMQ and the BWQ use the AIFS 7 time and do not have a backoff.

3.1.11.2 Block Acknowledgement

The 88W8782 includes support for IEEE 802.11e Block Acknowledgement to improve media utilization. Whereas legacy 802.11 MACs always send an acknowledgement (Ack) frame after each successfully received frame, block Ack allows several data frames to be transmitted before an Ack is returned. The 88W8782 block Ack scheme (BlockAck) allows a single Ack for a block of multiple MSDU/MPDUs.

3.1.12 Dynamic Frequency Selection

The IEEE 802.11 standards govern two different frequency ranges. 802.11g/b products operate within the 2.4 GHz range, 802.11a products operate within the 5 GHz range, and 802.11n products can operate in either the 2.5 GHz or 5 GHz frequency range. Because different countries around the world have allocated portions of the 5 GHz range to radar applications in addition to Wi-Fi, WLAN devices are required to detect the presence of radar pulses when operating in the 5 GHz range, and change channels when a conflict is detected. The 802.11 standard includes provisions for APs to inform wireless clients of the appropriate channel for local usage.

Dynamic Frequency Selection (DFS) for the 5 GHz range is covered by the IEEE 802.11h standard and FCC requirements.The 88W8782 WLAN MAC supports DFS by accepting DFS pulse data from the baseband unit and storing that data into the DFS queue for software interpretation. Software is notified of a DFS pulse arrival through interrupts.

See Section 3.2.2, Dynamic Frequency Selection, on page 60.

3.1.13 Transmit Beamformee Support

The 88W8782 supports beamformee functionality for the Explicit Feedback Transmit Beamforming feature specified in IEEE 802.11n standard.

Transmit Beamforming is a spatial filtering mechanism used at the transmitter (beamformer) to improve the received signal power or signal-to-noise ratio at an intended receiver (beamformee). To calculate an appropriate steering matrix for transmit spatial processing when transmitting to a specific beamformee, the beamformer needs to have an accurate estimate of the channel that it is transmitting over.

Under the 802.11n Explicit Feedback Beamforming scheme, the beamformer periodically transmits sounding PPDUs to solicit the latest channel information from the beamformee. Upon receiving a sounding PPDU from the beamformer, the beamformee makes a direct estimate of the channel from the associated training symbols, quantizes it (also computes the forward steering matrix), and transmits it back to the beamformer as a feedback frame. The beamformer will then use this feedback information to beamform all subsequent transmissions destined to the Beamformee.

Supported 802.11n transmit beamforming features include:

- Explicit Feedback Beamformee functionality
- Reception of NDP sounding and Squared sounding PPDUs
- Immediate feedback and delayed feedback scheme
- Compressed and Non-compressed Feedback format

3.1.14 Transmit Rate Adaptation

The 88W8782 WLAN MAC includes an enhanced auto rate drop scheme. This scheme features a software controlled multi-tiered rate drop mechanism, where the rate drop table is stored in memory. This allows the transmission rate to be changed even after the frame is queued, up until the point when the frame is fetched by hardware from the appropriate queue. The enhanced rate drop scheme can be used for both high throughput and legacy frame formats.

The duration computation for the rate adaptation scheme is performed in hardware.

3.1.15 Transmit Power Control

The 88W8782 is capable of per-packet transmit control, where the transmit power is programmable for each packet according to the Tx rate. The Transmit Rate-Based Power Control (TRPC) module controls the transmit power setting of the radio. Programmable transmitter registers in the radio include the following parameters:

- PTRGT—power target
- PWDET_HI—power detect high
- PWDET_LO—power detect low

3.1.15.1 TRPC Programming

TRPC programming occurs before each transmission.

There are sixteen sets of programmable registers in the radio for transmit power settings that correspond to various possible transmit rates.

The index for the rate selection is driven by the MAC, which is used for the table lookup in the radio. The MAC also provides control signals for the transmit antenna (one bit per antenna) before each transmission.

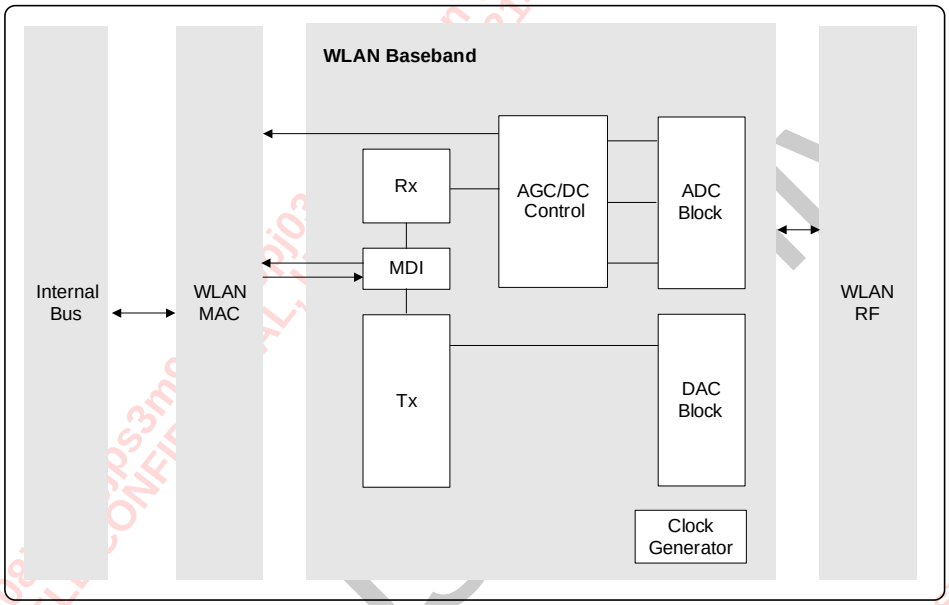
3.2 WLAN Baseband

The 88W8782 baseband processor is designed to support high performance, Single Input Single Output (SISO) WLAN applications. Features include:

- 802.11n 1x1 SISO—interfacing with on-chip Marvell SISO RF radio
- Backward compatibility with legacy 802.11a/g/b technology
- PHY data rates up to 150 Mbps
- 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz bandwidth in 40 MHz channel, and 20 MHz duplicate legacy bandwidth in 40 MHz channel mode operation
- Modulation and Coding Scheme (MCS)—0~7 and 32 (duplicate 6 Mbps)
- Dynamic Frequency Selection (radar detection)
  - Enhanced radar detection for long and shot pulse radar
  - Enhanced AGC scheme for DFS channel
  - Japan DFS requirements for W53 and W56
- 802.11k Radio Resource Measurement
- 802.11n Optional Features
  - 20/40 MHz coexistence
  - Space-Time Block Coding (SRBC) (1 stream receive)
  - Short guard interval for both 20 and 40 MHz operation (Tx/Rx)
  - Reduced Inter-Frame Spacing (RIFS) on receive path
  - Beamformee function and hardware acceleration for immediate feedback
  - Greenfield Tx/Rx
- Power save features

3.2.1 Architecture

Figure 18: Baseband Top Block Diagram



3.2.1.1 Operation

There are two data path operational modes:

- 40 MHz
- 20 MHz

High throughput (HT) mode supports packets with HT fields in a Mixed Mode or a Greenfield (GF) packet format. Legacy (L) mode supports 802.11 packets (use either single sub-channel).

40 MHz Mode

Data path operation is 40 MHz. The baseband dynamically switches between HT and legacy mode for each Tx/Rx packet.

- HT Mode—40 MHz or 20 MHz Tx/Rx and 802.11n MCS0~7 and MCS 32
- L Mode—all 802.11g/b rate operations on either upper or lower 20 MHz sub-channel

20 MHz Mode

Data path operation is 20 MHz.

- HT Mode—20 MHz Tx/Rx and 802.11n MCS0~7
- L Mode—all 802.11g/b rates

3.2.1.2 DSP Blocks

The 88W8782 baseband includes two digital signal processing paths:

- 802.11a/g and 802.11n for single stream
- 802.11b

High Throughput Tx

Figure 19 shows the transmit path.

Figure 19: Baseband DSP Block Diagram—Tx

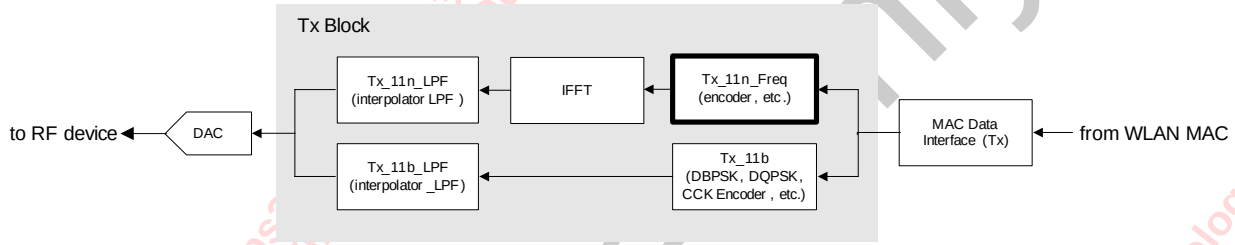
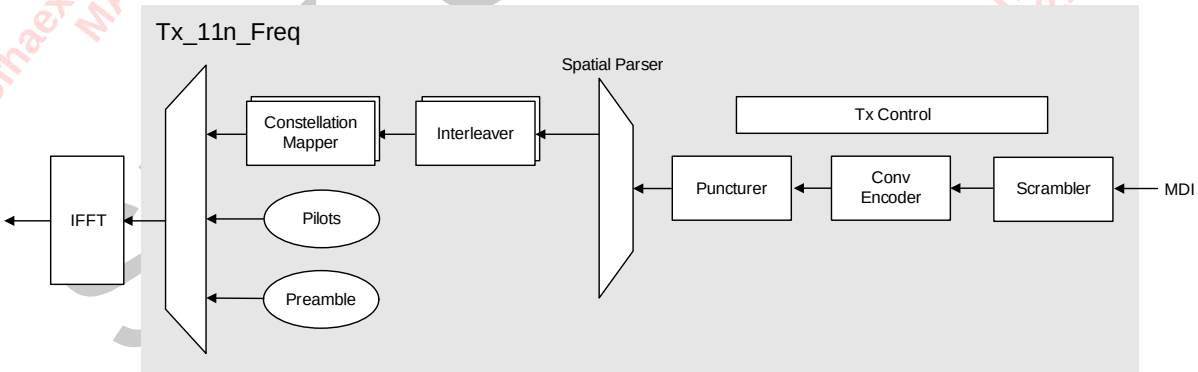


Figure 20 shows the further details of the Tx_11n_Freq transmit path.

Figure 20: Baseband 802.11n Block Diagram—Tx



High Throughput Rx

Figure 21 shows the receive path.

Figure 21: Baseband DSP Block Diagram—Rx

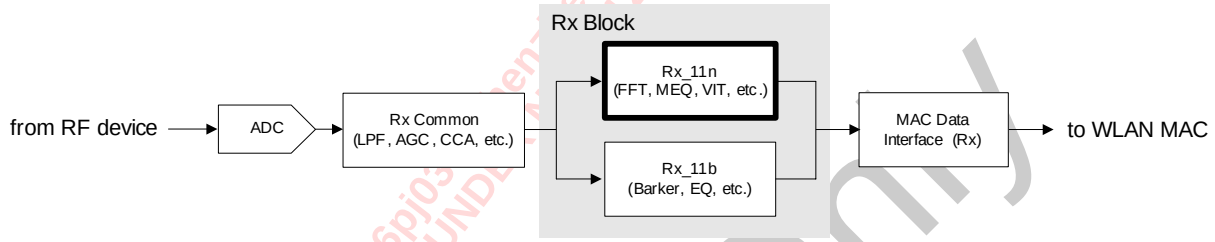
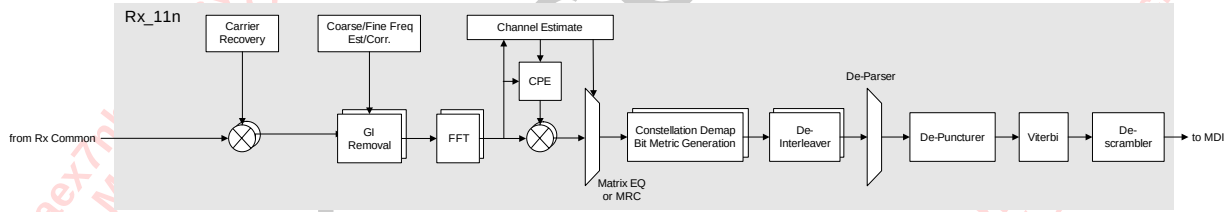


Figure 22 shows the further details of the Rx_11n receive path.

Figure 22: Baseband 802.11n Block Diagram—Rx



3.2.1.3 Clear Channel Assessment

Clear Channel Assessment (CCA) is used to determine the current state of the wireless medium.

3.2.1.4 Automatic Gain/DC Control/RSSI/Noise Floor

The 88W8782 can be configured for one receive path. The device contains a single gain control module, one RF DC loops, and one digital DC loops.

The gain and RF DC control interfaces share a 5-bit command bus. Gain commands always have priority over the DC commands.

AGC

The AGC circuitry is capable of coarse and fine gain adjustments based on peak detections from the radio, ADC output saturation monitoring, and gain target comparison at low pass filter (ACR LPF) output.

Enhanced AGC for DFS

The 88W8782 enhanced AGC has been designed to provide faster gain convergence and higher ACI rejection for received signals.

For 5 GHz DFS channels, the AGC is designed in conjunction with the DFS block to improve the detection rate of short (0.5 µs, 0.8 µs, 1 µs) DFS pulses and to detect if received DFS pulses are in-band or out-of-band.

DC Offset

There are two stages for DC offset compensation. The RF DC loop is active from the receiver turned on before the packet arrives. After the packet arrives, the digital DC loop is activated to compensate for residual DC offsets from the previous stage. Both the RF DC loop and digital DC loop maintain their compensation values after the packet. The compensation values are updated when the device is in receiving mode.

RSSI/Noise Floor

Noise floor is a filtered total AGC gain when there is no signal present at the antenna input. The noise floor is updated continuously until a signal arrives that triggers gain unlock. The RSSI is the instantaneous total AGC gain captured at the beginning of a legacy 802.11g long training field, at the end of high throughput short training field, or at the end of SFD for 802.11b packets.

3.2.2 Dynamic Frequency Selection

The 88W8782 baseband supports 802.11h Dynamic Frequency Selection (DFS) to detect the presence of radar signals.

3.2.2.1 Enhanced DFS for Short Radar Pulse

The 88W8782 enhanced DFS scheme (in conjunction with the enhanced AGC for DFS) is designed to increase pulse detection rates for shorter (0.5 µs, 0.8 µs, 1 µs), in-band DFS pulses. The scheme is designed to minimize the false-alarm rate for out-of-band DFS pulses.

3.2.2.2 In-Service Monitoring

During in-service monitoring, all stations are enabled.

3.2.3 802.11k Radio Resource Measurement

The 88W8782 WLAN Baseband supports 802.11k (draft) noise histogram computations.

3.2.4 802.11n Optional Features

The 88W8782 baseband supports the following optional features of the 802.11n specification.

3.2.4.1 20/40 MHz Coexistence

The 20/40 MHz feature enables the device to co-exist with legacy devices when operating in 40 MHz mode. While the HT link is able to achieve high data rates per the 802.11n specification, legacy and HT devices operating in the 20 MHz extension channels can experience significant drops in throughput as a result.

First generation 802.11n devices that transmit conservatively by raising their CCA in the event of any activity detection in the 40 MHz channel tend to experience reductions in throughput of the HT link. On the other hand, more aggressive methods of transmitting over the 40 MHz channel when free (with no consideration to the extension channel activity) can diminish throughout of the network in the extension channel.

3.2.4.2 Space-Time Block Coding

The device supports single stream reception of Space-Time Block Coding (STBC) packets from MCS0 to MCS7.

3.2.4.3 Short Guard Interval

The 88W8782 baseband supports a short Guard Interval (GI) for both 20 and 40 MHz operation.

3.2.4.4 Reduced Inter-Frame Spacing

The 88W8782 baseband supports the Reduced Inter-Frame Spacing (RIFS) feature for the receive path to shorten the delay between OFDM transmissions when operating in an OFDM-only network.

3.2.4.5 Greenfield Tx/Rx

The 88W8782 baseband supports greenfield packet formats to improve efficiency in an all 802.11n network.

3.2.4.6 Beamformee and Hardware Acceleration

The 88W8782 baseband supports explicit beamformee to improve the range of 802.11n data rates. Non-compressed or compressed steering matrices may be fed back to the beamformer. Receiving both NDP and “squared” sounding (required by Wi-Fi) are supported with up to 4 transmit antennas at the beamformer.

The baseband and MAC hardware applies a simplified, but near optimal, steering matrix computation algorithm, as well as a simple non-compressed and compressed feedback frame formation logic. Therefore, immediate feedback (within SIFS) is available in the case of NDP sounding. This is beneficial for high mobility environments.

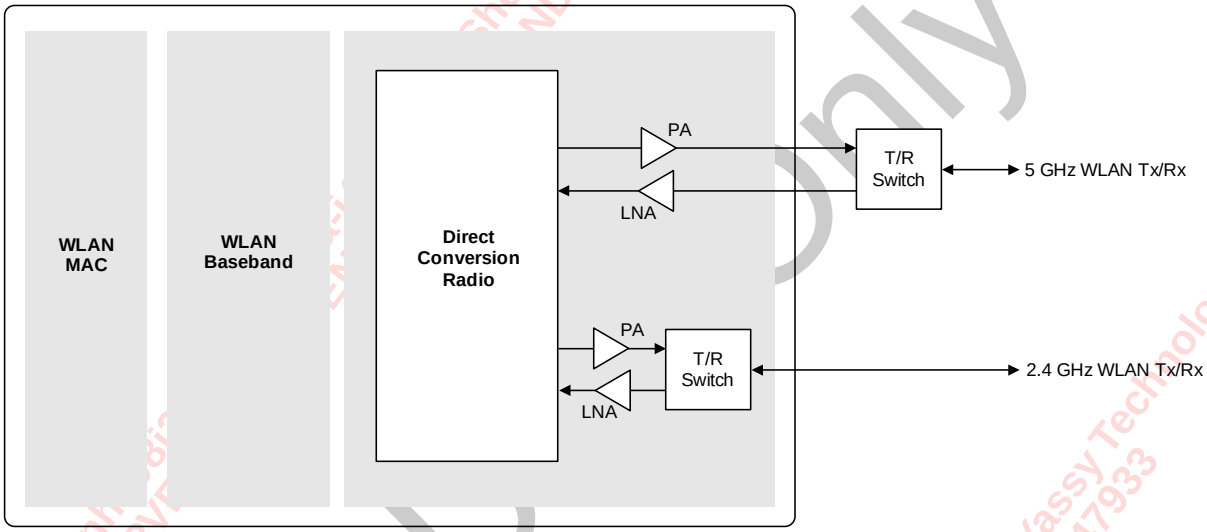
Delayed feedback is also supported for both sounding formats. Furthermore, the baseband hardware supports substream SNR and MCS (optional) feedback together with the beamforming feedback, allowing the beamformer to choose the correct MCS for the steered packets.

3.3 WLAN Radio

The 88W8782 direct conversion WLAN RF radio integrates all the necessary functions for transmit and receive operation.

Figure 23 shows a simplified block diagram of the WLAN radio.

Figure 23: WLAN Radio Block Diagram



3.3.1 Programmable Frequency Synthesizer

3.3.1.1 Frequency Channel Support

Table 16–Table 19 show the high rate frequency channels supported for operation in the 2.4 GHz ISM and 5 GHz UNII radio bands.

Table 16: 802.11g Channels Supported

Channel	Frequency (GHz)	North America	Europe	Spain	France	Japan MKK
1	2.412	X	X	--	--	X
2	2.417	X	X	--	--	X
3	2.422	X	X	--	--	X
4	2.427	X	X	--	--	X
5	2.432	X	X	--	--	X
6	2.437	X	X	--	--	X
7	2.442	X	X	--	--	X
8	2.447	X	X	--	--	X
9	2.452	X	X	--	--	X
10	2.457	X	X	X	X	X
11	2.462	X	X	X	X	X
12	2.467	--	X	--	X	X
13	2.472	--	X	--	X	X
14	2.484	--	--	--	--	--

Table 17: 802.11a Channels Supported

Channel	Frequency (GHz)	North America	Europe	Spain	France	Japan MKK
36	5.180	X	X	X	X	--
40	5.200	X	X	X	X	--
44	5.220	X	X	X	X	--
48	5.240	X	X	X	X	--
52	5.260	X	X	X	X	--
56	5.280	X	X	X	X	--
60	5.300	X	X	X	X	--
64	5.320	X	X	X	X	--
149	5.745	X	X	X	X	--
153	5.765	X	X	X	X	--
157	5.785	X	X	X	X	--
161	5.805	X	X	X	X	--
165	5.825	X	X	X	X	--

Table 18: 802.11h Channels Supported

Channel	Frequency (GHz)	North America	Europe	Spain	France	Japan MKK
100	5.500	X	X	X	X	--
104	5.520	X	X	X	X	--
108	5.540	X	X	X	X	--
112	5.560	X	X	X	X	--
116	5.580	X	X	X	X	--
120	5.600	X	X	X	X	--
124	5.620	X	X	X	X	--
128	5.640	X	X	X	X	--
132	5.660	X	X	X	X	--
136	5.680	X	X	X	X	--
140	5.700	X	X	X	X	--

Table 19: 802.11n Channels Supported (Japan)

Channel		Frequency (GHz)	North America	Europe	Spain	France	Japan MKK
1	5	2.422	X	X	X	X	--
2	6	2.427	X	X	X	X	--
3	7	2.432	X	X	X	X	--
4	8	2.437	X	X	X	X	--
5	9	2.442	X	X	X	X	--
6	10	2.447	X	X	X	X	--
7	11	2.452	X	X	X	X	--
36	40	5.190	X	X	X	X	--
44	48	5.230	X	X	X	X	--
52	56	5.270	X	X	X	X	--
60	64	5.310	X	X	X	X	--
100	104	5.510	X	X	X	X	--
108	112	5.550	X	X	X	X	--
116	120	5.590	X	X	X	X	--
124	128	5.630	X	X	X	X	--
132	136	5.670	X	X	X	X	--
149	153	5.755	X	X	X	X	--
157	161	5.795	X	X	X	X	--

3.3.1.2 Programming Channel Frequencies

The RF radio channel frequency is programmed through the RF registers.

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3.4 WLAN Encryption

The 88W8782 Advanced Wireless Encryption Unit (WEU) is compliant to the 802.11i MAC Security Enhancements. The WEU contains hardware support for encryption/decryption using:

- Advanced Encryption Standard (AES) / Counter-Mode/CBC-MAC Protocol (CCMP)
- Advanced Encryption Standard (AES) / Cipher-Based Message Authentication Code (CMAC)
- WLAN Authentication and Privacy Infrastructure (WAPI)
- Wired Equivalent Privacy (WEP) / Temporal Key Integrity Protocol (TKIP)

CCMP uses the AES algorithm with a 128-bit key for encryption, decryption, and Message Integrity Code (MIC) generation. CCMP protects the integrity of both MPDU data field and selected portion of the IEEE 802.11 MPDU header. Refer to Federal Information Processing Standard (FIPS) PUB 197 for further information on the AES algorithm.

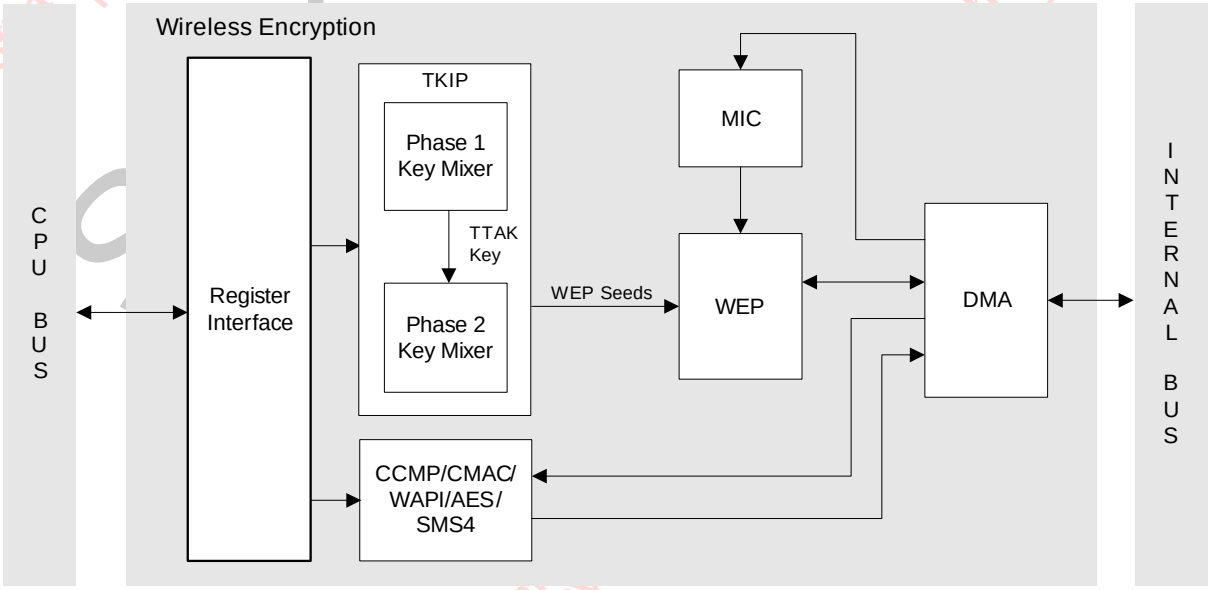
The Broadcast/Multicast Integrity Protocol (BIP) provides forgery protection for robust broadcast/multicast management frames using AES-128-CMAC for message integrity. The BIP protocol also provides replay protection. Refer to the NIST Special Publication 800-38B for more information.

WAPI is a Chinese National Standard for WLAN (GB 15629.11-2003). The WAPI standard is similar to IEEE 802.11i and Wi-Fi Alliance WPA/WPA2 specifications. WAPI uses the underline SMS4 algorithm for encryption and decryption. For more information, refer to "Security Analysis of WAPI Authentication and Key Exchange", Xinghua Li, Jianfeng Ma, and SangJae Moon, Lecture Notes in Computer Science, Network and Parallel Computing.

TKIP uses the WEP cipher algorithm with 128-bit temporal key for encryption and decryption.

Figure 24 shows a block diagram of the WEU.

Figure 24: Wireless Encryption Block Diagram



3.4.1 CCMP/CMAC/WAPI

The 88W8782 crypto engine can perform either CCMP/CMAC/WAPI encryption or decryption operation on a programmable length of data under firmware control.

Features include:

- Support for 128-bit key size
- Support for encryption and decryption operations
- Counter Mode with CBC-MAC Protocol (CCMP) processing mode
  - Message Integrity Code (MIC) over packet data and partial MPDU header
  - Counter mode encryption generation and checking
- AES-128 CMAC for message integrity
- WAPI protocol processing mode
  - Key expansion
  - MIC generation and checking
- Interrupt and status flags for the CPU upon completion

3.4.2 WEP/TKIP

WEP relies on an encryption/decryption algorithm used in the IEEE 802.11 standard. The algorithm is a symmetric stream cipher. The same key and algorithm are used for both encryption and decryption. Key management is performed by firmware.

TKIP processing is supported when performing WEP processing (64- or 128-bit).

4 Coexistence

The Marvell coexistence framework is based on the IEEE 802.15.2 recommended practice Packet Traffic Arbitration (PTA) scheme. This scheme is recommended for next generation mobile phones.

4.1 WLAN/Bluetooth Channel Information Exchange

Since Bluetooth and 802.11g/b and 802.11n WLAN use the same 2.4 GHz frequency band, each can cause interference with one other. The level of interference depends on the respective frequency channel used by Bluetooth and WLAN (other factors can impact interference, like Tx power and Rx sensitivity of the device).

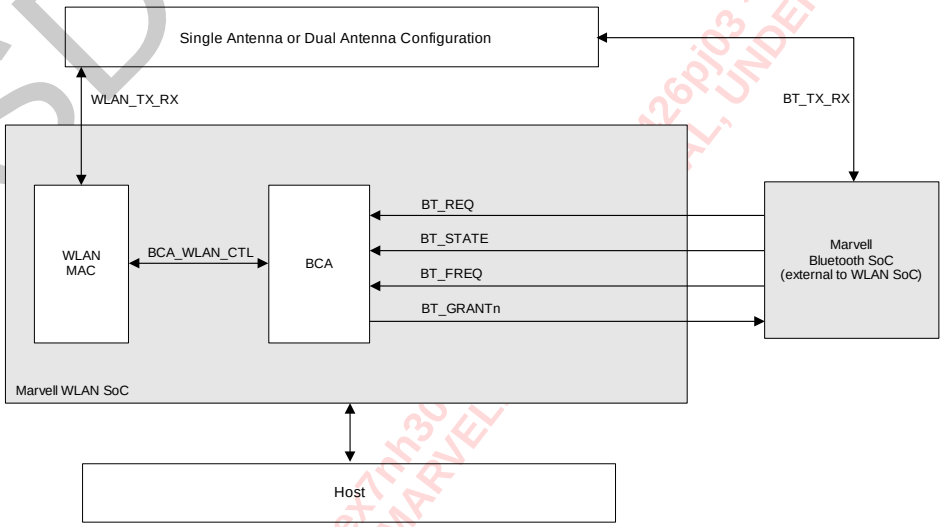
In a system with both Bluetooth and WLAN, the common host receives information about WLAN channel usage and passes this information to the Bluetooth device. For Bluetooth 1.2 devices with Adaptive Frequency Hopping (AFH) enabled, the Bluetooth device can block channel usage that overlaps the WLAN channel in use.

When the Bluetooth device avoids all channels used by the WLAN, the impact of interference is greatly reduced, but not completely eliminated. For Bluetooth 1.1 devices, the Bluetooth device cannot block WLAN channel usage. In this case, an active BCA scheme at the MAC level is required. The BCA scheme can also be used with Bluetooth 1.2 devices to further reduce the impact of interference to a minimum.

4.2 System Configuration

The 88W8782 WLAN MAC/BCA supports a coexistence interface for external, co-located 2.4 GHz devices. Figure 25 shows the configuration.

Figure 25: System Configuration—Top Block Diagram[1]



1. Antenna can be used as an option to enhance performance.

4.3 Bluetooth Coexistence Interface (BCI)

The 88W8782 supports the following Bluetooth Coexistence Interface (BCI) modes:

- Marvell 3/4-wire
- WL_ACTIVE 2-wire
- WL_ACTIVE 3/4-wire
- 1-wire

Only one co-located device can be attached to the interface.

4.3.1 Marvell 3/4-Wire

- BT_REQ—BCA input signal to inform that the Bluetooth device requests access to the medium.
- BT_GRANTn—BCA output signal to indicate permission to Tx. If low, the Bluetooth device can Tx. This signal stays low for the duration of Bluetooth transmission. Depending on the configuration of the BCA, this signal can also indicate permission to Rx.
- BT_STATE—BCA input signal to inform of the BT_REQ priority (1- or 2-bit) and the direction of the Bluetooth data (Tx or Rx).
- BT_FREQ (4-wire only)—BCA input signal to inform whether Bluetooth traffic will be using a channel that overlaps with the WLAN channel (in-band) or not (out-band). To use this, the host system must know what WLAN channel is being used and program the Bluetooth device with a list of Bluetooth channels considered to be overlapping.

4.3.2 WL_ACTIVE 2-Wire

- BT_PRIORITY—BCA input signal to indicate that high priority Bluetooth traffic is about to be exchanged between the Bluetooth devices. The assertion of this signal should proceed the actual Bluetooth packet slot time. De-assertion of this signal does not necessarily mean that there is no Bluetooth activity.
- WL_ACTIVE—BCA output signal to indicate the WLAN is active (either Tx or Rx packets). The Bluetooth device should defer all transmissions when WL_ACTIVE is high, except for high priority transmissions. Some devices may also defer high priority transmissions.

Both signals are active high signals.

4.3.3 WL_ACTIVE 3/4-Wire

- BT_ACTIVE—BCA input signal to indicate that a Bluetooth traffic is about to be exchanged between the Bluetooth devices. The assertion of this signal should proceed the actual Bluetooth packet slot time, and cover the duration of the transfer.
- BT_PRIORITY0—BCA input signal to indicate priority Bit[0] of Bluetooth packet. Signal is valid for entire BT_ACTIVE assertion.
- BT_PRIORITY1 (4-wire only)—BCA input signal to indicate priority Bit[1] of Bluetooth packet. Signal is valid for entire BT_ACTIVE assertion.
- WL_ACTIVE—BCA output signal to indicate the WLAN is active (either Tx or Rx packets).

Both signals are active high signals.

4.3.4 1-Wire

- BT_REQ—BCA input signal to indicate the Bluetooth device requests access to the medium. The assertion of this signal precedes the actual Bluetooth packet slot time. De-assertion occurs after the end of the last byte of data. When asserted, the WLAN device is stopped from transmitting.

4.4 BCA Capability

The Marvell BCA can be configured for various systems and use cases.

- Programmable BCI timing, interface modes, and signal polarity to support a variety of external Bluetooth devices
- Programmable RF switch control for single, dual, and hybrid antenna configurations
- Programmable decision policies and transaction lock behavior for various use cases
- Interface with external or on-chip Bluetooth module (depends on product specification)
- Support Bluetooth 1.1 or Bluetooth 1.2 AFH
- WLAN/Bluetooth coordinated low-power design
- Enhanced information sharing between WLAN and Bluetooth for combo systems

4.4.1 Marvell BCI

The Marvell BCI is a a serial-based signaling scheme that uses 3 or 4 wires and allows more information to be transferred compared to the WL_ACTIVE BCI. Priority and direction are multiplexed on the BT_STATE line, with room for more information without additional lines. BT_GRANTn is a direct grant indication for Bluetooth.

4.4.2 WL_ACTIVE BCI

The WL_ACTIVE BCI is a parallel-based signaling scheme that uses between 2 to 4 signals. The scheme transfers activity and priority information on separate lines, and grant information is inferred.

Marvell supports this parallel-based signaling scheme, but does not recommend its use due to limited grant control and lack of directional information.

4.4.3 Arbitration

Arbitration is performed when there is contention between WLAN and Bluetooth requests. The contention is resolved by a customizable decision matrix that allows independent grant decision for each device. Both devices can be granted access at the same time.

The vectors for the decision matrix include:

- WLAN priority (2-bit)
- WLAN direction
- Bluetooth priority (1- or 2-bit)
- Bluetooth direction
- Bluetooth frequency in/out-band

The decision matrix is optimized for performance in each usage scenario and system configuration. The system designer can override decision outcomes at any time.

4.4.3.1 AFH

If AFH is enabled in the Bluetooth device, and there is sufficient guard-band outside the WLAN operating frequency, the Bluetooth device uses the OutOfBand (OOB) channel with respect to the WLAN device. Otherwise, the Bluetooth device uses the InBand (IB) and OOB channels with respect to the WLAN device.

The IB and OOB information is either provided by the Bluetooth device through the BCI, or can be provided through firmware controls in a shared-host system. IB/OOB is a vector in the decision matrix.

4.4.3.2 Decision Policies

System configuration is a major factor in the planning of decision policies. The configuration governs how RF paths are shared and how much interference there will be. There are four interference combinations between WLAN and Bluetooth:

- WLAN Tx and Bluetooth Tx
- WLAN Tx and Bluetooth Rx
- WLAN Rx and Bluetooth Tx
- WLAN Rx and Bluetooth Rx

Reasonable policies for devices running in a dual-antenna configuration include:

- WLAN Tx and Bluetooth Tx in OOB situation have little interference impact on each other. Therefore, the decision matrix grants both.
- WLAN Tx and Bluetooth Tx in IB situation have a sizable interference impact on each other. Therefore, the decision matrix allows either WLAN or Bluetooth Tx, based on relative packet priorities.
- WLAN Tx and Bluetooth Rx (both OOB and IB) have sizable interference impacts on Bluetooth Rx. Therefore, the decision matrix grants or denies WLAN Tx based on relative packet priorities.
- WLAN Rx and Bluetooth Tx (both OOB and IB) have sizable interference impacts on WLAN Rx. Therefore, the decision matrix grants or denies Bluetooth Tx based on relative packet priorities.
- WLAN Rx and Bluetooth Rx (both OOB and IB) have no impact on each other. Therefore, the decision matrix grants both.

For the devices running in a basic single-antenna configuration, the linear switching imposes restrictions on simultaneous transfers. Reasonable policies include:

- WLAN and Bluetooth are never granted at the same time
- Decision matrix grants a device based on relative packet priorities and direction
- Priority order: Hi > Medium Hi > Medium > Low
- For equal priority contention, select one device to win that optimizes usage case

For devices running in an enhanced single-antenna configuration, the linear switching imposes restrictions on some simultaneous transfers. The policies for this configuration may be a combination of dual-antenna and basic single-antenna policies.

4.4.3.3 Transaction Stopping

The arbiter allows control of what transfers can be stopped after an initial grant. If allowed, a transaction can be stopped for a higher priority request. A transaction stop decision is a function of the decision policies and transaction stopping control. The transaction stopping control is configurable per device and direction.

4.5 WLAN Capability

The WLAN uses an internal coexistence interface (WCI) to exchange request/grant with the BCA. Features of the WCI include:

- Packet-based request signaling with direction and priority information
- 1- or 2-bit priority signaling to support four priority levels
- Multiple WLAN Rx request trigger sources, including early prediction
- WLAN Tx request cancellation and abort if grant denied or revoked in middle of request
- 802.11n AMPDU treated as single packet

4.5.1 WLAN Packet Classification

- Programmable mask allows each frame type to be mapped to a priority
- Default setting puts response frames (i.e., ACK), beacons, and QoS frames as high priority
- WLAN Tx and Rx have separate priority masks

4.5.2 WLAN Queue Classification

- Programmable mask allows each transmit queue to be mapped to a priority
- Queue-based mapping is optional for software-generated frames only

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5 Host Interface

The 88W8782 bus interface connects host interface bus units to the CPU bus of the device via the internal bus. The connection of each unit is multiplexed with other bus units.

5.1 SDIO Interface

The 88W8782 supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

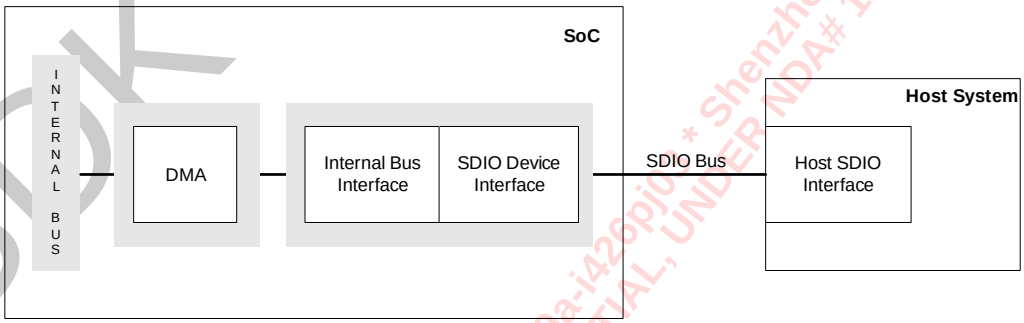
The 88W8782 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

The SDIO device interface main features include:

- On-chip memory used for CIS
- Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer modes at the full clock range of 0 to 50 MHz
- Special interrupt register for information exchange
- Allows card to interrupt host

Figure 26 shows the interface circuitry between an external SDIO bus and the internal shared bus.

Figure 26: SDIO Interface Block Diagram



5.1.1 SDIO Interface Signal Description

Table 20 shows the signal mapping between the 88W8782 device and the SDIO specification.

See Section 1.4, Configuration Pins, on page 38 for host interface configuration settings.

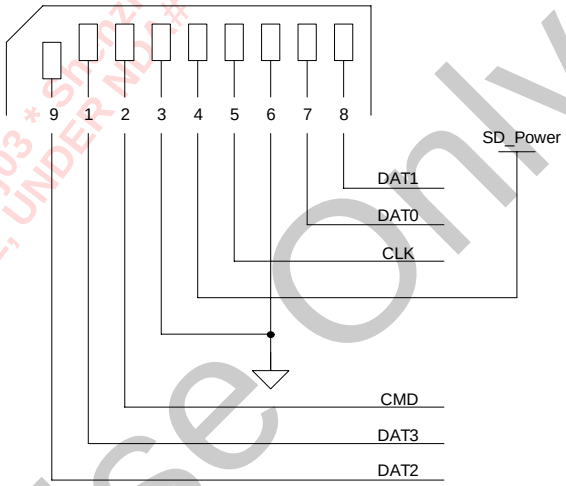
Table 20: SDIO Interface Signal Description

88W8782 Pin Name	Signal Name	Type	Description
SD_CLK	CLK	I/O	SDIO 1-bit mode: Clock SDIO SPI mode: Clock
SD_CMD	CMD	I/O	SDIO 1-bit mode: Command line SDIO SPI mode: Data input
SD_DAT[3]	DAT3	I/O	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used SDIO SPI mode: Chip select (active low)
SD_DAT[2]	DAT2	I/O	SDIO 4-bit mode: Data line bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional) SDIO SPII mode: Reserved
SD_DAT[1]	DAT1	I/O	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt SDIO SPI mode: Interrupt
SD_DAT[0]	DAT0	I/O	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line SDIO SPI mode: Data output

5.1.2 SDIO Interface Functional Description

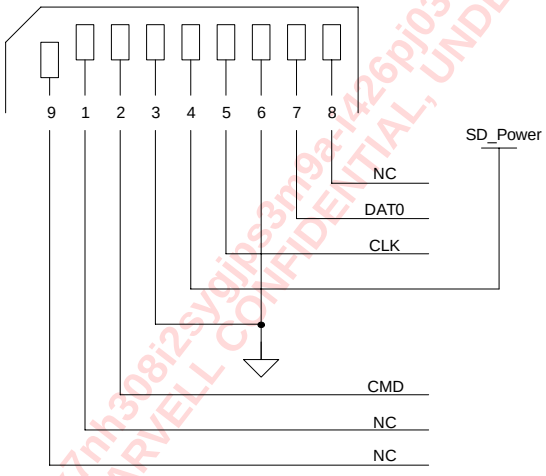
5.1.2.1 SDIO Connection/Function

Figure 27: SDIO Physical Connection—4-Bit Mode[1]



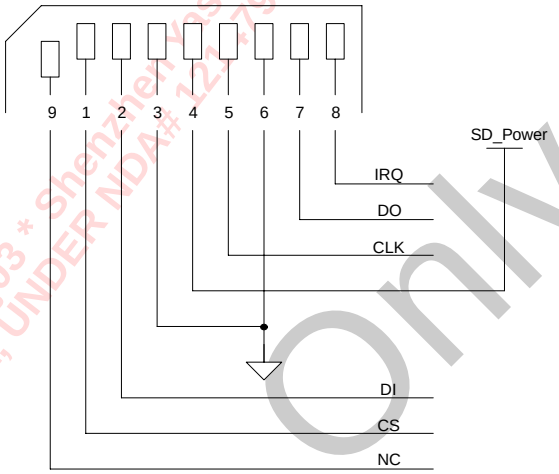
1. In 4-bit SDIO mode, data is transferred on all 4 data pins (DAT[3:0]), and the interrupt pin is not available for exclusive use as it is utilized as a data transfer line. Thus, if the interrupt function is required, a special timing is required to provide interrupts. The 4-bit SDIO mode provides the highest data transfer possible, up to 100 Mbps.

Figure 28: SDIO Physical Connection—1-Bit Mode[1]



1. In 1-bit SDIO mode, data is transferred on the DAT[0] pin only. Pin 8, which is undefined for memory, is used as the interrupt pin.

Figure 29: SDIO Physical Connection—SPI Mode[1]



1. Pin 8, which is undefined for memory, is used as the interrupt pin in SPI mode.

Table 21: SDIO Electrical Function Definition—1-bit

Pin	SDIO 1-bit Mode	
1	N/C	Not used
2	CMD	Command line
3	VSS1	Ground
4	VDD	Supply voltage
5	CLK	Clock
6	VSS2	Ground
7	DATA	Data line
8	IRQ	Interrupt
9	RW	Read Wait (optional)

Table 22: SDIO Electrical Function Definition—SPI

Pin	SPI Mode	
1	CS	Card Select
2	DI	Data input
3	VSS1	Ground
4	VDD	Supply voltage
5	SCLK	Clock
6	VSS2	Ground
7	DO	Data output
8	IRQ	Interrupt
9	NC	Not used

Table 23: SDIO Electrical Function Definition—4-bit

Pin	SDIO 4-bit Mode	
1	CD/DAT[3]	Data line 3
2	CMD	Command line
3	VSS1	Ground
4	VDD	Supply voltage
5	CLK	Clock
6	VSS2	Ground
7	DAT[0]	Data line 0
8	DAT[1]	Data line 1 or Interrupt (optional)
9	DAT[2]	Data line 2 or Read Wait (optional)

5.1.2.2 SDIO Command List

All mandatory SDIO commands are supported.

Table 24: SDIO Mode, SDIO Commands

Command	Command Name	Description
CMD0	GO_IDLE_STATE	Used to change from SDIO to SPI mode
CMD3	SEND_RELATIVE_ADDR	SDIO Host asks for RCA
CMD5	IO_SEND_OP_COND	SDIO Host asks for and sets operation voltage
CMD7	SELECT/DESELECT_CARD	Sets SDIO target device to command state or back to standby
CMD15	GO_INACTIVE_STATE	Sets SDIO target device to inactive state
CMD52	IO_RW_DIRECT	Used to read/write host register and CIS table
CMD53	IO_RW_EXTENDED	Used to read/write data from/to SQU memory

Table 25: SPI Mode, SDIO Commands

Signal Name	Type	Description
CMD0	GO_IDLE_STATE	Used to change from SDIO to SPI mode
CMD5	IO_SEND_OP_COND	Used in initialization state
CMD52	IO_RW_DIRECT	Used to read/write host register and CIS table
CMD53	IO_RW_EXTENDED	Used to read/write data from/to SQU memory
CMD58	CRC_ON_OFF	Enable/disable CRC (SPI only)

6 Peripheral Bus Interface

The 88W8782 Peripheral Bus Unit (PBU) connects several low speed peripherals to the CPU bus of the device. The PBU buffers up to eight data units per bus transaction and supports both single and burst transfer modes.

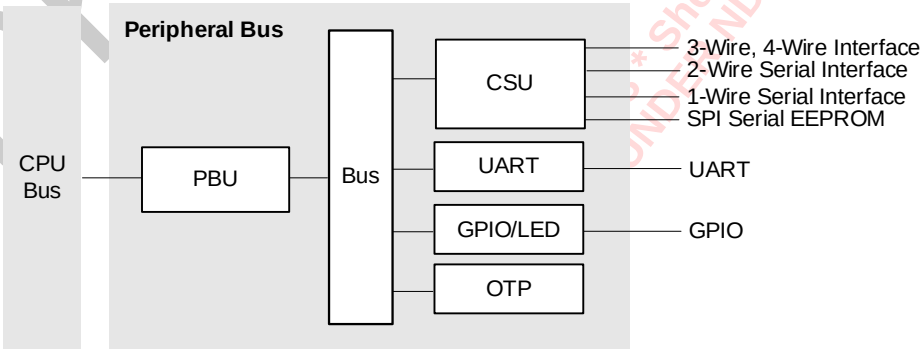
Features supported include:

- Clocked Serial Unit(CSU)
  - 3-Wire, 4-Wire (3W4W) Interface
  - 2-Wire Serial Interface (TWSI)
  - 1-Wire Serial Interface
  - SPI Serial (EEPROM) Interface
- UART Interface
- GPIO Interface
- One-Time Programmable Memory (OTP)

6.1 Data Flow

Figure 30 shows the connection of low speed peripherals to the CPU bus. Data flow through the PBU is from the CPU bus interface through a FIFO to one of the peripheral devices. The peripheral device handles input and output operations to and from the external destination. Access to peripheral host devices occurs through CPU writes to the PBU address space.

Figure 30: PBU Block Diagram



6.2 Operation

The PBU has two synchronous FIFOs, one for transmit data and the other for receive data. The FIFOs cross clock domains between the internal bus and peripheral bus clock domains.

When the PBU intends to receive any cycles on the internal PBU, it must first wait until any current transactions are complete. Both sides of the PBU are synchronized by internal transmit and receive start and done signals.

6.3 Control

- Generate a peripheral soft reset
- Configure peripheral clock speeds

6.3.1 Soft Reset

Soft reset generates a 4-cycle length active low pulse after the rising edge of PCLK to initialize peripheral devices to their default states.

6.3.2 Peripheral Clock Speeds

Peripheral clock speeds are computed by the equation: PCLK = UART

6.4 Clocked Serial Unit

The CSU is used to exchange data with the RF radio, baseband, and external serial EEPROM.

The CSU provides a read-only status to monitor the activity of low speed peripherals. Features include:

- Single host operation
- Programmable serial clock frequency

The CSU supports the following serial synchronous bus protocols for serial interface operation:

- 3-Wire, 4-Wire Serial Interface
- 2-Wire Serial Interface
- 1-Wire Serial Interface
- SPI Serial EEPROM Interface

6.4.1 Serial Clock Frequency

The CSU uses the internal PCLK signal in the PBU to generate the correct serial clock frequency. In addition, it applies a clock prescaler to clock the input and output data to external devices.

6.4.2 3-Wire, 4-Wire Interface

The clock prescaler is based on the following equation, where SCLK is the serial clock, PCLK is the PBU internal clock, and PRER is the clock prescaler:

$$SCLK = \frac{PCLK}{2 \bullet (PRER + 1)}$$

6.4.3 2-Wire Serial Interface

The 88W8782 2-Wire Serial Interface (TWSI) is an interface bridge between a 2-wire serial bus and the CPU. The main features of TWSI include:

- Programmable serial clock frequency
- Single master operation
- Single and multi-byte data transfer with minimum CPU interrupts
- MAC parallel interface for back-door access to external RF device
- Internal clock gating based on mode select
- Double read buffer

6.4.3.1 Interface Description

Table 26 shows the pins used to connect to TWSI EEPROM.

Table 26: TWSI EEPROM Interface Description

88W8782 Pin Name	EEPROM Pin Name	Description
SER_WB	SO	Serial Read/Write Control Signal (input) Not used.
SER_CLK	SCK	Serial Clock Signal (input/output) EEPROM serial clock to/from the SoC/EEPROM.
SER_DAT	SI	Serial Data (input/output) EEPROM serial data to/from the SoC/EEPROM.
SER_CSn	CS	Chip Select (output) Not used.

6.4.3.2 Serial Clock Frequency

For TWSI mode, the clock prescaler is based on the following equation, where SCLK is the serial clock, PCLK is the PBU internal clock, and PRER is the clock prescaler:

$$SCLK = \frac{PCLK}{5 \bullet (PRER + 1)}$$

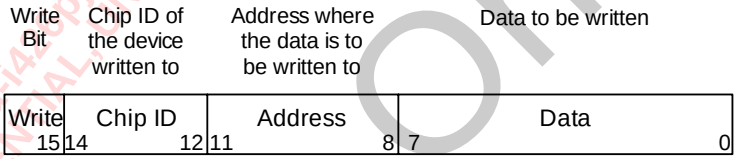
6.4.4 1-Wire Serial Interface

The 88W8782 can be combined with the Marvell 88PG8211 power management device (PMIC) to achieve ultra-low power consumption. Each 88PG8211 buck/LDO can be individually programmed to power up, power down, or sleep.

A 1-wire serial interface (W1_CNTL) is used between the 88W8782 and 88PG8211 and is clocked by the PMIC clock of the 88W8782.

The 88PG8211 has eight, 8-bit registers that are programmable (write-only) by the 88W8782. The 88PG8211 has a chip ID (101 or 010) on the interface for identification, as shown in Figure 31.

Figure 31: 1-Wire Data Format



6.4.5 SPI EEPROM

The 88W8782 supports a SPI EEPROM device to hold constants such as MAC address, CIS tables, or code for the internal processor. The 88W8782 supports 1-, 2-, and 3-byte address modes, which allows for EEPROM sizes from 4 KB to 1 MB. The SPI interface can run up to 16 MHz.

Note Internal Boot ROM can access 2- and 3-byte addresses only.

6.4.5.1 Interface Description

Table 27 shows the pins used to connect to SPI EEPROM.

Table 27: SPI EEPROM Interface Description

88W8782 Pin Name	EEPROM Pin Name	Description
SER_WB	SO	Serial Read/Write Control Signal (input) EEPROM serial data from the EEPROM to the SoC.
SER_CLK	SCK	Serial Clock Signal (output) EEPROM serial clock from the SoC to the EEPROM.
SER_DAT	SI	Serial Data (output) EEPROM serial data from the SoC to the EEPROM.
SER_CSn	CS	Chip Select (output) EEPROM chip select from the SoC to the EEPROM.

6.4.5.2 Boot from SPI EEPROM

When CON[2:0] are programmed, firmware reads and executes boot information from the SPI EEPROM.

See Section 1.4, Configuration Pins, on page 38.

- EEPROM size must be sufficiently large for firmware code when booting from EEPROM.
- Marvell supports a 2-byte or 3-byte address for SPI EEPROM.

6.4.5.3 SPI EEPROM External Memory

The SPI EEPROM can be used to store MAC addresses or other data. To access the EEPROM, the CPU executes read and write operations through the PBU unit ID into the CSU address space.

6.4.5.4 Write and Read Sequence

Byte Write

The 88W8782 supports the following Write instructions.

- WRITE—Simple Write instruction
- WRSR—Write to the EEPROM Status Register
- WREN—Write Enable command to the EEPROM
- WRDI—Write Disable command to the EEPROM

Figure 32: Byte Write Signal Diagram

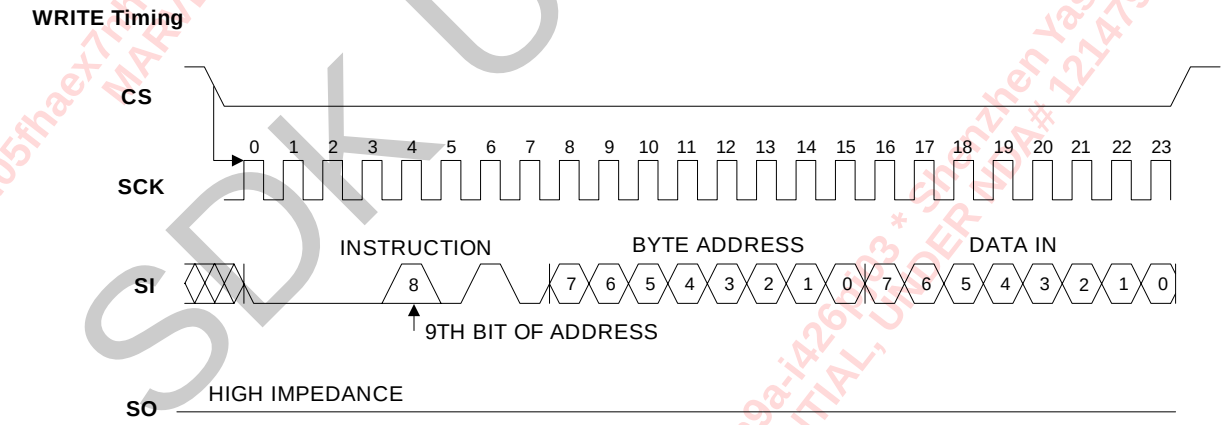
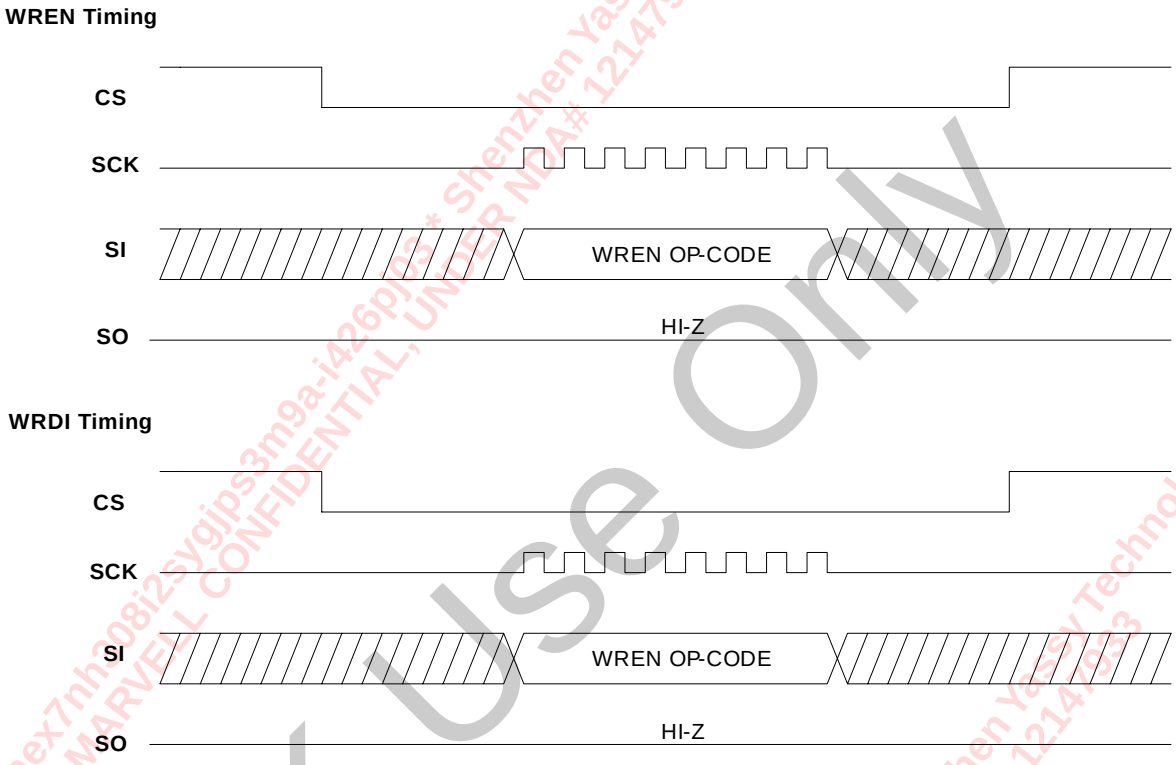


Figure 33: Write Enable and Write Disable Signal Diagrams

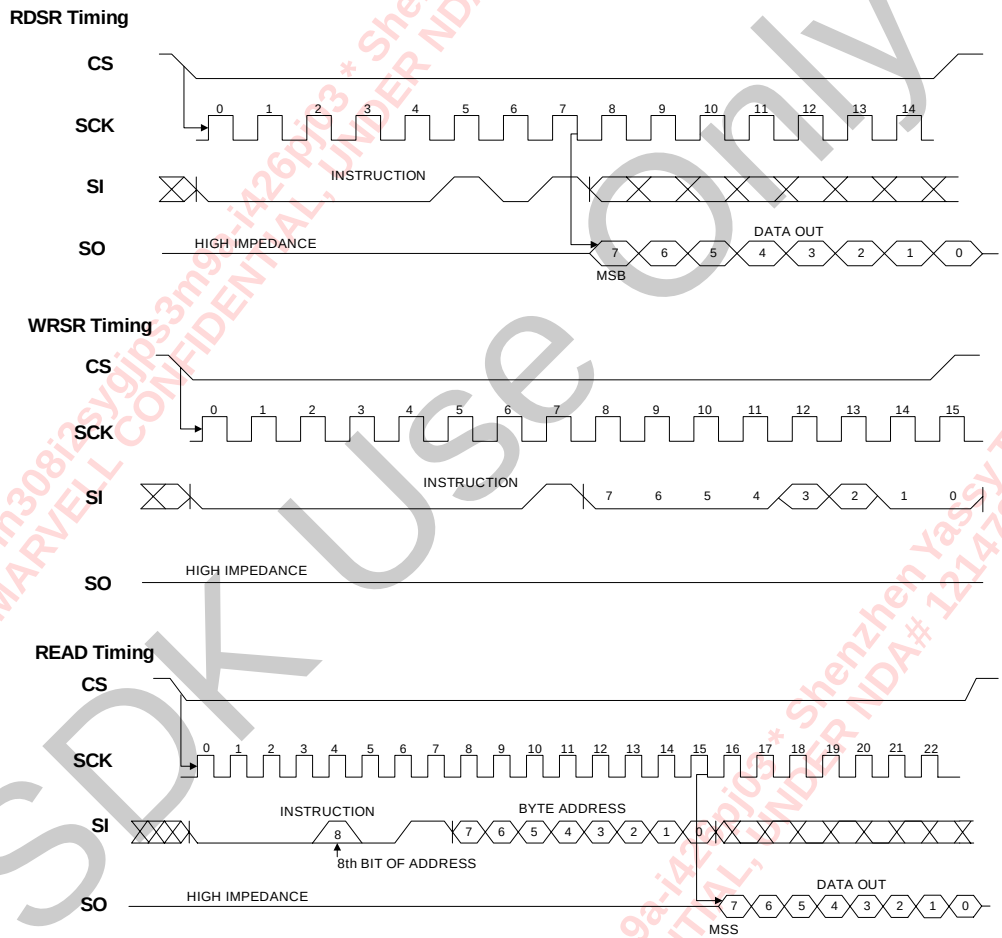


Byte Read

The 88W8782 supports the following read instructions.

- READ—Simple Read instruction
- RDSR—Read the EEPROM Status Register

Figure 34: Byte Read Signal Diagram



6.5 UART Interface

The 88W8782 supports a high speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification.

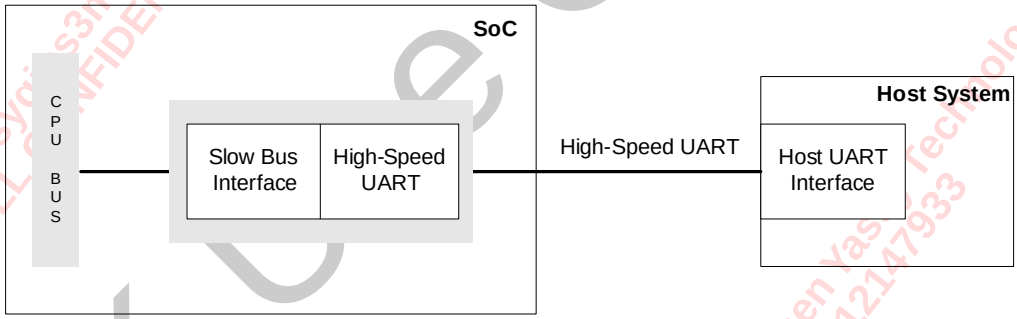
The UART interface features include:

- FIFO mode permanently selected for transmit and receive operations
- Two pins for transmit and receive operations
- Interrupt triggers for low-power, high throughput operation

The UART interface operation includes:

- Upload boot code to the internal CPU (for debug purposes)
- Support diagnostic tests
- Support data input/output operations for peripheral devices connected through a standard UART interface

Figure 35: High-Speed UART Interface Block Diagram



6.5.1 UART Interface Signal Description

Table 28 shows the standard UART signal names on the device.

Table 28: UART Pin Definitions

88W8782 Signal Name	16550 Standard Pin Name	Description
UART_SIN	SIN	Serial data input from modem, data set, or peripheral device
UART_SOUT	SOUT	Serial data output from modem, data set, or peripheral device

6.6 GPIO Interface

6.6.1 Overview

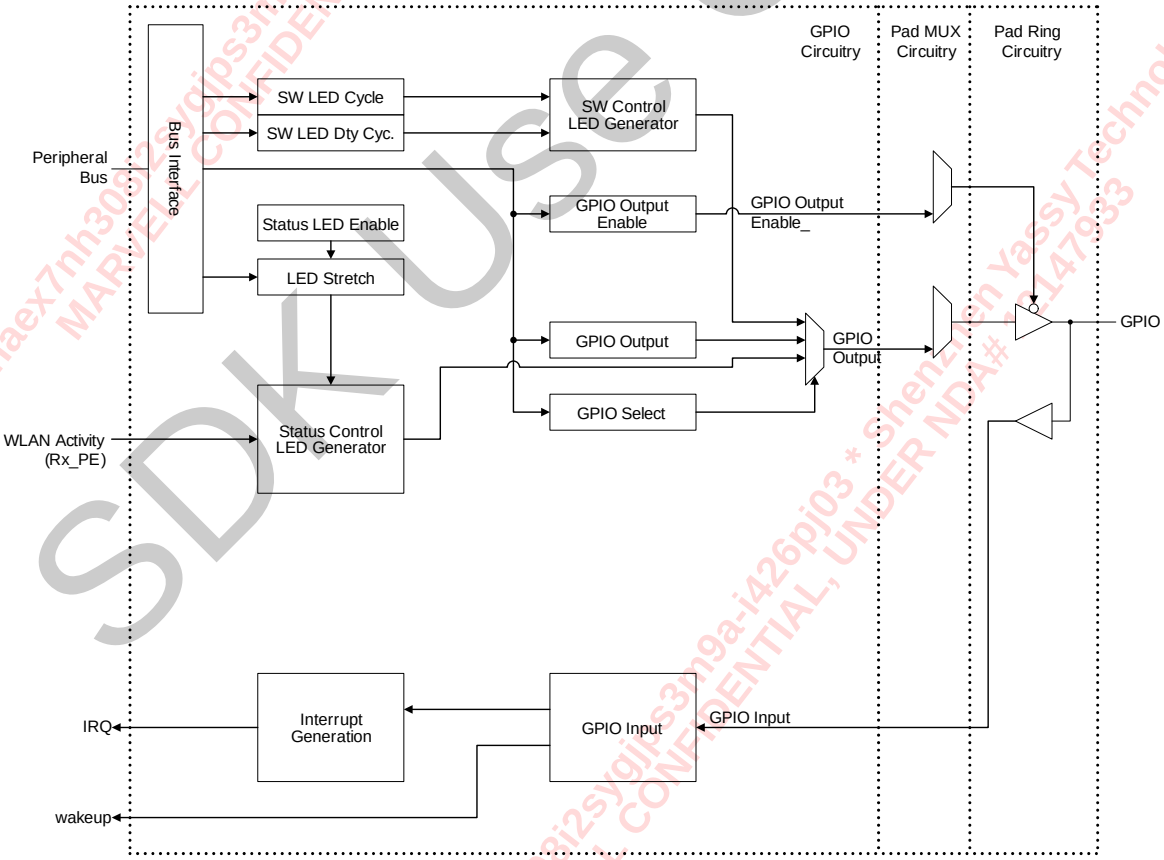
The General-Purpose I/O (GPIO) interface is used to implement user-defined input and output signals to and from the 88W8782 device, such as external interrupts, LED controlled outputs, and other user-defined I/Os.

The main features of the GPIO interface include:

- User-defined GPIOs; each I/O configured to either input or output
- Each GPIO independently controlled
- Each I/O configurable to output bit from GPIO_OUT[5:0]

Figure 36 shows a block diagram of the 88W8782 GPIO Unit (GPU). This circuitry exists for each of the GPIO pins, although some functions may be implemented only on certain pins.

Figure 36: GPU Block Diagram



6.6.2 GPIO Functions

Table 29 shows the general functions associated with each GPIO pin.

Table 29: GPIO Functions

GPIO Function	GPIO Pin					
	0	1	2	3	4	5
General Purpose						
Input	X	X	X	X	X	X
Output	X	X	X	X	X	X
LED						
LED Output	--	X	--	--	--	--

6.6.3 LED Pulse Stretching

LED statuses on the GPIO pins can be pulse-stretched. Pulse stretching is necessary, because the duration of these status events may be too short to be observable on the LEDs. The pulse-stretch duration can be programmed via register.

6.6.4 Blink Rate

The software controlled LEDs can indicate events by blinking LEDs. Blink rate periods are register programmable.

6.7 One-Time Programmable Memory

The 88W8782 includes a One-Time Programmable (OTP) memory to eliminate the need for an external EEPROM.

7 Electrical Specifications

7.1 Absolute Maximum Ratings

Table 30: Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
VDD12	Power supply voltage with respect to VSS	--	1.2	1.32	V
VIO	1.8V/2.6V/3.3V digital power supply	--	1.8	2.2	V
		--	2.6	3.1	V
		--	3.3	4.0	V
VDD33	Power supply voltage with respect to VSS	--	3.0	4.0	V
	Power supply voltage with respect to VSS	--	3.3	4.0	V
AVDD18	Power supply voltage with respect to VSS	--	1.8	1.98	V
AVDD33	Power supply voltage with respect to VSS	--	3.3	TBD[1]	V
AVDD33_USB	Power supply voltage with respect to VSS	--	3.3	4.1	V
LVLDO_VIN	Power supply voltage with respect to VSS	1.62	1.8	1.98	V
VBLDO_VIN	Power supply voltage with respect to VSS	3.0	3.3	4.8	V
VBLDO33_VIN	Power supply voltage with respect to VSS	3.0	3.6	4.8	V
$T_{STORAGE}$	Storage Temperature	-55	--	+125	°C

1. TBD = to be determined

7.2 Recommended Operating Conditions

Table 31: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
VDD12	1.2V digital power supply	--	1.14	1.2	1.32	V
VIO	1.8V/2.6V/3.3V digital power supply	--	1.62	1.8	1.98	V
		--	2.5	2.6	2.7	V
		--	2.97	3.3	3.63	V
VDD33	3.0V digital power supply	--	2.7	3.0	3.15	V
	3.3V digital power supply	--	2.97	3.3	3.63	V
AVDD18	1.8V analog power supply	--	1.71	1.8	1.89	V
AVDD18	1.8V analog power supply	--	1.71	1.8	1.89	V
AVDD33	3.3V analog power supply	--	2.97	3.3	3.63	V
AVDD33_USB	3.3V USB 2.0 power supply	--	2.97	3.3	3.63	V
LVLDO_VIN	1.8V LV LDO input voltage supply	--	1.62	1.8	1.98	V
VBLDO_VIN	3.3V VBAT LDO input voltage supply	--	3.0	3.3	4.8	V
VBLDO33_VIN	3.6V VBAT LDO33 input voltage supply	--	3.3	3.6	4.8	V
T_A	Ambient operating temperature	Commercial	0	--	70	°C
T_J	Maximum junction temperature	--	--	--	125	°C

7.2.1 Internal Operating Frequencies

Table 32: Internal Operating Frequencies[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{SYSCLK}	CPU clock speed	--	--	--	128	MHz
	System clock speed	--	--	--	128	MHz
	Encryption clock speed	--	--	--	128	MHz

1. Table 32 refers to the internal system and CPU clock. For information on the allowable reference clock frequencies, see Section 7.6, Clock Specifications, on page 98.

7.3 Digital Pad Ratings—VIO

7.3.1 1.8V Operation

7.3.1.1 General

Table 33: DC Electricals—1.8V Operation (VIO)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	0.7*V18	--	V18+0.3	V
V_{IL}	Input low voltage	--	-0.3	--	0.3*V18	V
V_{HYS}	Input hysteresis	--	150	--	--	mV
V_{OH}	Output high voltage	--	V18-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

7.3.1.2 Host Interface

Table 34: DC Electricals—Host Interface, 1.8V Operation (VIO)[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	0.7*V18	--	V18+0.3	V
V_{IL}	Input low voltage	--	-0.3	--	0.3*V18	V
V_{HYS}	Input hysteresis	--	200	--	--	mV
V_{OH}	Output high voltage	--	V18-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

1. Applicable to SDIO host interface pads.

7.3.2 2.6V Operation

7.3.2.1 General

Table 35: DC Electricals—2.6V Operation (VIO)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	0.7*V26	--	V26+0.3	V
V_{IL}	Input low voltage	--	-0.3	--	0.3*V26	V
V_{HYS}	Input hysteresis	--	200	--	--	mV
V_{OH}	Output high voltage	--	V26-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

7.3.2.2 Host Interface

Table 36: DC Electricals—Host Interface, 2.6V Operation (VIO)[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	0.7*V26	--	V26+0.3	V
V_{IL}	Input low voltage	--	-0.3	--	0.3*V26	V
V_{HYS}	Input hysteresis	--	200	--	--	mV
V_{OH}	Output high voltage	--	V26-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

1. Applicable to SDIO host interface pads.

7.3.3 3.3V Operation

7.3.3.1 General

Table 37: DC Electricals—3.3V Operation (VIO)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	0.7*V33	--	V33+0.3	V
V_{IL}	Input low voltage	--	-0.3	--	0.3*V33	V
V_{HYS}	Input hysteresis	--	200	--	--	mV
V_{OH}	Output high voltage	--	V33-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

7.3.3.2 Host Interface

Table 38: DC Electricals—Host Interface, 3.3V Operation (VIO)[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	0.7*V33	--	V33+0.3	V
V_{IL}	Input low voltage	--	-0.3	--	0.3*V33	V
V_{HYS}	Input hysteresis	--	200	--	--	mV
V_{OH}	Output high voltage	--	V33-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

1. Applicable to SDIO host interface pads.

7.4 Digital Pad Ratings—VDD33

7.4.1 3.0V Operation

Table 39: DC Electricals—3.0V Operation (VDD33)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	0.7*NBIAS	--	V30+0.3	V
V_{IL}	Input low voltage	--	-0.3	--	0.3*NBIAS	V
V_{HYS}	Input hysteresis	--	250	--	--	mV
V_{OH}	Output high voltage	--	V30-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

7.4.2 3.3V Operation

Table 40: DC Electricals—3.3V Operation (VDD33)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	0.7*NBIAS	--	V33+0.3	V
V_{IL}	Input low voltage	--	-0.3	--	0.3*NBIAS	V
V_{HYS}	Input hysteresis	--	250	--	--	mV
V_{OH}	Output high voltage	--	V33-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

7.5 Package Thermal Conditions

Table 41: Thermal Conditions—68-Pin QFN

Symbol	Parameter	Condition	Typ	Units
θ_{JA}	Thermal resistance[1] Junction to ambient of package. $\theta_{JA} = (T_J - T_A)/ P$ P = total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	22.7	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 1 meter/sec air flow	20.2	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 2 meter/sec air flow	19.2	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 3 meter/sec air flow	18.6	°C/W
ψ_{JT}	Thermal characteristic parameter[1] Junction to top center of package. $\psi_{JT} = (T_J - T_{TOP})/P$ T_{TOP} = temperature on top center of package	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	0.21	°C/W
ψ_{JB}	Thermal characteristic parameter[1] Junction to top center of package. $\psi_{JT} = (T_J - T_B)/P$ T_B = power dissipation from top center of package	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	8.99	°C/W
θ_{JC}	Thermal resistance[1] Junction to case of the package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = power dissipation from top of package	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	8.5	°C/W
θ_{JB}	Thermal resistance[1] Junction to board of package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from bottom of package to PCB surface	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	9.2	°C/W

1. Refer to white paper on AN-63 Thermal Calculations for more information.

7.6 Clock Specifications

7.6.1 Single-Ended Clock Input Modes

7.6.1.1 2.4 GHz Mode

Table 42: CMOS Mode[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	AVDD18 - 0.5	AVDD18	AVDD18 + 0.2	V
V_{IL}	Input low voltage	--	0	0	0.4	V

1. Typical input capacitance is approximately 2 pF and input resistance is >20 kΩ.

Table 43: Low-Swing Mode[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
VLS_IH	Single-ended high-level voltage	--	--	--	1.8	V
VLS_IL	Single-ended low-level voltage	--	0	--	--	V
VLS_Amp	Low-swing clock amplitude (pk-pk)	--	0.5	--	--	V
VLS_Slope	Low-swing mid-point slope	--	50	--	--	MV/s
Duty	Duty cycle	--	45	50	55	%

1. AC-coupling capacitor is integrated into the SoC.

Table 44: Phase Noise—2.4 GHz Operation

Parameter	Test Conditions	Min	Typ	Max	Units
Fref = 26 MHz	Offset = 1 kHz	--	--	-126	dBc/Hz
	Offset = 10 kHz	--	--	-137	dBc/Hz
	Offset = 100 kHz	--	--	-143	dBc/Hz
	Offset > 1 MHz	--	--	-143	dBc/Hz
Fref = 38.4 MHz	Offset = 1 kHz	--	--	-123	dBc/Hz
	Offset = 10 kHz	--	--	-134	dBc/Hz
	Offset = 100 kHz	--	--	-140	dBc/Hz
	Offset > 1 MHz	--	--	-140	dBc/Hz
Fref = 40 MHz	Offset = 1 kHz	--	--	-123	dBc/Hz
	Offset = 10 kHz	--	--	-134	dBc/Hz
	Offset = 100 kHz	--	--	-140	dBc/Hz
	Offset > 1 MHz	--	--	-140	dBc/Hz
Fref = 44 MHz	Offset = 1 kHz	--	--	-122	dBc/Hz
	Offset = 10 kHz	--	--	-133	dBc/Hz
	Offset = 100 kHz	--	--	-139	dBc/Hz
	Offset > 1 MHz	--	--	-139	dBc/Hz

7.6.1.2 Dual-Band (2.4 and 5 GHz) Mode

Table 45: Phase Noise—Dual-Band Operation

Parameter	Test Conditions	Min	Typ	Max	Units
Fref = 26 MHz	Offset = 1 kHz	--	--	-130	dBc/Hz
	Offset = 10 kHz	--	--	-150	dBc/Hz
	Offset = 100 kHz	--	--	-156	dBc/Hz
	Offset > 1 MHz	--	--	-156	dBc/Hz
Fref = 38.4 MHz	Offset = 1 kHz	--	--	-126	dBc/Hz
	Offset = 10 kHz	--	--	-146	dBc/Hz
	Offset = 100 kHz	--	--	-152	dBc/Hz
	Offset > 1 MHz	--	--	-152	dBc/Hz
Fref = 40 MHz	Offset = 1 kHz	--	--	-126	dBc/Hz
	Offset = 10 kHz	--	--	-146	dBc/Hz
	Offset = 100 kHz	--	--	-152	dBc/Hz
	Offset > 1 MHz	--	--	-152	dBc/Hz
Fref = 44 MHz	Offset = 1 kHz	--	--	-125	dBc/Hz
	Offset = 10 kHz	--	--	-145	dBc/Hz
	Offset = 100 kHz	--	--	-151	dBc/Hz
	Offset > 1 MHz	--	--	-151	dBc/Hz

7.6.2 Crystal

Table 46: Crystal Specifications

Parameter	Condition	Typical	Units
Fundamental Frequencies	--	26, 38.4, 40, 44	MHz
Frequency Tolerance	Over operating temperature	< ±10	ppm
	Over process at 25ºC	< ±10	ppm
SMD and AT Cut Height	--	<1.2	mm
Load Capacitor	Across	10	pF
Maximum Series Resistance	--	60	ohm
Resonance Mode	--	A1, Fundamental	--

7.6.3 Sleep Clock

Table 47: External Sleep Clock Timing
NOTE: Limited to within 10 °C variance.

Symbol	Parameter	Min	Typ	Max	Units
CLK	Clock frequency range/accuracy • CMOS input clock signal type • ±250 ppm (initial, aging, temperature)	--	32.768	--	kHz
V_{IH}	Input levels	0.8	--	1.98	V
V_{IL}		0.0	--	0.25	V
PN	Phase noise requirement (@ 100 KHz)	--	-125	--	dBc/Hz
Jc	Cycle Jitter	--	1.5	--	ns (RMS)
SR	Slew rate limit (10-90%)	--	--	100	ns
DC	Duty cycle tolerance	20	--	80	%

7.7 Coexistence Specifications

The 88W8782 coexistence pins are powered from the VIO voltage supply.

See Section 7.3, Digital Pad Ratings—VIO, on page 93 for DC specifications.

7.7.1 Marvell 3/4-Wire

Figure 37: Marvell 3/4-Wire Timing Diagram

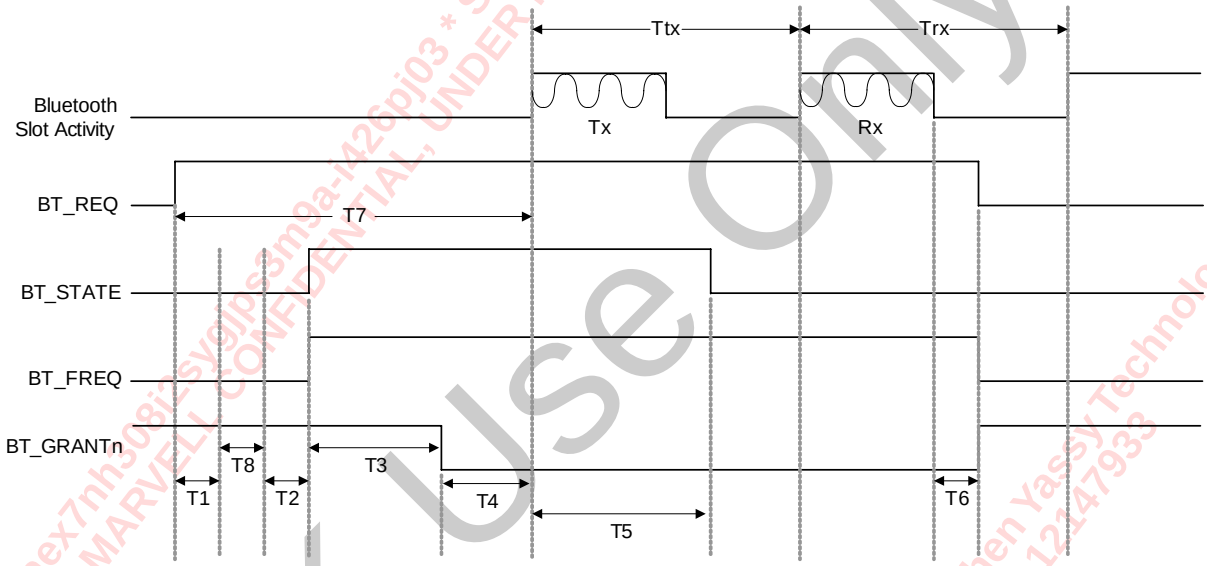


Table 48: Marvell 3/4-Wire Timing Data

Symbol	Parameter	Min	Typ	Max	Units
T1	Priority[0] info is valid in BT_STATE on and after T1 from BT_REQ rise.	0	1	100	µs
T2	TxRx Info is valid in BT_STATE on and after T2. The BT_STATE must hold until there is any change of direction in the next slots.	2	19	100	µs
T3	Time from TxRx Info valid to BCA grant decision. T3 = T7 - T4 - T2 - T8 - T1	2	40	594	µs
T4	BT_GRANTn needs to be valid T4 time before the upcoming slot. BT_GRANTn indicates Tx grant, and may also indicate Rx grant*. Once a slot is granted, the subsequent slots are also granted unless there is a change in direction from Rx to Tx. Rx to Tx change always re-arbitrates.	2	80	594	µs
T5	TxRx Info for the next slot is valid on and after T5 to the start of the next slot. If direction remains the same for the next slot, then BT_STATE must not change during the current slot. If the direction changes for the next slot, then BT_STATE must change only after the last bit of Bluetooth data is transferred; otherwise the transfer may be disrupted.	50	40	600	µs
T6	The BT_REQ signal de-asserts T6 time after last bit of Bluetooth data is transferred.	0	15	25	µs
T7	Time from BT_REQ rise to first Bluetooth slot boundary. Bluetooth slot boundary is marked by the first bit of Bluetooth data.	8	150	600	µs
T8	Optional Priority[1] information is valid in BT_STATE on and after T8. This time parameter only exists if BCA is configured for 2-bit priority on same BT_STATE pin. Otherwise, the start of T2 would come after T1.	2	10	100	µs
Ttx	Slot time (fixed for Bluetooth)	--	625	--	µs
Trx	Slot time (fixed for Bluetooth)	--	625	--	µs

7.7.2 WL_ACTIVE 2/3/4-Wire

Figure 38: WL_ACTIVE 2/3/4-Wire Timing Diagram

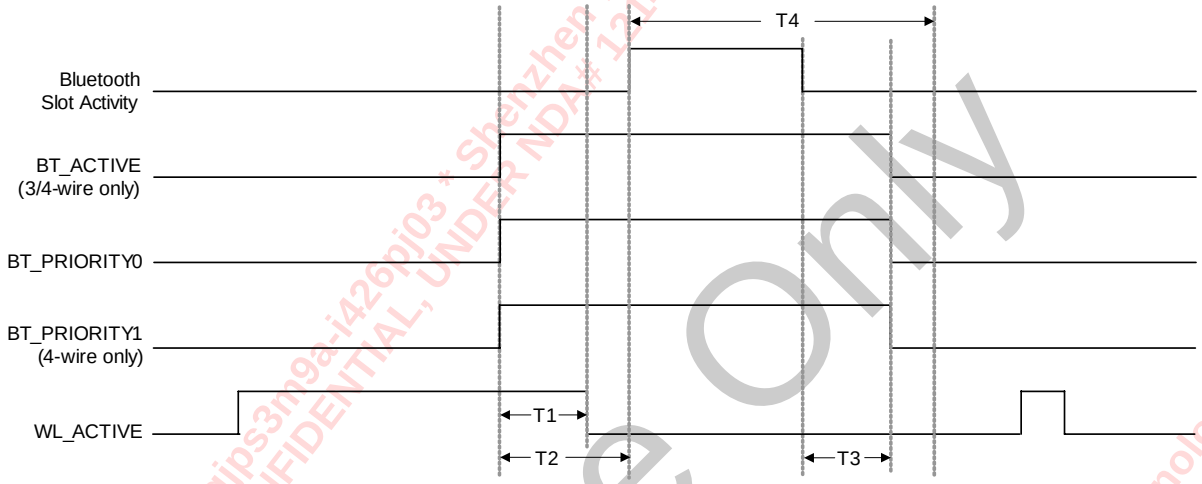


Table 49: WL_ACTIVE 2/3/4-Wire Timing Data

Symbol	Parameter	Min	Typ	Max	Units
T1	• If WLAN can be stopped[1], WL_ACTIVE will de-assert prior to Bluetooth slot start (T1 < T2). • If the Bluetooth device samples WL_ACTIVE before starting priority transfer[1], WL_ACTIVE needs to de-assert earlier than the sampling time.	0	--	499	µs
T2	Time from BT_PRIORITY rise to start of Bluetooth activity.	20	50	499	µs
T3	Time from end of Bluetooth activity to BT_PRIORITY fall.	0	0	499	µs
T4	Slot time (fixed for Bluetooth)	--	625	--	µs

1. Supported by Marvell device.

7.8 Host Interface Specifications

7.8.1 SDIO

The 88W8782 SDIO host interface pins are powered from the VIO voltage supply.

See Section 7.3, Digital Pad Ratings—VIO, on page 93 for DC specifications.

The SDIO electrical specifications are identical for the 1-bit SDIO, 4-bit SDIO modes.

Figure 39: SDIO Protocol Timing Diagram—Normal Mode

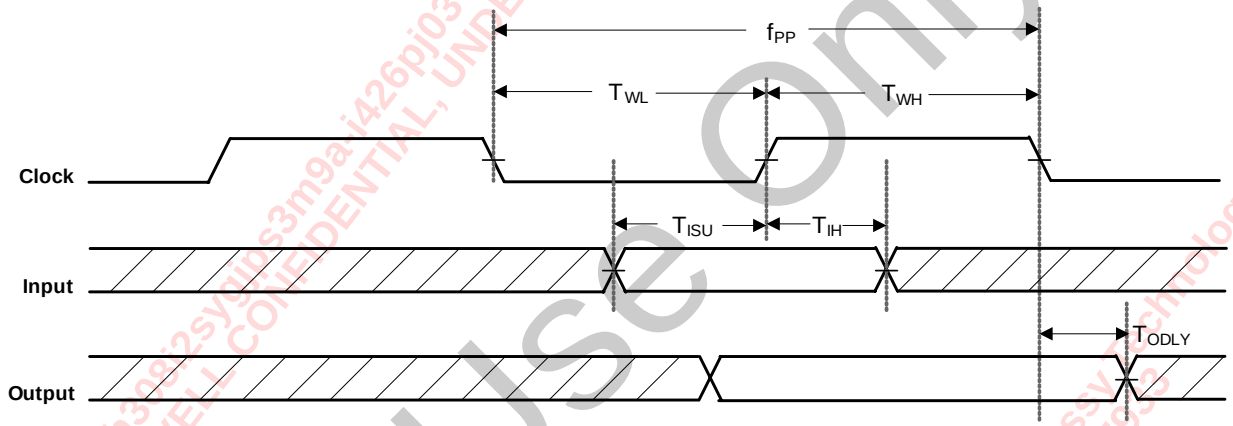


Figure 40: SDIO Protocol Timing Diagram—High Speed Mode

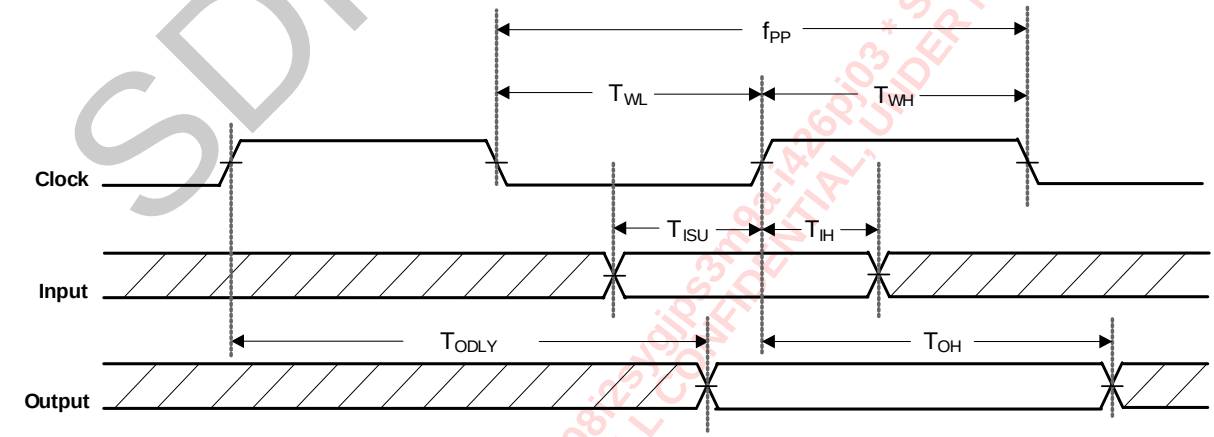


Table 50: SDIO Timing Data[1]

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WL}	Clock Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{WH}	Clock High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time	--	--	--	7.33	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

1. The SDIO-SPI CS signal timing is identical to all other SDIO inputs.

7.9 Peripheral Bus Interface Specifications

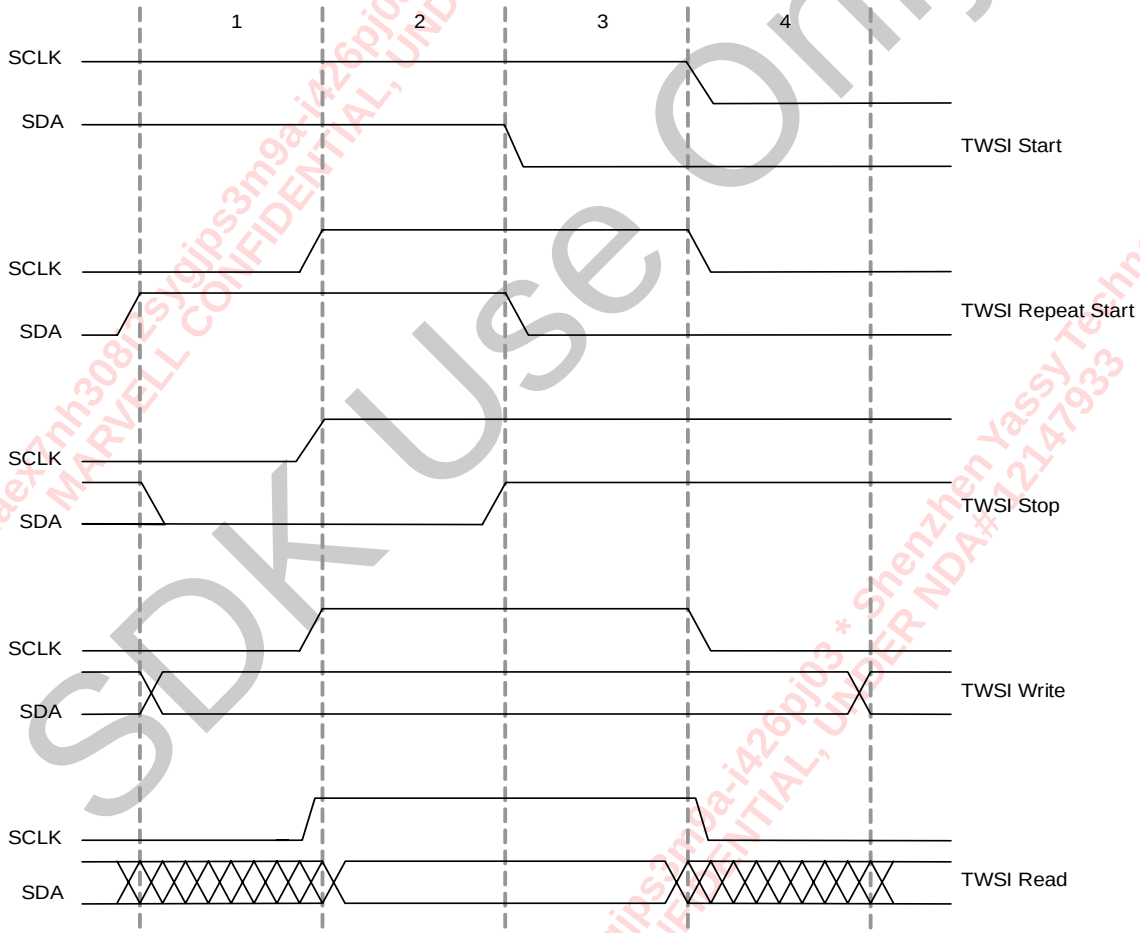
7.9.1 Clocked Serial Unit

The 88W8782 clocked serial pins are powered from the VIO voltage supply.

See Section 7.3, Digital Pad Ratings—VIO, on page 93 for DC specifications.

7.9.1.1 TWSI

Figure 41: TWSI Signaling



7.9.1.2 SPI EEPROM Serial Interface

Figure 42: SPI EEPROM Serial Interface Timing Diagram

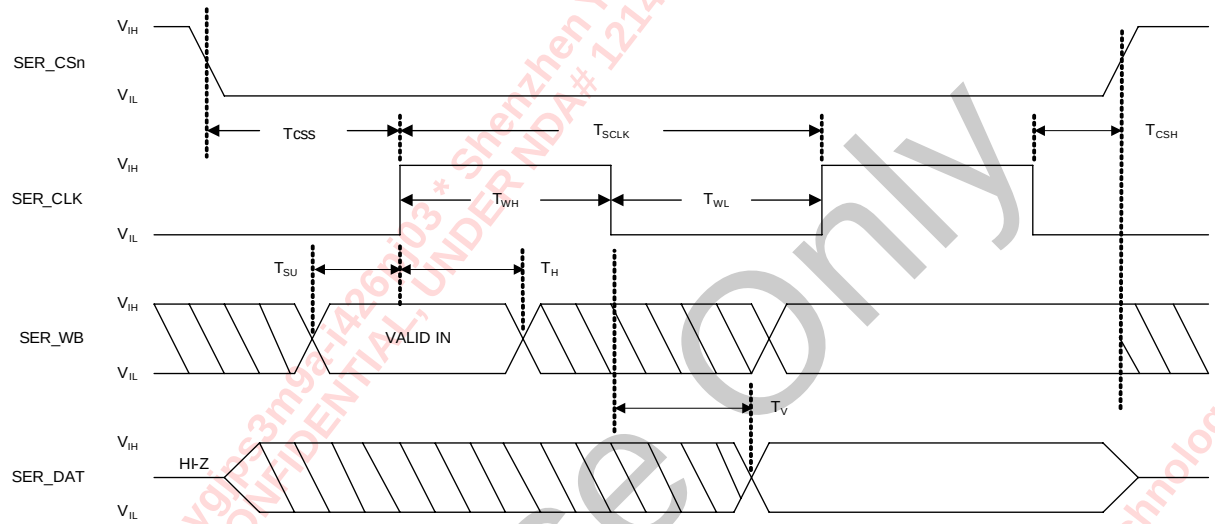


Table 51: SPI EEPROM Serial Interface Timing Data[1]

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CSS}	Chip select setup time	--	--	1/(2*SCLK)	--	ns
T_{CSH}	Chip select hold time	--	--	1/(2*SCLK)	--	ns
T_{SCLK}	SCLK period[2]	--	$2/f_{SYSCLK}$	--	$2^{17}/f_{SYSCLK}$	ns
T_{WH}	SCLK width high	--	$1/f_{SYSCLK}$	--	$2^{16}/f_{SYSCLK}$	ns
T_{WL}	SCLK width low	--	$1/f_{SYSCLK}$	--	$2^{16}/f_{SYSCLK}$	ns
T_{SU}	Setup time (SRWB to SCLK)	--	15	--	--	ns
T_{H}	Hold time (SRWB from SCLK)	--	0	--	--	ns
T_{V}	SDA output delay (from SCLK)	--	--	--	80	ns

1. f_{SYSCLK} = system clock frequency (see Table 32, Internal Operating Frequencies, on page 92).
2. Internal pullup only. No external pullup. Maximum serial clock frequency limited to 16 MHz (for transceiver).

7.9.2 UART

The 88W8782 UART Tx and Rx pins are powered from the VIO voltage supply.

See Section 7.3, Digital Pad Ratings—VIO, on page 93 for DC specifications.

7.9.3 GPIO

The 88W8782 GPIO pins are powered from the VIO voltage supply.

See Section 7.3, Digital Pad Ratings—VIO, on page 93 for DC specifications.

7.9.3.1 LED Mode

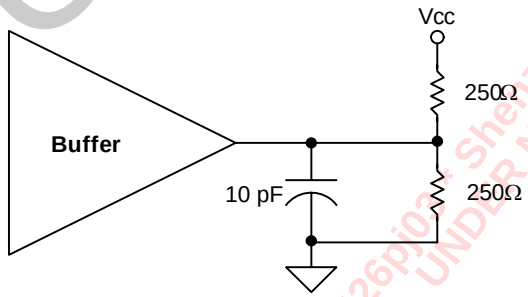
Table 52: LED Mode[1]

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Typ	Units
I_{OH}	Switching current high	Tristate on pad (requires pull-up on board)	Tristate when driving high	mA
I_{OL}	Switching current low	@ 0.4V	10	mA

1. LED Mode is independently selectable for the GPIO[1].

Figure 43: Slew Rate Measurement



7.10 Test Interface Specifications

The 88W8782 test interface pins are powered from the VIO voltage supply.

See Section 7.3, Digital Pad Ratings—VIO, on page 93 for DC specifications.

Figure 44: JTAG Timing Diagram

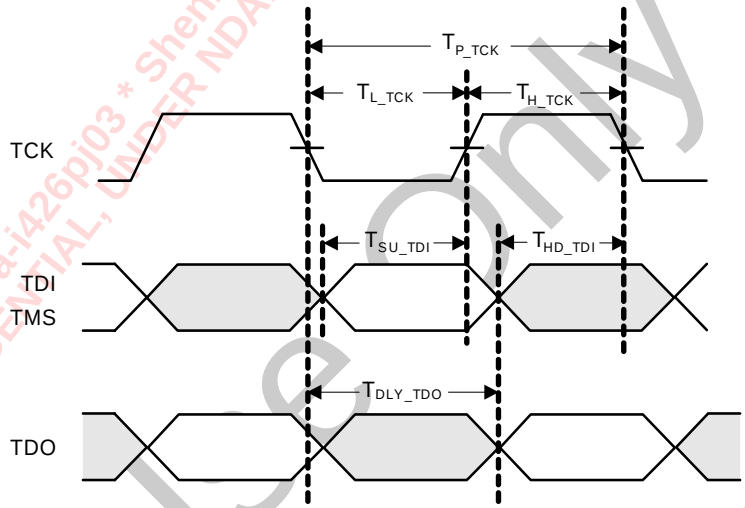


Table 53: JTAG Timing Data[1]

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period	--	40	--	--	ns
T_{H_TCK}	TCK High	--	12	--	--	ns
T_{L_TCK}	TCK Low	--	12	--	--	ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time	--	10	--	--	ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time	--	10	--	--	ns
T_{DLY_TDO}	TCK to TDO Delay	--	0	--	15	ns

1. Does not apply to CPU JTAG enabled by the TMS_CPU pin.

8 Part Order Numbering/Package Marking

8.1 Part Order Numbering

Figure 45 shows the part order numbering scheme. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 45: Sample Part Number

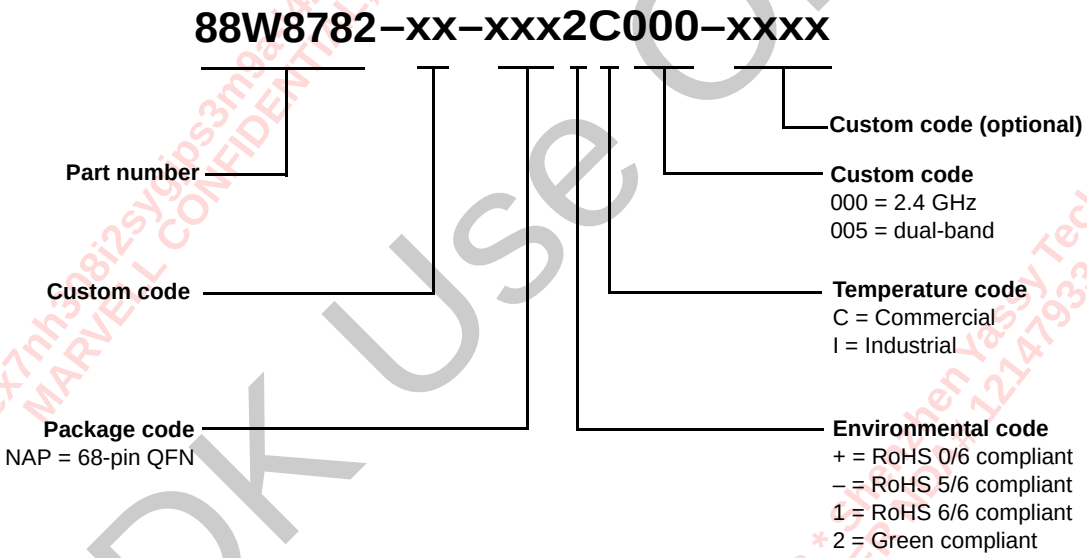


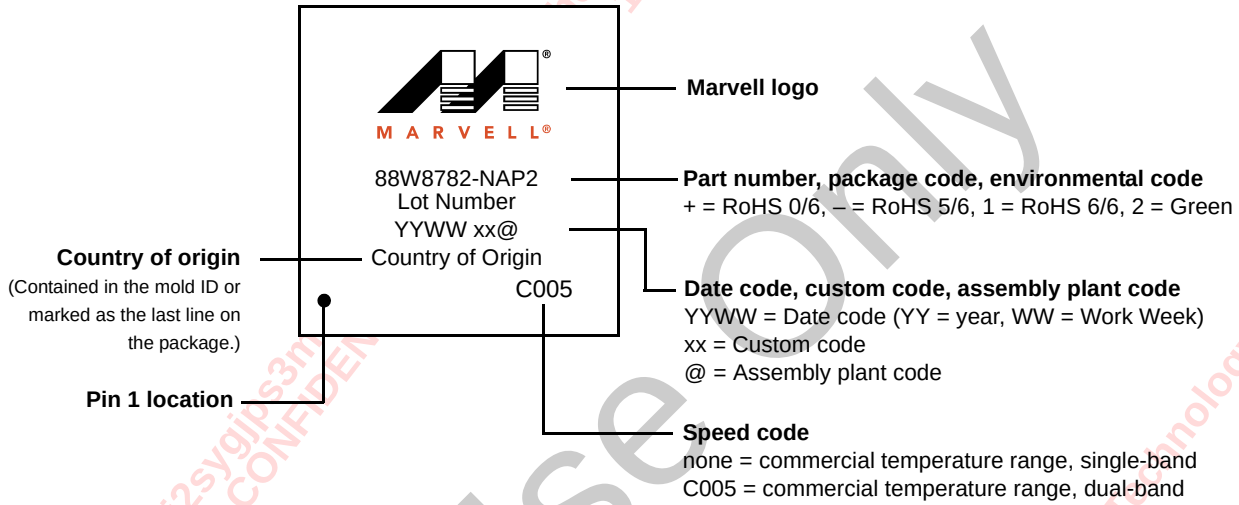
Table 54: Part Order Options

Package Type	Part Order Number
68-pin QFN (Tape-and-Reel)	88W8782-xx-NAP2C000-P123 (2.4 GHz band)
68-pin QFN (Tape-and-Reel)	88W8782-xx-NAP2C005-P123 (dual-band)

8.2 Package Marking

Figure 46 shows a sample package marking and pin 1 location for the device.

Figure 46: Commercial Package Marking and Pin 1 Location—QFN Package Option



Note: Above drawing is not drawn to scale. Location of markings is approximate.

A Acronyms and Abbreviations

Table 55: Acronyms and Abbreviations

Acronym	Definition
ABR	Automatic Baud Rate
ACK	Acknowledgement
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AFC	Automatic Frequency Correction
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
AIFS	Arbitration Interframe Space
AP	Access Point
APB	Advanced Peripheral Bus
API	Application Program Interface
ARM	Advanced RISC Machine
ATIM	Announcement Traffic Indication Message
BAMR	Base Address Mask Register
BAR	Base Address Register
BBU	Baseband Processor Unit
BCB	Benzocyclobutene (flip chip bump process)
BLE	Bluetooth Low Energy
BOM	Bill of Materials
BSS	Basic Service Set
BSSID	Basic Service Set ID
BTU	Bluetooth Baseband Unit
BRF	Bluetooth RF Unit
BWQ	Bandwidth Queue
CBC	Cipher-Block Chaining
CBP	Contention-Based Period
CCA	Clear Channel Assessment
CCK	Complementary Code Keying
CCMP	Counter Mode CBC-MAC Protocol
CDE	Close Descriptor Enable

Table 55: Acronyms and Abbreviations (Continued)

Acronym	Definition
CFP	Contention-Free Period
CFQ	Contention-Free Queue
CID	Connection Identifier
CIS	Card Information Structure
CIU	CPU Interface Unit
CMD	Command
CMQ	Control Management Queue
CRC	Cyclic Redundancy Check
CS	Card Select
CSMA/CA	Carrier Sense Multiple Access / Collision Avoidance
CSMA/CD	Carrier Sense Multiple Access / Collision Detection (802.3 MAC)
CSU	Clocked Serial Unit
CTS	Clear to Send
DAC	Digital to Analog Converter
DBPSK	Differential Binary Phase Shift Keying
DCD	Device Controller Driver
DCE	Data Communication Equipment
DCF	Distributed Coordination Function
DCLA	Direct Current Level Adjustment
DCU	DMA Controller Unit
DFS	Dynamic Frequency Selection
DIFS	Distributed Interframe Space
DMA	Direct Memory Access
dQH	Device Queue Head
DQPSK	Differential Quadrature Phase Shift Keying
DSM	Distribution System Medium
DSP	Digital Signal Processor
dTD	Linked List Transfer Descriptors
DTIM	Delivery Traffic Indication Map
EAP	Extensible Authentication Protocol
ED	Energy Detect
EDCA	Enhanced Distributed Channel Access
EEPROM	Electrically Erasable Programmable Read Only Memory
EIFS	Extended Interframe Space
ERP-OFDM	Extended Rate PHY-Orthogonal Frequency Division Multiplexing
FAE	Field Application Engineer
FIFO	First In First Out

Table 55: Acronyms and Abbreviations (Continued)

Acronym	Definition
FIPS	Federal Information Processing Standards
FIQ	Fast Interrupt Request
FM	Frequency Modulation
FMU	Frequency Modulation Unit
FMR	Frequency Modulation Decoder/RF
FW	Firmware
GI	Guard Interval
GPIO	General Purpose Input Output
GPL	GNU General Public License
GPU	General Purpose Input Output Unit
HIU	Host Interface Unit
HSIC	High Speed Inter-Chip
HT	High Throughput
HW	Hardware
I/Q	Inphase/Quadrature
IB	InBand
IBSS	Independent Basic Service Set
ICE	In-Circuit Emulator (or Emulation)
ICR	Interrupt Cause Register
ICU	Interrupt Controller Unit
ICV	Integrity Check Value
IE	Information Element
IEEE	Institute of Electrical and Electronics Engineers
IEMR	Interrupt Event Mask Register
IF	Interface
IFS	Interframe Space
IMR	Interrupt Mask Register
IPG	Inter Packet Gap
IPsec	Internet Protocol Security
IR	Infrared
IRQ	Interrupt Request
ISA	Instruction Set Architecture
ISDN	Integrated Services Digital Network
ISM	Industrial Scientific and Medical
ISMR	Interrupt Status Mask Register
ISR	Interrupt Status Register
JEDEC	Joint Electronic Device Engineering Council

Table 55: Acronyms and Abbreviations (Continued)

Acronym	Definition
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LME	Layer Management Entity
LNA	Low Noise Amplifier
LQFN	Low Quad Flat Non-leaded
LSB	Least Significant Bit
LSP	Low Speed Peripheral
MAC	Media/Medium Access Controller
MC	Memory Controller
MCS	Modulation Coding Scheme
MCU	WLAN MAC Control Unit
MDI	Modem Data Interface
MIB	Management Information Base
MIC	Message Integrity Code
MII	Media Independent Interface
MIMO	Multiple Input Multiple Output
MIPS	Million Instructions Per Second
MLME	MAC Sublayer Management Entity
MMI	Modem Management Interface
MMPDU	MAC Management Protocol Data Unit
MMU	Memory Management Unit
MPDU	MAC Protocol Data Unit
MSB	Most Significant Bit
MSDU	MAC Service Data Unit
Multi-ICE	JTAG emulator for ARM-based SoC devices
NAV	Network Allocation Vector
NDP	Null Data Packet
NL	No load
NPTR	Next Descriptor Pointer
OFDM	Orthogonal Frequency Division Multiplexing
OID	Object Identifier
OOB	OutofBand
PA	Power Amplifier
PAD	Packet Assembler/Disassembler
PBU	Peripheral Bus Unit
PC	Point Coordinator
PCB	Printed Circuit Board

Table 55: Acronyms and Abbreviations (Continued)

Acronym	Definition
PCF	Point Coordination Function
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PEAP	Protected EAP
PHY	Physical Layer
PIFS	Priority Interframe Space
PLL	Phase-Locked Loop
PLME	Physical Layer Management Entity
PMU	Power Management Unit
POST	Power On Self Test
PPK	Per-Packet Key
PPM	Pulse Position Modulation
PSK	Pre-Shared Keys
PTA	Packet Traffic Arbitration
PWK	Pair Wise Key
QAM	Quadrature Amplitude Modulation
QFN	Quad Flat Non Leaded Package
QoS	Quality of Service
RA	Receiver Address
RBDS	Radio Broadcast Data System
RDS	Radio Data System
RF	Radio Frequency
RIFS	Reduced Interframe Space
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
RSSI	Receiver Signal Strength Indicator
RTS	Request To Send
RTU	General Purpose Timer Unit
SA	Source Address
SAP	Service Access Point
SCLK	Serial Interface Clock
SDA	Serial Interface Data
SFD	Start of Frame Delimiter
SIFS	Short Interframe Space
SIU	Serial Interface Unit (UART)

Table 55: Acronyms and Abbreviations (Continued)

Acronym	Definition
SJU	System/Software JTAG Controller Unit
SM	Switch Module
SMI	Serial Management Interface
SNR	Signal To Noise Ratio
SO	Serial Out
SoC	System-on-Chip
SPI	Serial Peripheral Interface
SQU	Internal SRAM Unit
SRWB	Serial Interface Read Write
SSID	Service Set Identifier
STBC	Space-Time Block Coding
TA	Transmitter Address
TBG	Time Base Generator
TBTT	Target Beacon Transmission Time
TCM	Tightly Coupled Memory
TCP/IP	Transmission Control Protocol/Internet Protocol
TCQ	Traffic Category Queue
TDM	Time Division Multiplexing
TDU	Time Division Multiplexing Unit
TIM	Traffic Indication Map
TKIP	Temporal Key Integrity Protocol
TPC	Transmit Power Control
TQFP	Thin Quad Flat Pack
TRPC	Transmit Rate-based Power Control
TSC	TKIP Sequence Counter
TSF	Timing Synchronization Function
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UBM	Under Bump Metal
VCO	Voltage Controlled Oscillator
WAP	Wireless Application Protocol
WEP	Wired Equivalent Privacy
Wi-Fi	Wireless Fidelity (IEEE 802.11)
WLAN	Wireless Local Area Network
WMM	Wi-Fi Multimedia
WPA	Wi-Fi Protected Access
WPA2	Wi-Fi Protected Access 2

Table 55: Acronyms and Abbreviations (Continued)

Acronym	Definition
WPA2-PSK	Wi-Fi Protected Access 2-Pre-shared Keys
WPA-PSK	Wi-Fi Protect Access-Pre-shared Keys
WSE	Wireless Interconnection System Engine
XFQFN	Extra-Fine Quad Flat Non-leaded
XOSC	Crystal Oscillator

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B Revision History

Table 56: Revision History

Document Type	Document Revision
Released	Rev. C
Package • Table 3, WLAN RF Front-End Control Interface, on page 21: added pin state data, referred to GPIO[5] for state and supply data • Table 4, Power Down Interface, on page 22: added pin state data • Table 5, Clock Interface, on page 22: added pin state data • Table 6, Host Interface, on page 23: added pin state data • Table 7, Multi-Purpose Interface, on page 24: added pin state data • Table 8, EEPROM/TWSI Interface, on page 25: added pin state data • Table 9, Bluetooth Coexistence Interface, on page 26: added pin state data • Table 10, JTAG Interface, on page 26: added pin state data	

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