**Analogue Music synthesiser**

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**Introduction**

Analogue music synthesiser is an influential device that changed rock music as well as helped to create electronic music. Unlike traditional musical instruments that could only produce specific sounds by their natures, synthesisers could produce any kind of music within human imagination by directly modifying the essential elements of sound, that is, the frequency that determines the tone; the waveshape and envelope that determine the timbre. This report explores the design and construction of an analog synthesizer.

In this ELEC40006 project, the aim was to create a well-functioning analogue audio synthesizer that could produce 7 tones of sounds within the C major octave. The type we were going to build was a subtractive, monophonic synthesizer since its basic principles, theory and plans were pretty mature, so that there could be lots of old, good designs to be referred to. Monophonic means the user could only press down one key at a time, rather than multiple keys. Hence every time only a sound with one of the 7 tones is produced. It was monophonic because that would only require one oscillator (which acts as the core in synthesizer design) rather than multiple ones, potentially reducing the cost and the LTspice final simulation time. Monophonic design still met the requirement although its functionally might be less than a polyphonic design, maybe in the future the final design could be upgraded to polyphonic which would just be a simple, repetitive process.

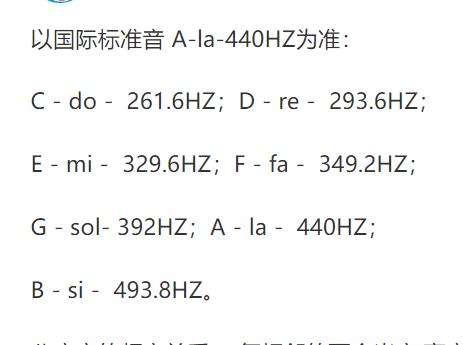


Figure 1. Scientific pitch notation (ref[1])

Our group: Jingyi Liang, Jingyi Wu and Zhaoyu Wu, decided to split the whole project into 4 parts: input stage (controller that simulates a keyboard, input voltage controlled oscillator), signal processing stage (voltage controlled filter), power amplifier stage( voltage controlled amplifier) and signal remodel stage (envelope generator), with Jingyi Wu focusing on the input, Zhaoyu Wu designing and building the filter stage and low frequency oscillator and Jingyi Liang working mostly on the amplifier and envelope generator. In the first few weeks we planned to spend most of our time interpreting the concepts, looking for resources online (usually on google and YouTube), and testing and fixing our modular design on separate schematics and had these component attached together in the final week, some modifications were made as well to ensure a desirable performance of the final synthesizer design. We communicate with each other, exchange ideas and schematics via WeChat app. Since we were all in China, we had up to 6 hours of co-working time every day. In this report, explanations the designing process of specific implementation of all of the modules will be described in detail.

**Design Overview**

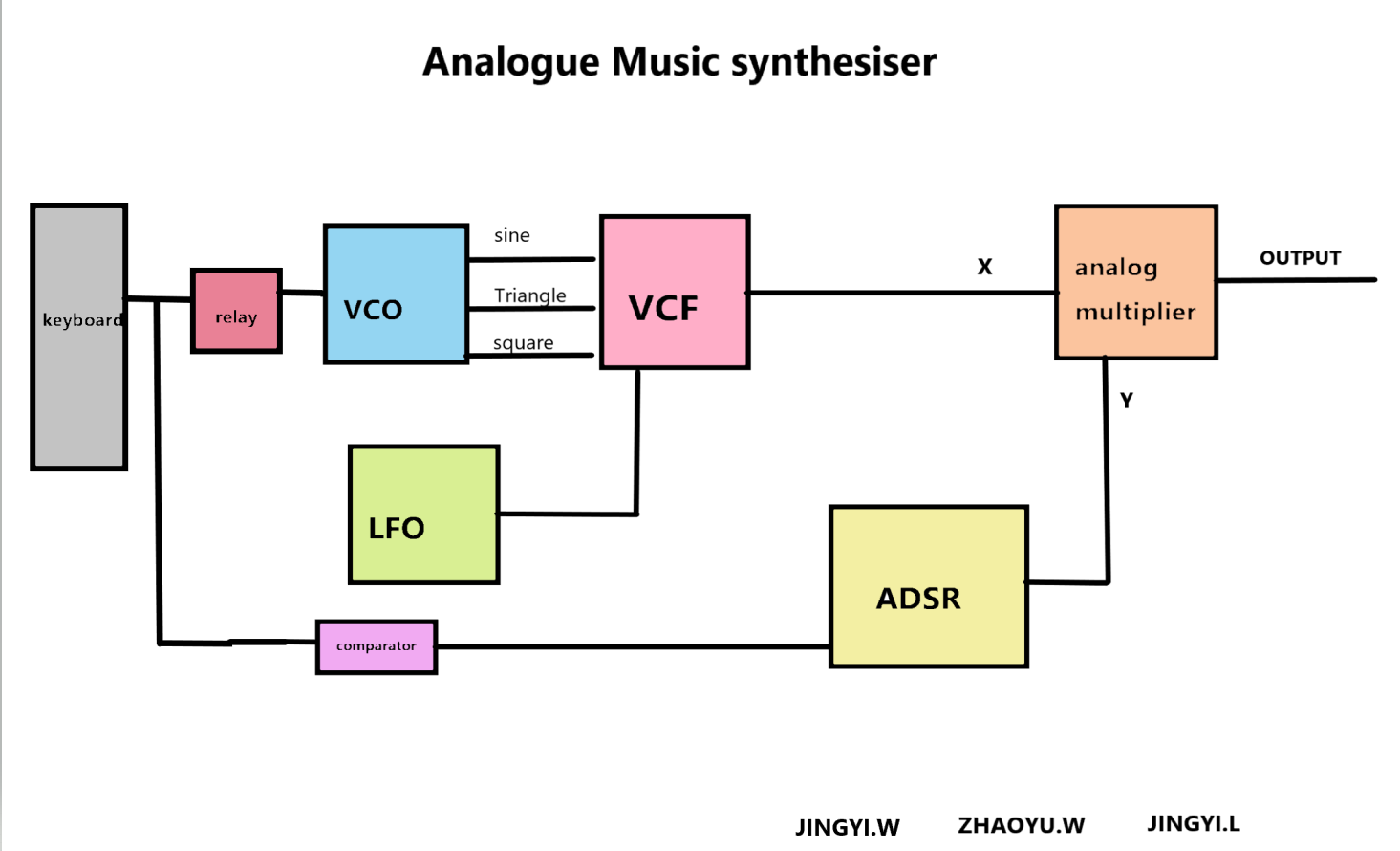


Figure 2. Overall block diagram of the whole synthesiser system

Figure 2 shows the overall design of the synthesiser system. As a modular synthesiser it had its each stage as a completely separate module and are processing the signal differently. In this block diagram each block represents a module and the lines represent the signals.

The dc voltage input is generated from the user interface of the synthesizer: the keyboard, with one voltage value corresponding to one key in reality. This keyboard then sends the signal to the voltage controlled oscillator (VCO), which produces several waveforms with frequencies that depend on the value of input signals. Theses waveforms are the basis of the sound signal that is going to be processed. Without it, no sound could be heard. Therefore the VCO is the core design in a synthesizer.

For this design, 3 types of waveforms are generated from VCO: square, triangle and sine, each outputted at a different node on the schematic. And selection of waveform will need to be done manually by the user by reconnecting the 3 outputs to the next stage: the voltage controlled filter (VCF).

The signal then propagates through VCF, which can act as either a low-pass, high-pass, or a band-pass filter depending on user set parameters. It filters the input at a frequency set by control knobs and input voltages. The purpose of this module is to remove some selection of harmonics to alter the timbre of the output waveform in order to lower the noise level.

The low frequency oscillator (LFO) is a more limited oscillator whose frequency is controlled manually and is designed to produce frequencies from around a kilohertz down to millihertz. This low frequency oscillation can be used as a control signals to create some intriguing effects and here it is used to sweep the frequency of VCF to create slowly changing tones or timbers.

The ADSR is an envelope generator that produces a time dependent output signal which is used to shape the signal outputted from VCF through an analog multiplier in order to transform the signal to a more realistic waveform. It is controlled by a gate signal that is outputted from a comparator, which compares the input voltage from user interface to the minimum voltage needed (which produces the lowest frequency pitch) so it only provides a constantly high dc voltage to turn the gate on and activate ADSR when input reaches the level we need.

The word 'ADSR' stands for 4 sections of the envelope: attack, decay, sustain and release, which is shown in Figure 3 below. Generally speaking, it simulates the physical behaviour of the key: at the moment the key is pressed, the voltage ramps up exponentially to a maximum value from zero and then decays down to a constant sustain level when the key is hold. After the key is released the voltage gradually decreases back to around zero.

For ADSR to work properly, a relay model is added between input stage and VCO to hold the input voltage so that after the key is let go there is still voltage in the circuit and the ‘release’ section would not decline to zero directly.

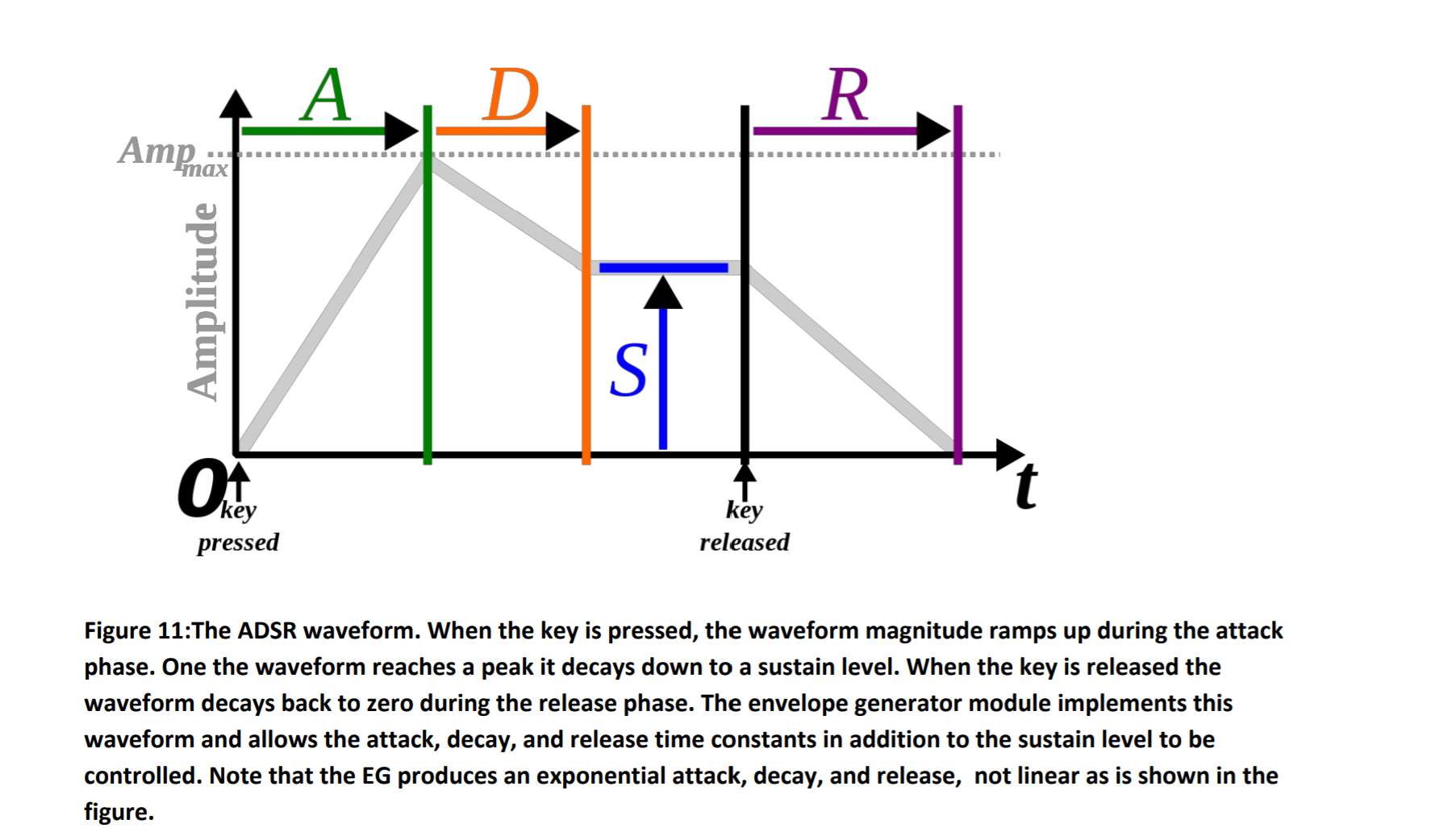


Figure 3. Process of ADSR

Finally, the analog multiplier simply multiplies the main signal and the ASDR signal together to remodel the main signal into the realistic shape.

To sum up:

-VCO: generated wave by turning a dc voltage into ac signal

-VCF: filters noise of different levels

-LFO: used as control input of filter to adjust its behaviour

-comparator: ensures input voltage reaches minimum requirement

-Envelope generator: shapes the signal into ADSR

-analog multiplier: mix the envelope signal with the main signal for more realistic sounds

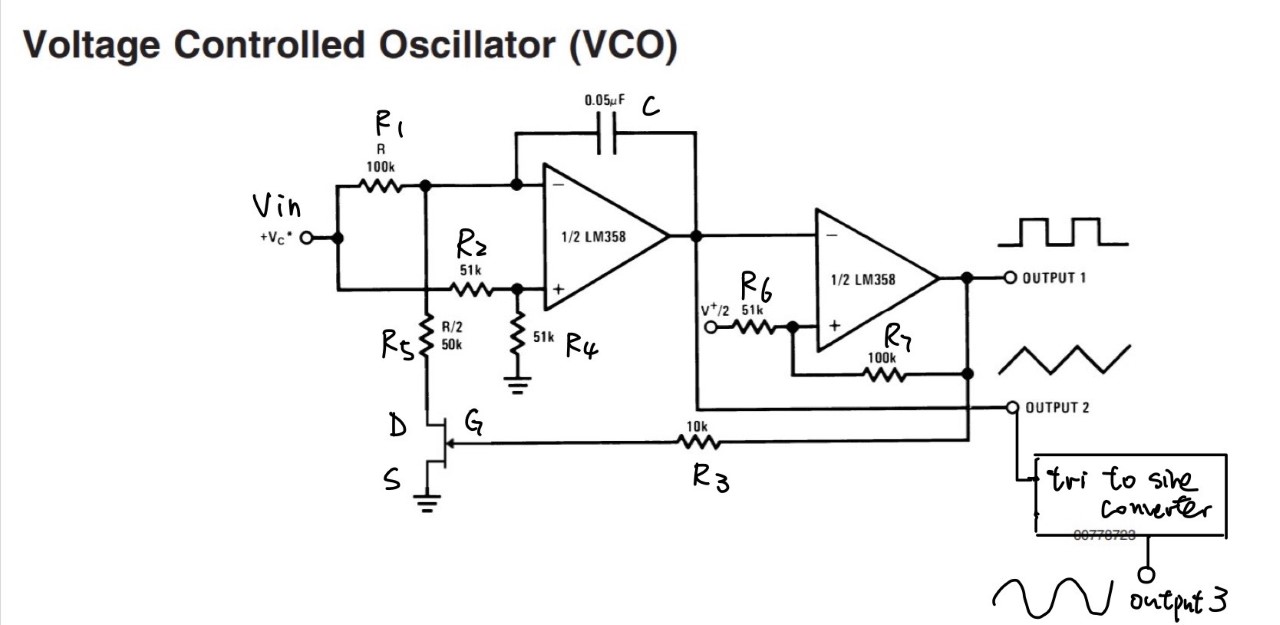
These five modules construct the basic system of an analogue audio synthesiser. Structure of some additional components that are included in the circuit (e.g potentiometer) and the detailed description as well as the testing process of each module will be explored later in this report.

**Voltage controlled oscillator(VCO) [By Jingyi Wu]**

As the starting point of the whole project, VCO has a role of taking in a dc voltage and converting that into several types of waveforms. In this section the detailed design process and working principles of VCO will be introduced.

1. **Design and working principle**

The schematic was inspired by the data sheet of LM358 which mentioned one of its applications as a VCO, as presented in Figure 1-1. A N-channel MOSFET was used instead of BJT as it works better as a switch and is a cheaper component.



**Figure 1-1. schematic of VCO with NMOS instead of BJT**

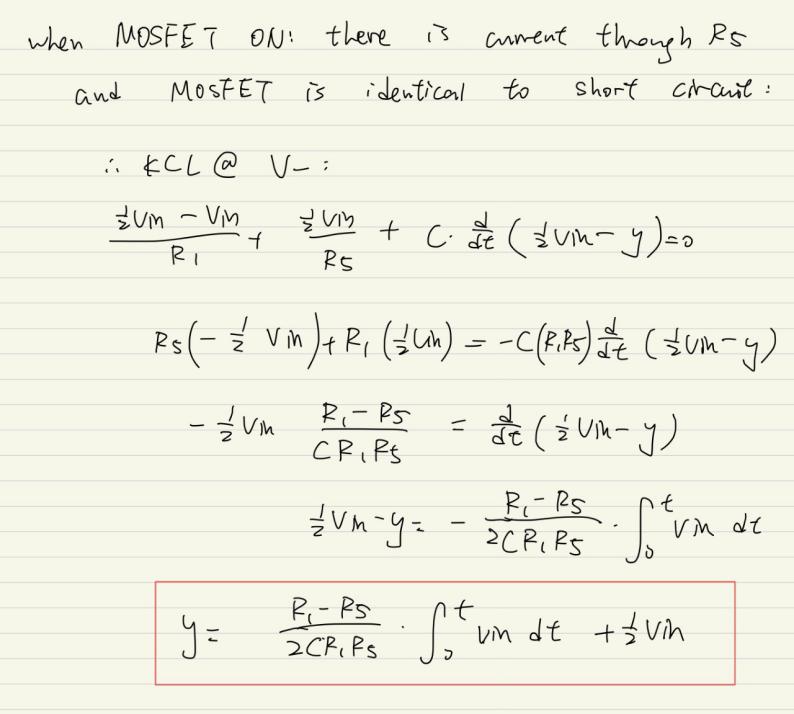
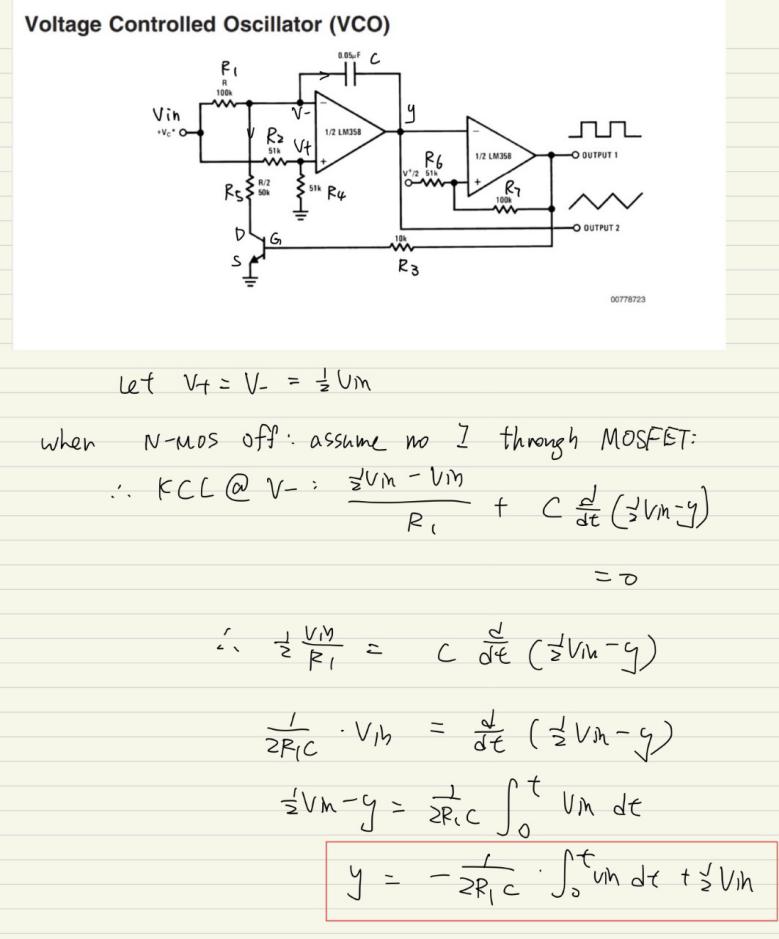
* Integrator working principles and equations

The VCO can be broken down into 3 subcircuits.

The first one is an integrator which integrates the input signal creating a linearly decreasing output whose slope depends on value of the input voltage. Due to the potential divider arrangement constituted by R2 and R4, half of the input voltage is applied to the non-inverting input of the first op-amp as a control voltage. This input determines what value the integrator should start integrating from.

The triangular waveform is created by changing state of the MOSFET. When the MOSFET is turned ON, the current from the resistor R1 flows through the MOSFET. The voltage which is now converted into current signal charges the capacitor C as there is no current into the op-amp. Therefore, to source this current, the first op-amp must provide a steadily rising output voltage; When the MOSFET is turned OFF, the current flows from R1 and hence discharges the capacitor. Therefore, from the first op-amp falling output voltage is needed. Thus the cycle of charging and discharging produces a periodic output which is a triangular waveform.

Values of R1 and R5 determine the gradients of rising and falling edges of the triangle wave according to the integrator equations, as illustrated in Eq[1] below. The ratios 1/R1 and (R1-R5)/R1R5 controls the gradients of falling and rising slopes respectively. So in order to generate the most desired, upright triangle waveform, which means the two gradients need to equal in magnitude (1/R1= (R1-R5)/R1R5 ), a 2:1 ratio of R1 to R5 is required. And therefore duty cycle of the square wave produced in next stage will be 50% as it takes the same time for an upright triangle wave to reach the two threshold levels. This also gives a basic idea of how to generate a sawtooth wave.



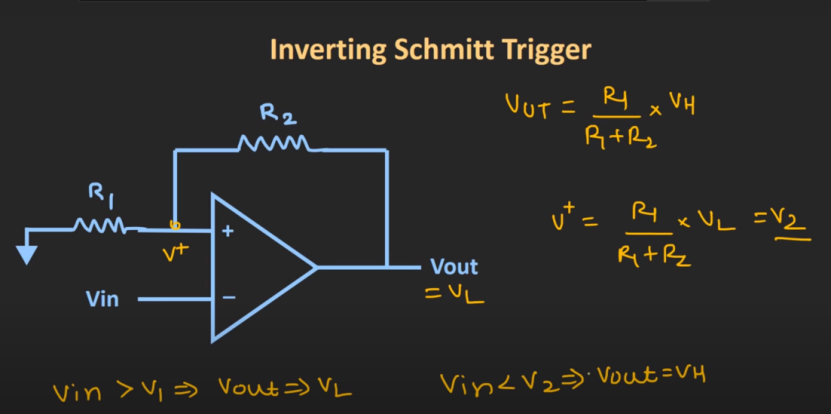
**Eq[1] equations for integrator( y(t):output of integrator; vin: dc input;**

**Left: when mosfet off; Right: when mosfet on)**

These equations were derived by applying KCL taking the node at inverting input of op-amp.

* Schmitt trigger working principles and equations

The second amplifier works as the Schmitt trigger. In this stage the triangular wave from integrator is accepted as the inverting input and when it reaches the upper threshold voltage Vtu or falls below the lower threshold level Vtl of the Schmitt trigger, VCC and VEE will be outputted respectively. Hence a square wave with positive voltage VCC and negative voltage VEE is produced (marked as output 1 on Figure 1-1). The threshold levels are determined by ratio between R6 and R7(see Figure 1-1), as illustrated by eq[2] below. Then this square wave is used as the gate voltage of MOSFET which controls the direction of output from integrator, hence synchronizes the triangular and square wave.



Eq[2]:

Vut=R1/(R1+R2) \* VCC

Vlt=R1/(R1+R2) \* VEE

These equations are derived by doing KCL at node V+=Vin:

Vin/R1=-(Vin - Vout)/R2

Vin=R1/(R1+R2) \* Vout

-When Vin reach Vut: Vout=VCC(just before Vut is reached)

So Vut=R1/(R1+R2) \* VCC

-Similarly, when Vin decreases down to Vlt: Vout=VEE(just before Vin fall below Vlt)

So Vlt=R1/(R1+R2) \* VEE

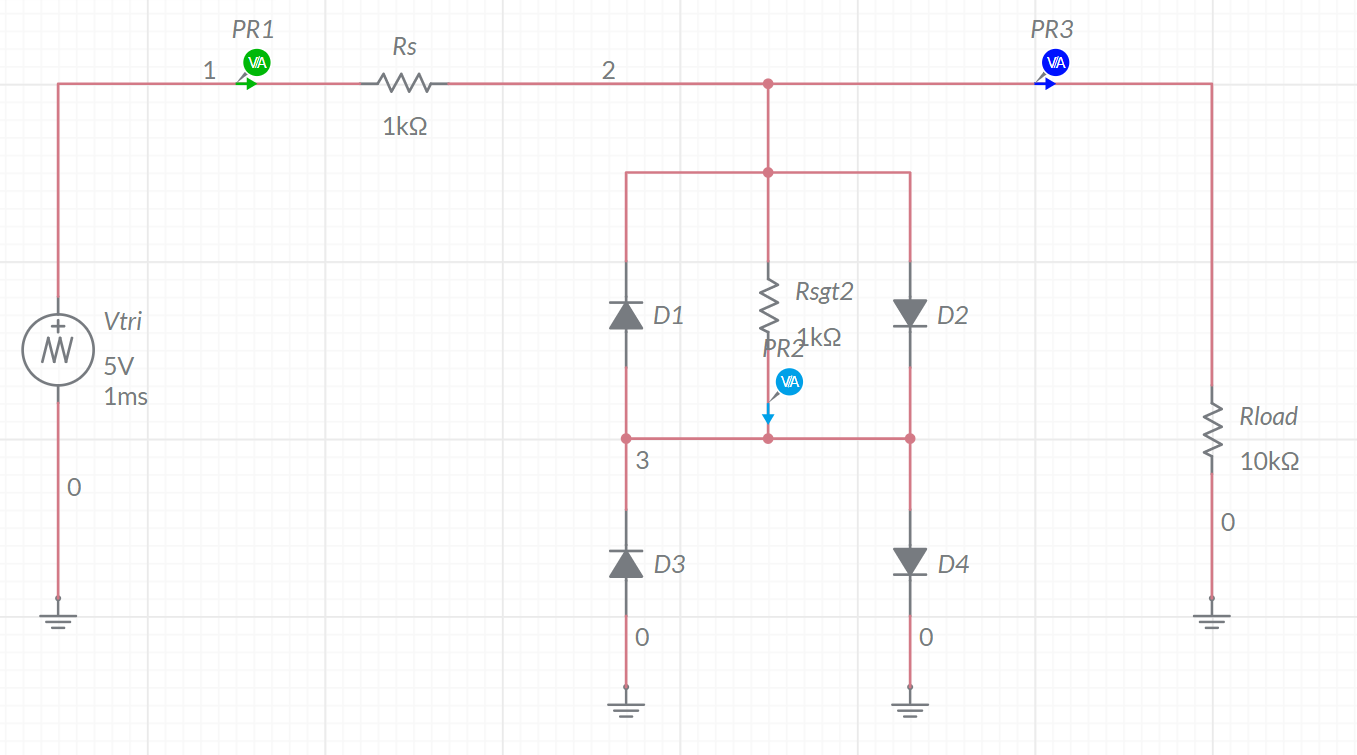
When Vin reaches Vut: output changes from high to low(VCC to VEE);

On the contrary, when Vin falls below Vlt: output changes from low to high(VEE to VCC).

**Eq[2] Vut and Vlt derivations of inverting Schmitt trigger**

* How to generate sine wave

The third stage is a triangle to sine wave converter, which is added to output 2 (see Figure 1-1). Instead of using a simple RC filter, a Four-Diode Three-Segment Triangular To Sine Wave Shaper (Figure 1-2) was used for reason that will be explained experimentally later in the next section.



**Figure 1-2.Four-Diode Three-Segment Triangular To Sine Wave Shaper Schematic(ref[1.2])**

This circuit reshapes the triangular wave into a segmented approximation of sine wave and this version produces 3 segments per quarter cycle. As presented in Figure 1-2, when the input is at a very low level, all diodes are reverse-biased and therefore the circuit is just a voltage divider formed by Rs and Rload, which forms a linear segment at the beginning of output (marked PR3 on the diagram). As magnitude of input increases eventually and is sufficient to turn diode D4 (if voltage at PR2 is greater than 0.7V) or D3 (if PR2 voltage smaller than -0.7V) on, the current diverted to D3 or D4 branch will reduce the slope of the output voltage. This results in the second segment of the approximation to sine wave. As the input magnitude increases further, D1 (if input is negative enough) or D2 (if input is positive enough) also become forward-biased and more current is diverted from the input, which leads to further decrease in the slope of output. This is the third segment of the approximation.

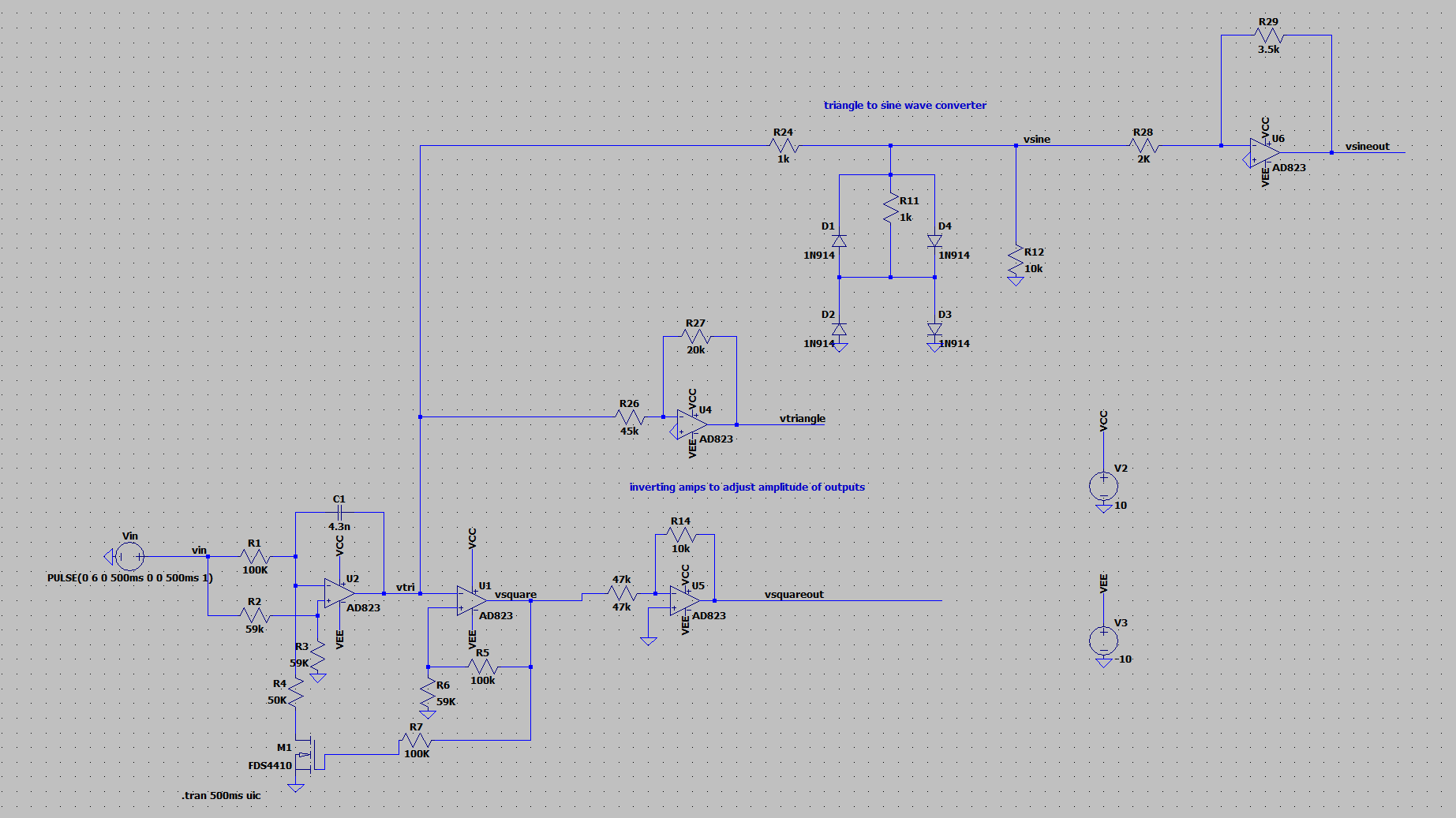
Frequency of the output waves depends on value of the dc input. For larger input, the linear wave produced by integrator at the beginning has steeper slope, therefore reaches threshold voltages of the Schmitt trigger quicker. Then a more frequent square wave is outputted and MOSFET switches between on and off more frequently, sequentially results in a more frequent triangular wave.

The above expectations and theories will also be proved experimentally by simulation result in the next section.

1. **Schematic, Selection of components, testing process and adjustments**

* How were the NMOS and op-amps selected?

Having tried most of the NMOS and op-amps available in library of LTSpice, FDS4410 and AD823 were found to give the fastest simulation. According to the data sheet of FDS4410 (see Appendix), the gate threshold voltage VGS(th) of this MOSFET was around 3V, so a square wave of 20V peak-to-peak would be sufficient to turn this MOSFET on and off. Therefore, +10V and -10V were chosen as VCC and VEE of the op-amps respectively.



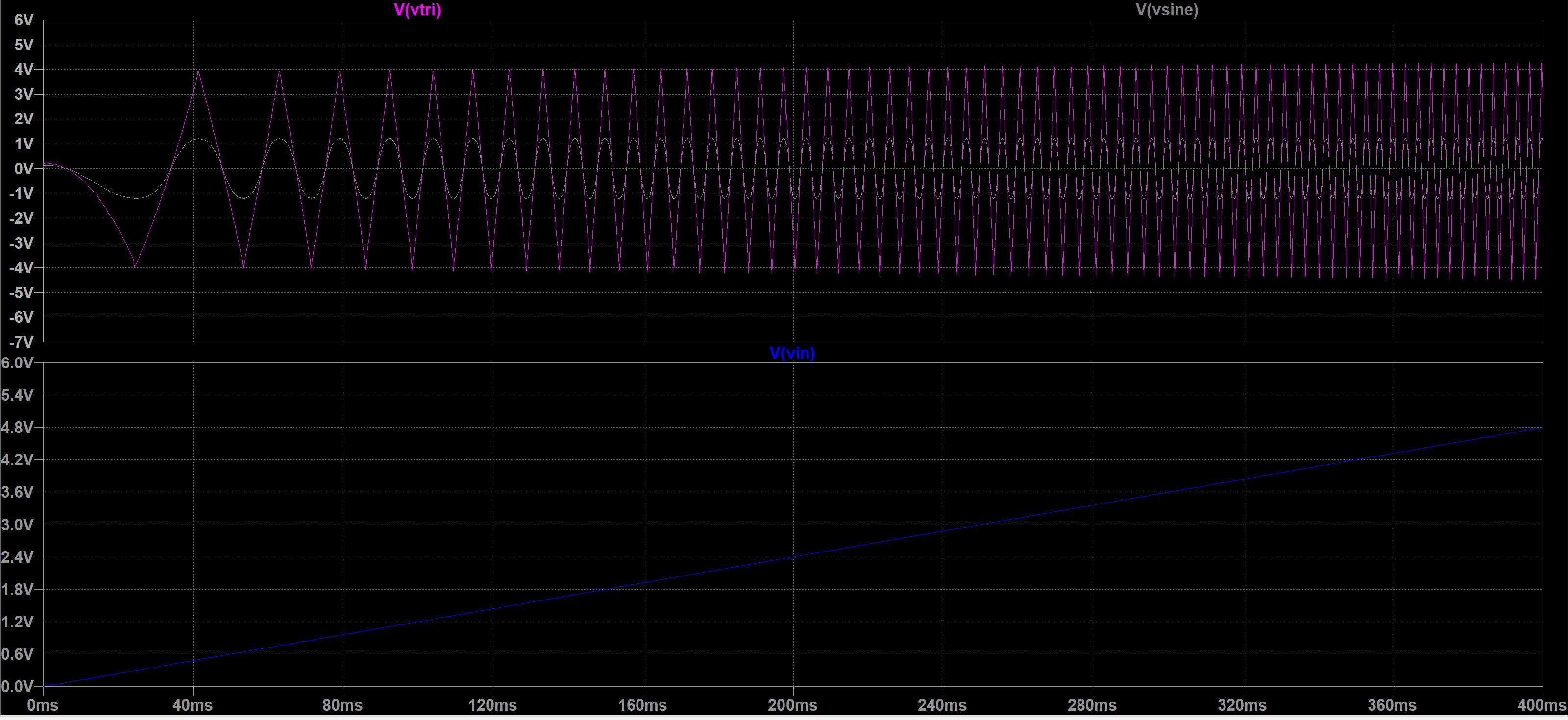
**Figure 1-3. VCO**

* How were the resistor values selected?

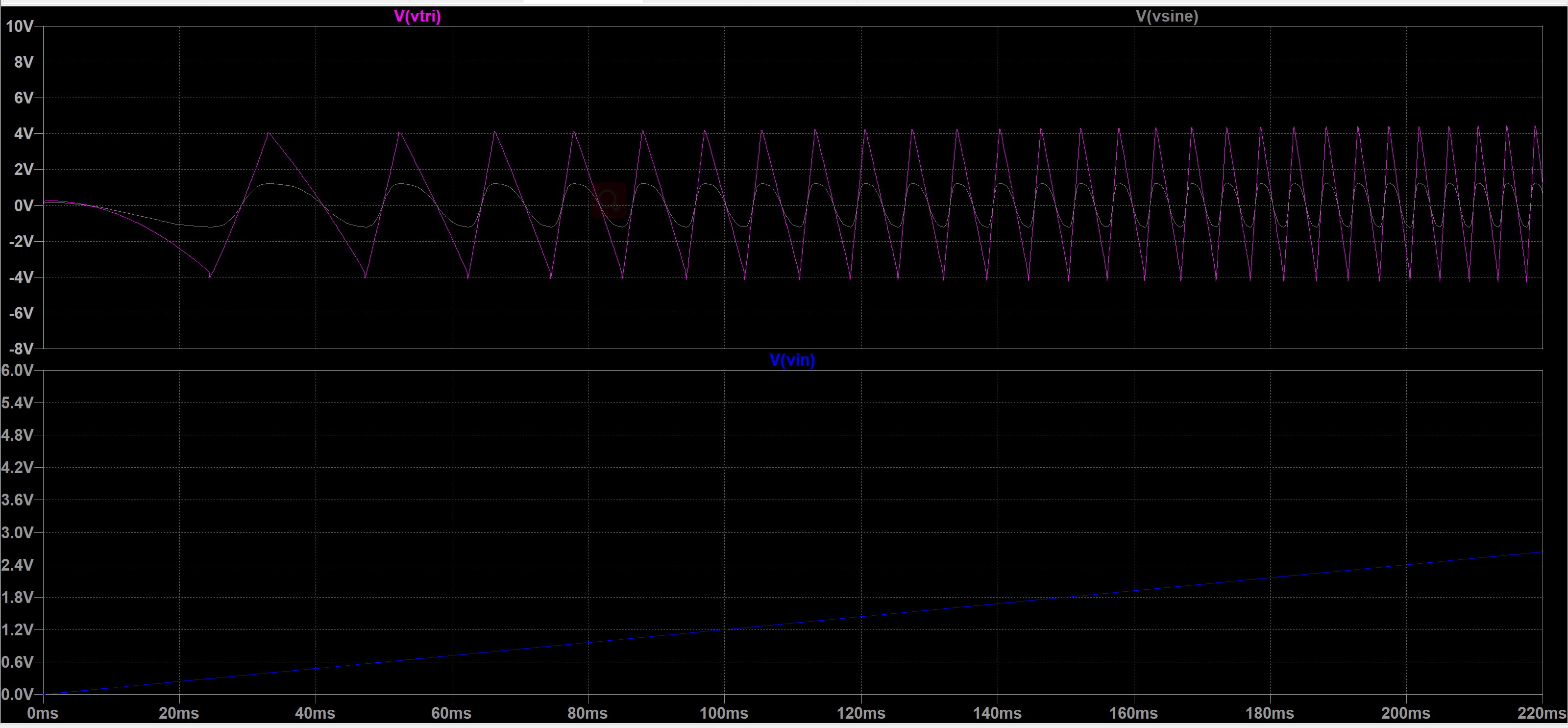
As shown in Figure 1-3, U2 works as the integrator and U1 constructs the Schmitt trigger. U4, U5 and U6 are just inverting amplifiers that balance the amplitudes of each wave to approximately same value (around 2V) by finding out the ratio between them and selecting resistor values using equation for inverting amplifier: Rout=-Rf/R1 \* Vin, where Rf is the feedback resistance and R1 is resistance imported to the inverting input.

As concluded in previous section, we inferred that a 2:1 ratio between R1 and R4 in Figure 6(R4 in Figure 1-3 corresponds to R5 in Figure1-1) would make the positive and negative gradients equal, producing upright triangle waves and sine waves. So 100k and 50k were selected. Figure 1-4 is a comparison between the resultant triangle waves by varying ratio of R1 to R4, which indicates how sawtooth wave can be generated.

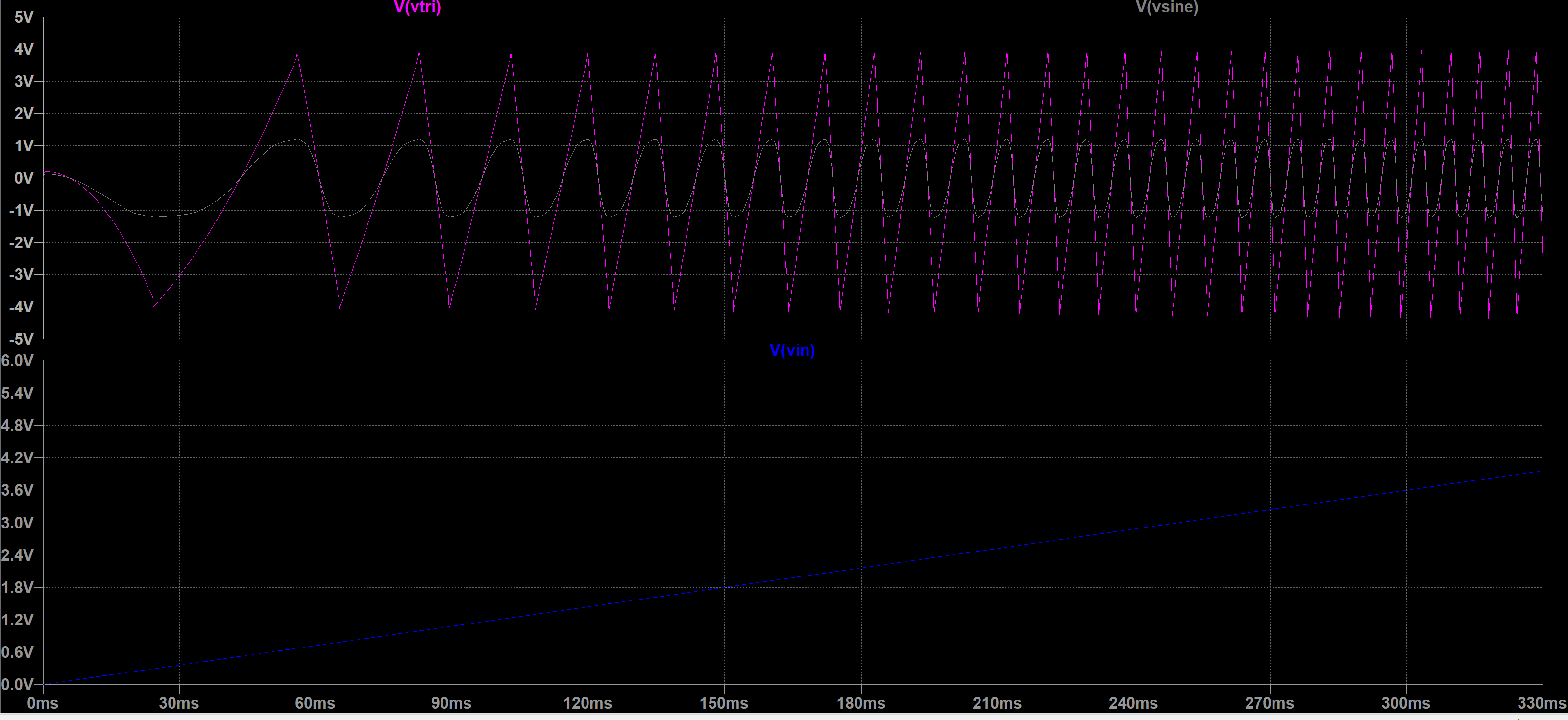
1. R1:R4=2:1(100k and 50k):upright:



1. R1:R4=10:3(100k and 30k):triangle tilts to the left:



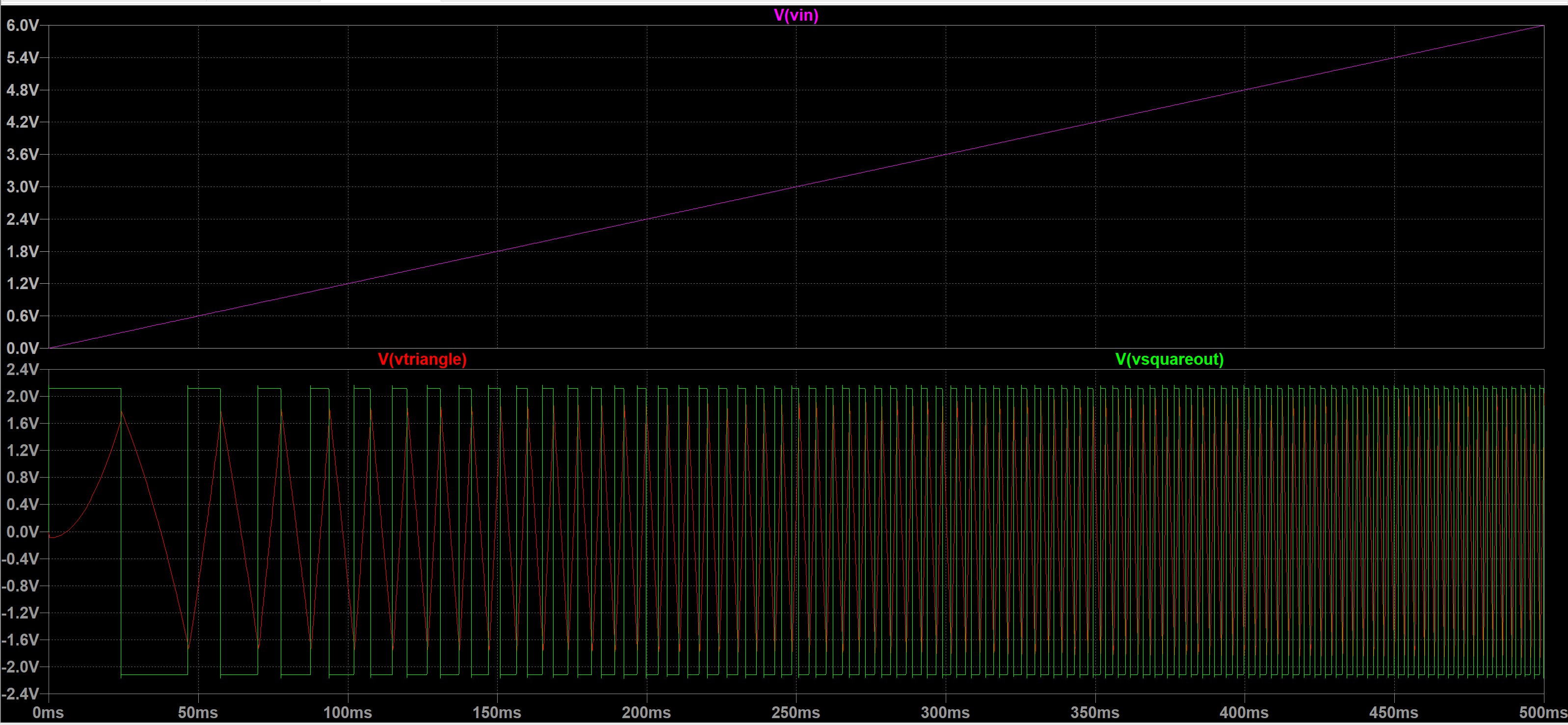
(3)R1:R4=10:7(100k and 70k):triangle tilts to the right:



**Figure 1-4. Change in shape of triangle wave as R1:R4 ratio varied**

* How to vary the frequency

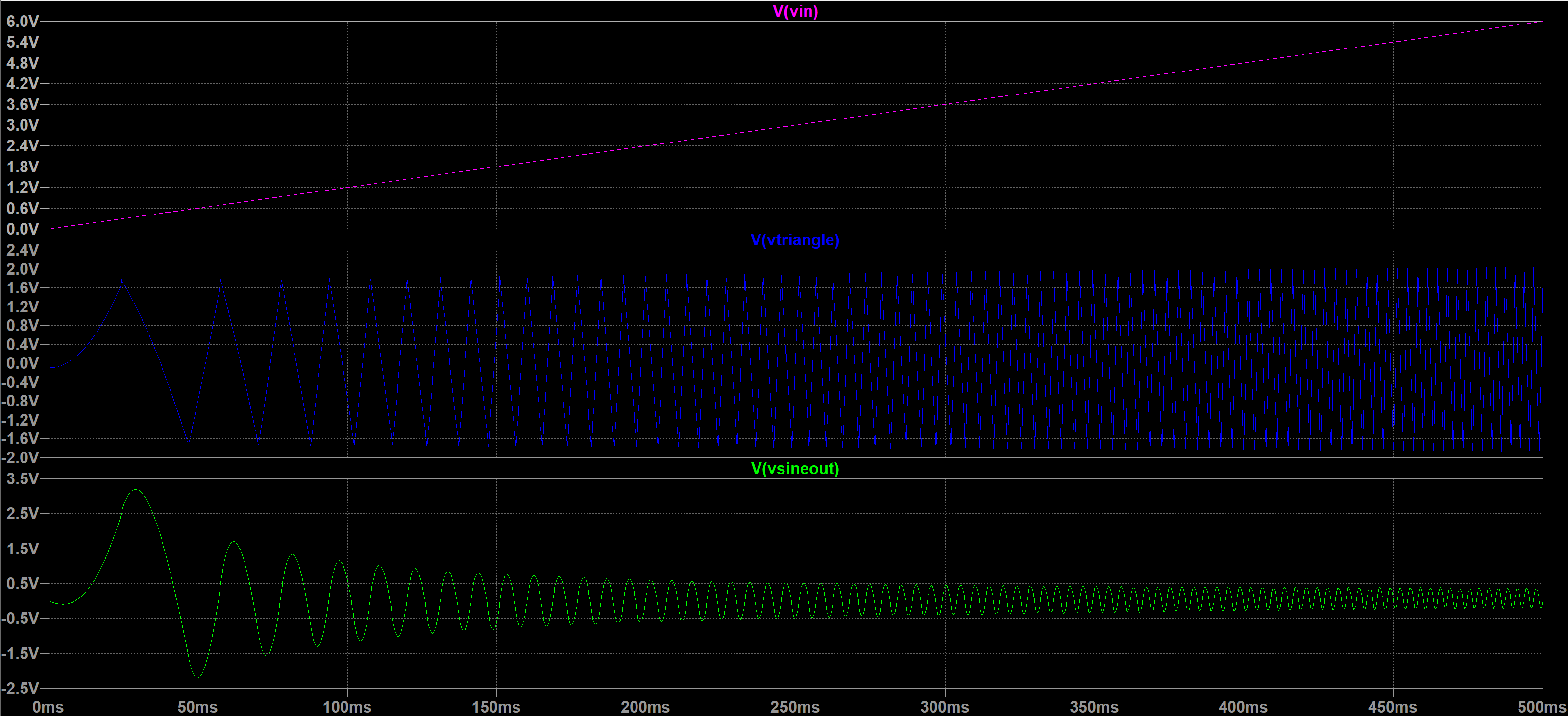
Relationship between the outputs signals and the input voltage is shown in Figure 1-5 below. By inputting a linearly increasing voltage, it is obvious that frequency of output has also increased , which is a proof of what was inferred before.



**Figure 1-5. Change of frequency with input voltage(top: vin; bottom: red triangle, green square)**

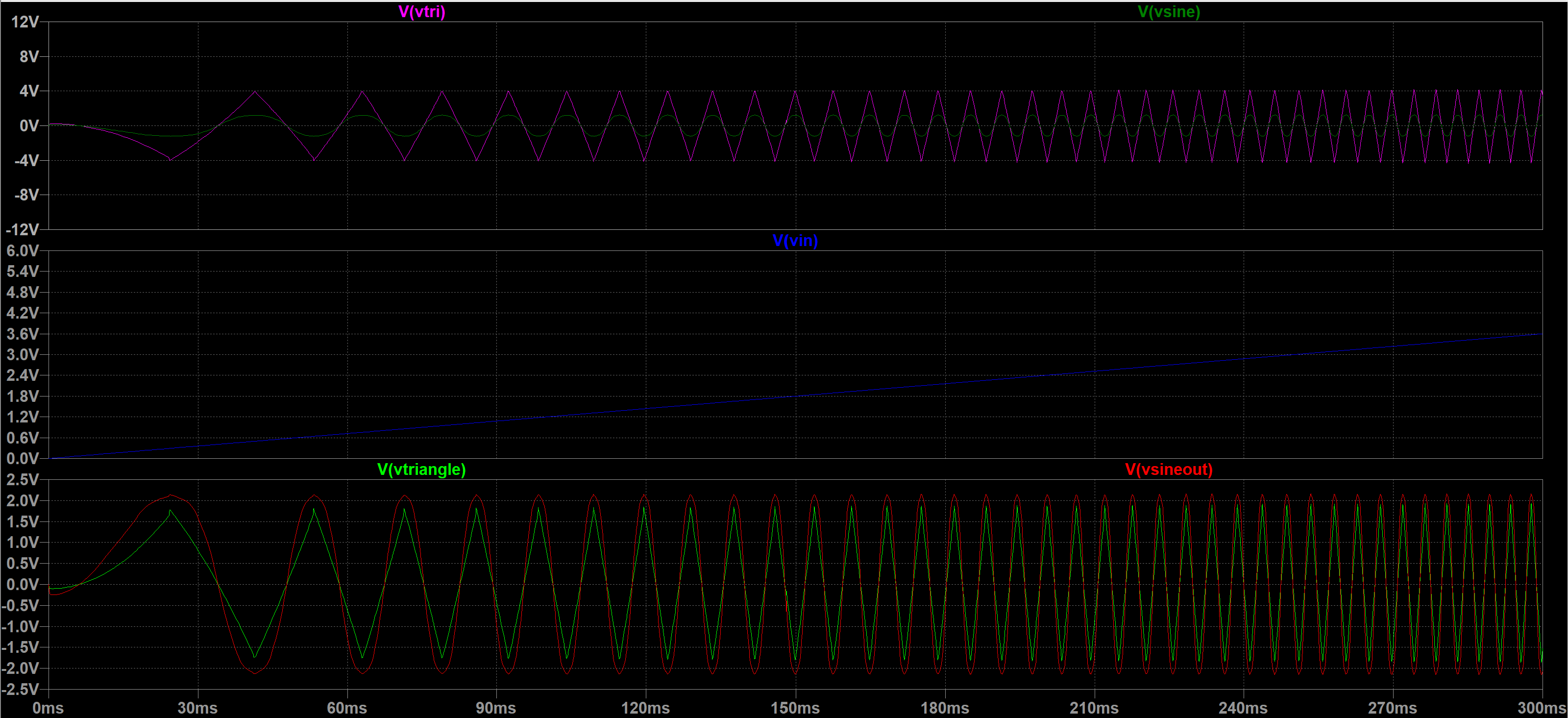
* Why not RC filter?

Reason for not using RC filter, which we designed in the very first version of VCO to transform triangular wave into sine wave, is that the amplitude of generated sine wave varies with the input voltage, as what is demonstrated in Figure 1-6 below. For fixed valued R and C, the threshold voltage is settled. As frequency of inputted triangle wave rises, amplitude of generated sine wave has decreased to a very small value, which is not desirable.



**Figure 1-6. decreasing amplitude of sine wave as input increases(top: vin; middle: triangle; bottom: sine)**

Reason for this is that more harmonic signals are getting filtered off as input frequency goes up, relating to the Fourier Transform of sine wave. So instead, the converter is used which produces sine waves with constant amplitude. In this case the amplitude is no longer affected by the changing frequency but only depends on the amplitude of the triangle wave, as shown in Figure 1-7.



**Figure 1-7. converter output for increasing frequency(top: triangle and sin waves before balancing amplitudes; middle: vin; bottom: triangle and sine waves after balancing amplitudes)**

Furthermore, value of the capacitor was determined experimentally by making slight changes referring to the value given in Figure 1-1 in order for the VCO to give the required range of frequencies, as the speed of charging and discharging affects frequency of generated wave. By adjusting the input voltage and measuring frequency manually, the following table was obtained:

**Table[1]:Vin to frequency table**

|  |  |  |
| --- | --- | --- |
| **pitch** | **Corresponding Frequency/Hz** | **Vin to produce the frequency/V** |
| C-do | 261.6 | 4.8 |
| D-re | 293.6 | 5.4 |
| E-mi | 329.6 | 6.15 |
| F-fa | 349.2 | 6.6 |
| G-sol | 392 | 7.5 |
| A-la | 440 | 8.7 |
| B-si | 493.8 | 10 |

This table is needed for construction of keyboard, which will be presented in the following chapter.

* What can be added

If we had more time, sub-circuits to produce other waveforms such as sawtooth wave to create new timbres could be added. The circuit to create sawtooth wave is basically the same as that of the triangle wave except that value of the resistors in series with the capacitor (R5 in figure 1-1) would be different, according to the previous explanations.

Here the switching between different waveforms can only be done by manually reconnecting the different outputs of VCO to next stage, which instead can be done by adding 3 voltage controlled switches to each of the outputs and include them as part of the user interface.

But to ensure that the system is not overloaded, only these three types of waves were generated and the outputs were left like this.

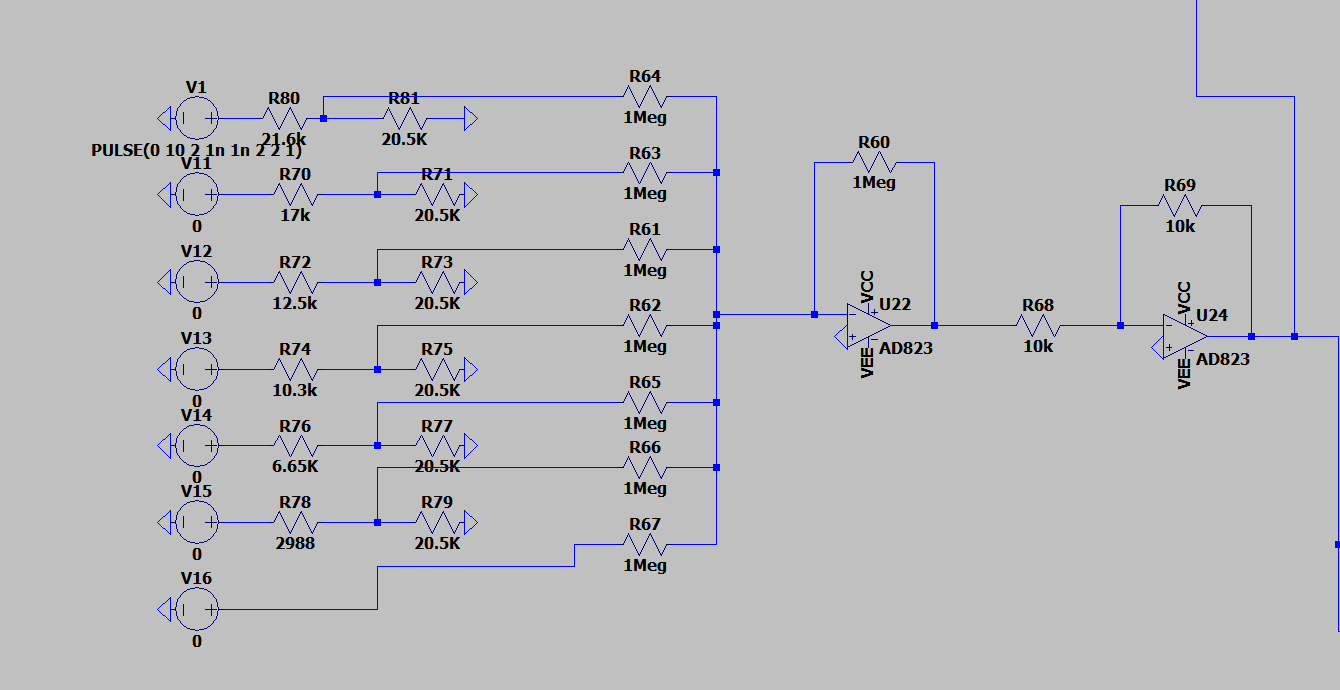
**Keyboard(user interface)[By Jingyi Wu]**

As the user interface stage, keyboard is the only module that can be controlled by the user, and takes the role of supplying the dc signal of particular values to the whole system. Below the whole process of designing, building and testing of the keyboard will be illustrated.

1. **Design and testing process**

* The initial thoughts

Referring to behaviour of VCO, an idea of using a summing amplifier as the keyboard came to our mind first(Figure 2-1).

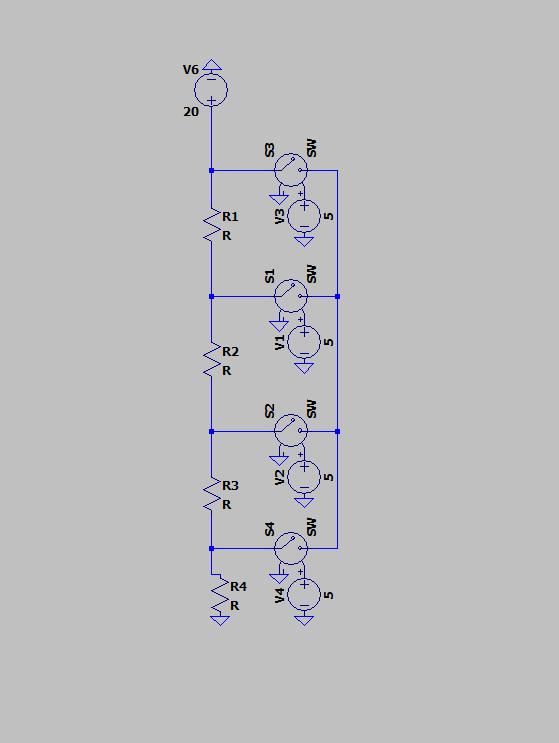


**Figure 2-1. Summing amplifier as input**

This circuit sums up all voltages at the inverting input of the op-amp. Each time only one voltage source is allowed to be turned on, and applying a 10V pulse represents the action of pressing and releasing a key. By selecting proper resistor values, the required Vin for each pitch is created at the point in between of the left-most 2 resistors(which construct a potential divider structure, see Figure 2-1). The input resistances of each line and the feedback resistance of op-amp were set to be equally large to satisfy the condition for adder to work: Rf=Rin.

This design worked well, but obviously has used too many resistors and added an amplifier to the whole circuit, which not only loads the whole system but also increases the total cost.

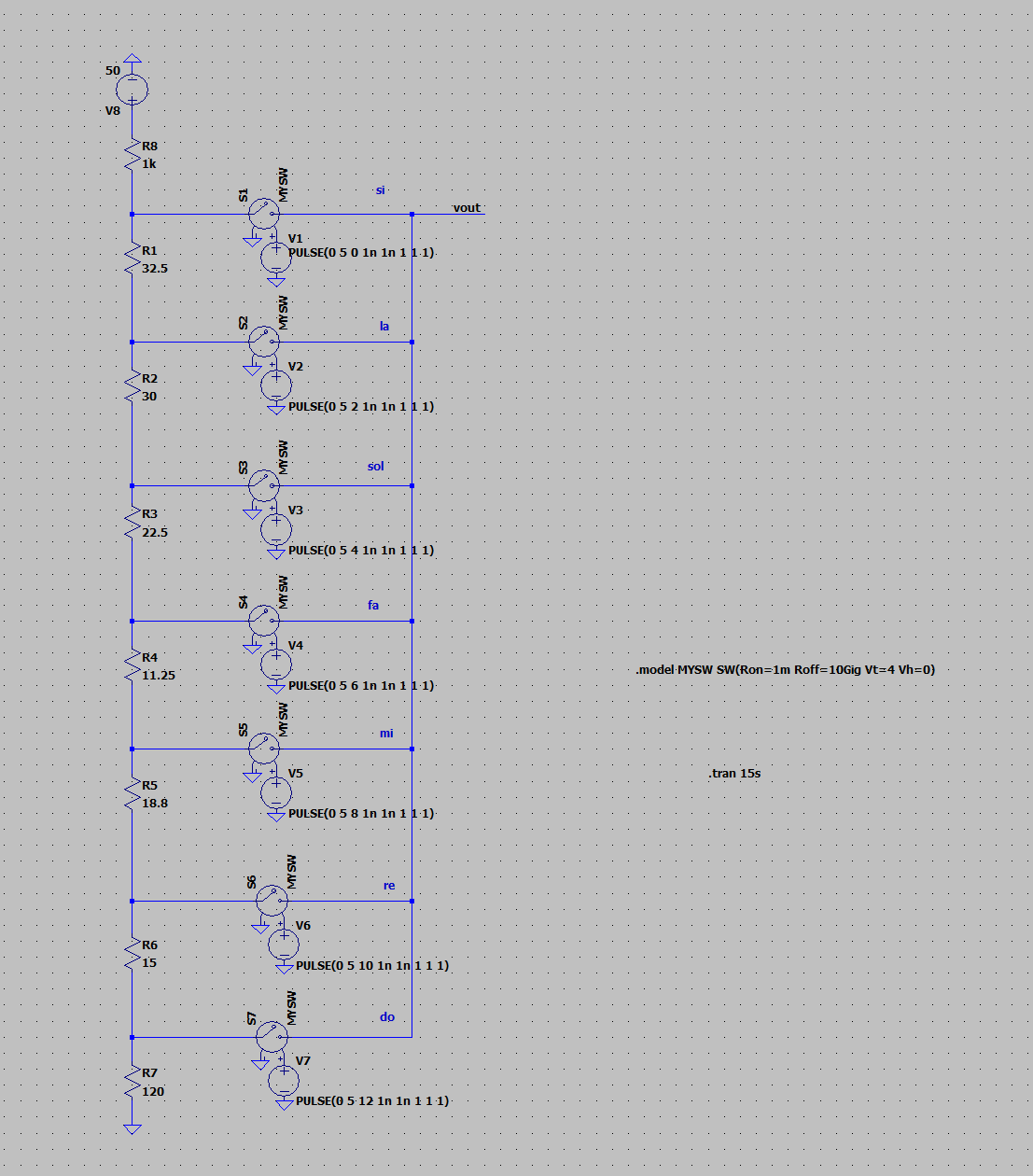
So to improve, a second idea of using a potential divider circuit combined with 7 voltage-controlled switches came about(see Figure 2-2), which uses fewer components and behaves in a cleverer way.

****

**Figure 2-2. Initial design of keyboard**

* Working principles of the premium design

The resistors are connected in series to act as a voltage divider and voltage controlled switches represent the keys, each will be turned on by applying a 5V control voltage, so applying a pulse to the control will also simulate the process of pressing and releasing a key. When one of the switches is turned on, the voltage at this point will be taken as the output. Values of the resistors were calculated to divide the voltage source into required Vin values(see table[1]), simply by calculating the ratios between the resistance from sampling point to ground and the total resistance (applying potential divider rule). Then we got the first premium version of the keyboard(Figure2-3).



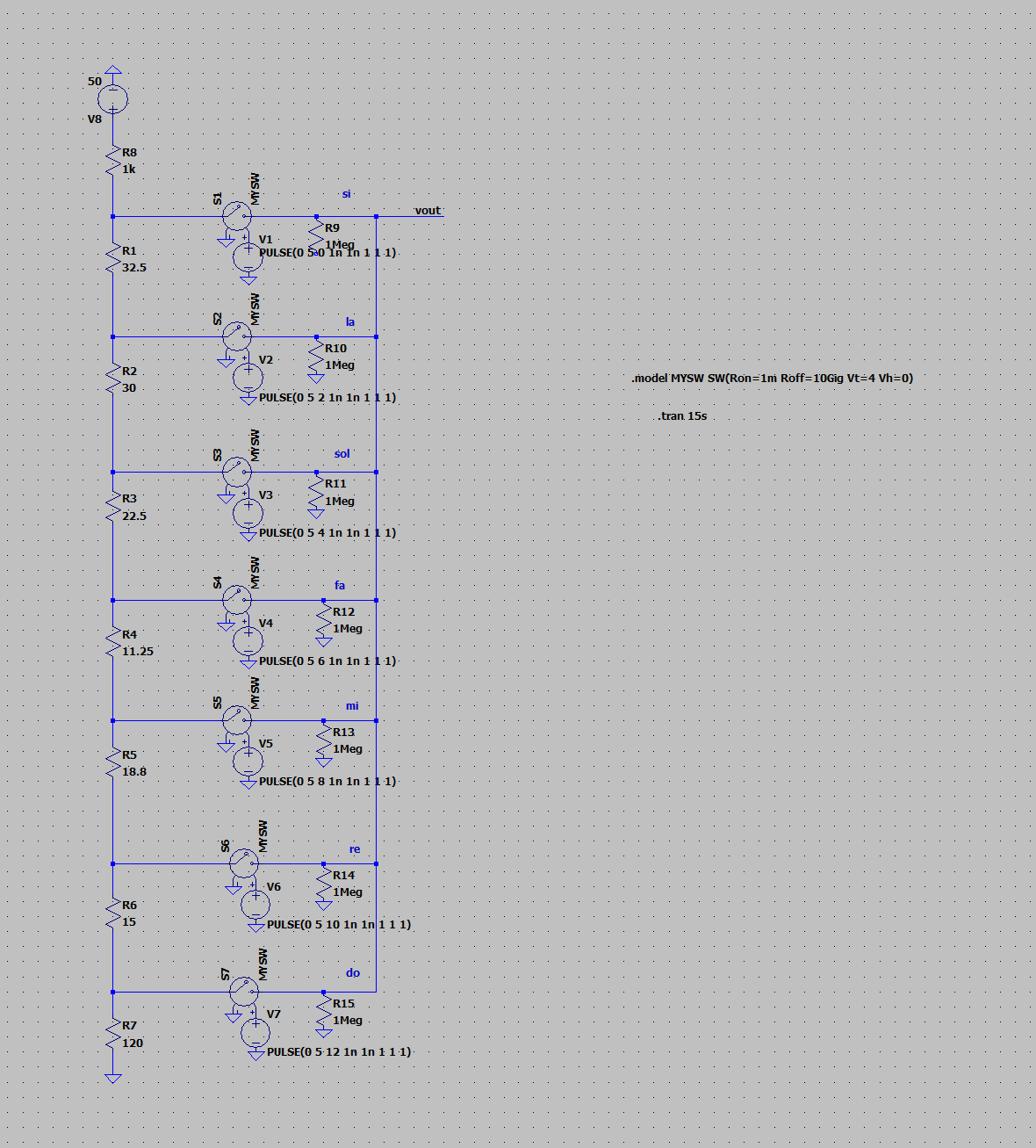
**Figure 2-3. First draft of keyboard**

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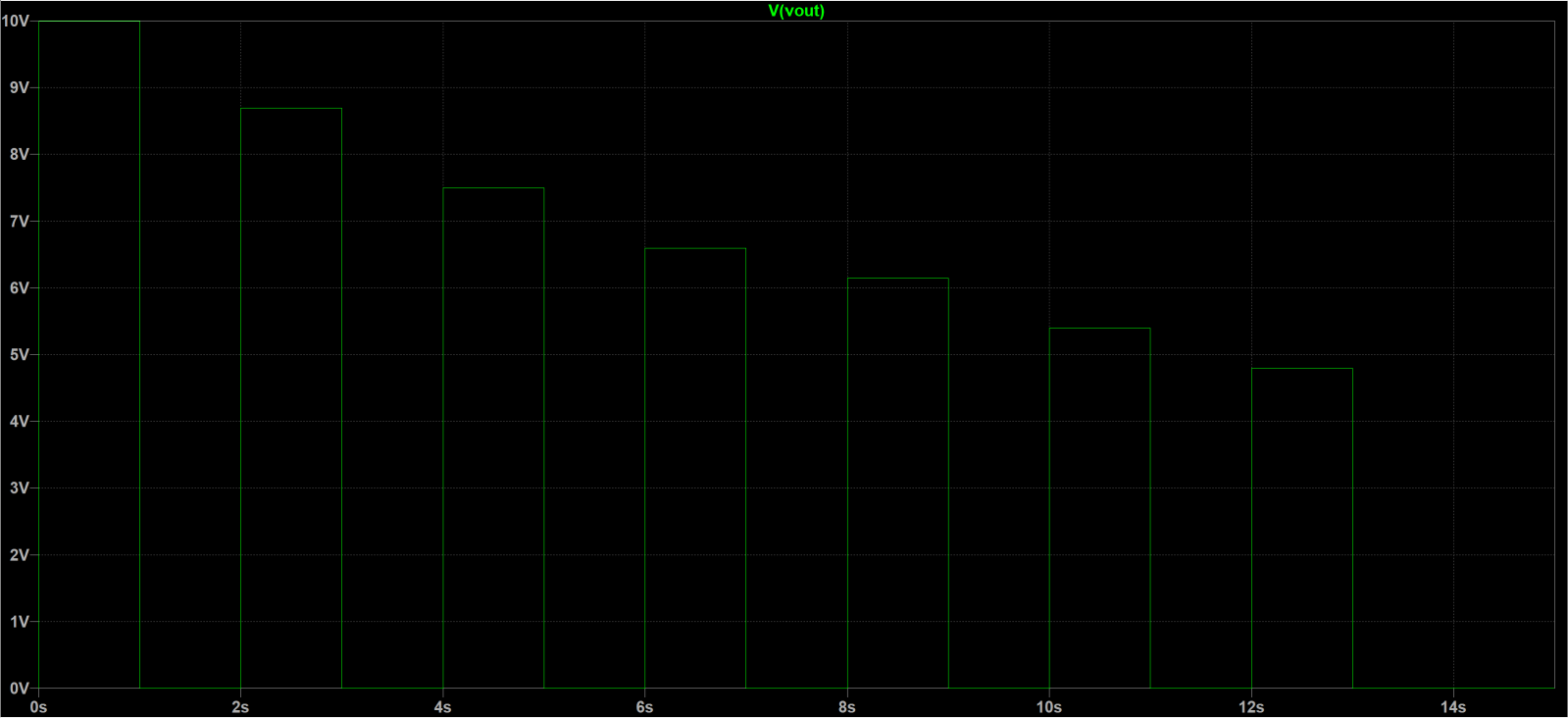
**Figure 2-4. simulation result of 1st draft**

* Issues and solutions

The control voltages were 5v pulses with different time delays, representing the situation of pressing the keys one by one. However the simulation result (see Figure 2-4) showed that the output was not zero when all switches were closed. So to solve this problem, a large resistor was added to each line(see figure 2-5, 2-6) to ensure that the output point is grounded when all switches are closed and no voltage loss from the potential divider arrangement.



**Figure 2-5. 2nd draft of keyboard**

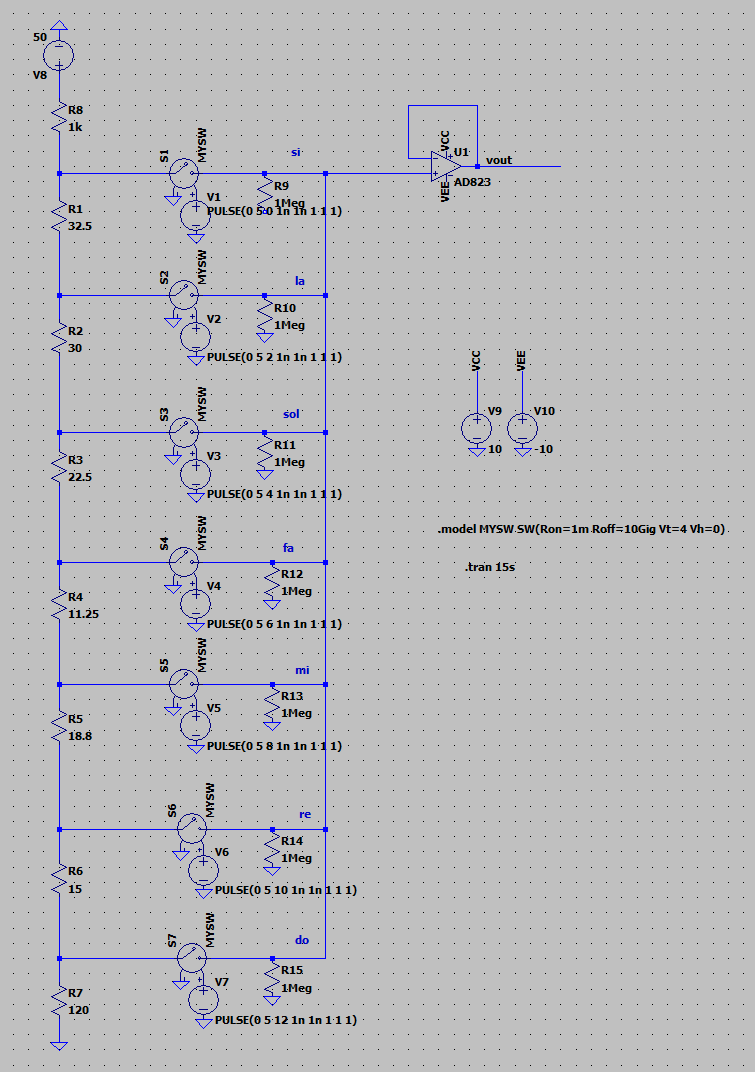
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**Figure 2-6. 2nd draft simulation result**

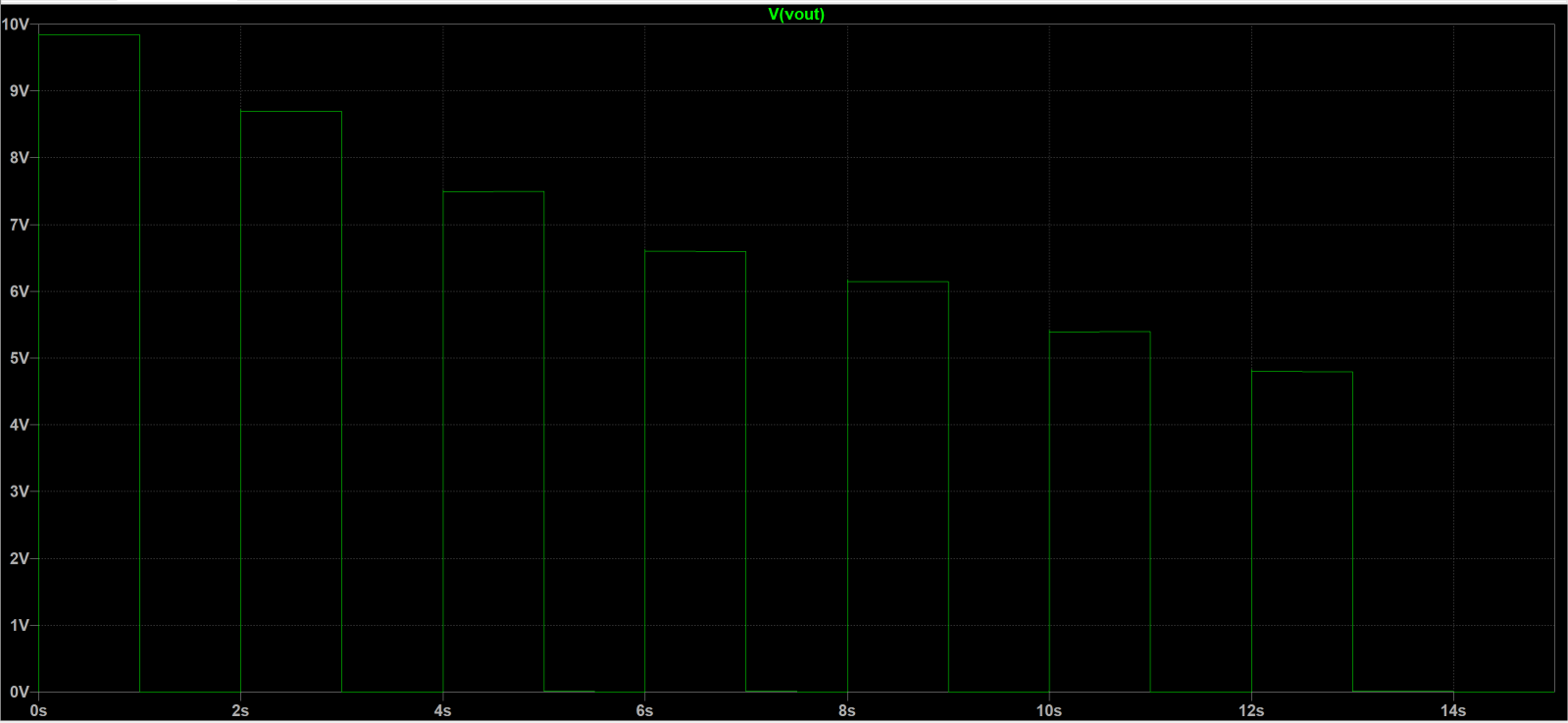
Now the step decrease in the outputted dc voltages became very clear.

* More improvements

Finally to guarantee that the dc voltage into VCO won’t be affected by resistance of this input stage, a unity gain amplifier is added in between the two modules as a buffer and separates the two stages(see figure 2-7) by cutting off the current and diverts only the voltage to the next stage.



**Figure 2-7. final version of keyboard**

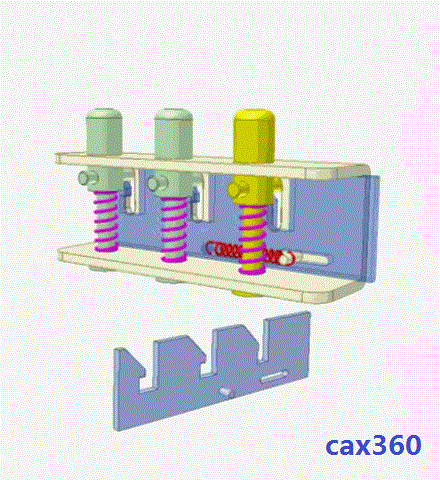
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**Figure 2-8.keyboard final version simulation result**

The result had no difference before and after adding the buffer, guaranteed that the outputted signal would not be altered.

* How to optimise?

For this monophonic synthesiser design, only one key is allowed to be pressed down each time, or the input voltage will be too large and blow up the whole circuit. If not cautioned to the user, this might only be possible through some mechanical engineering to the keys in reality (can refer to the design of buttons of table air fans, see gif[1]).

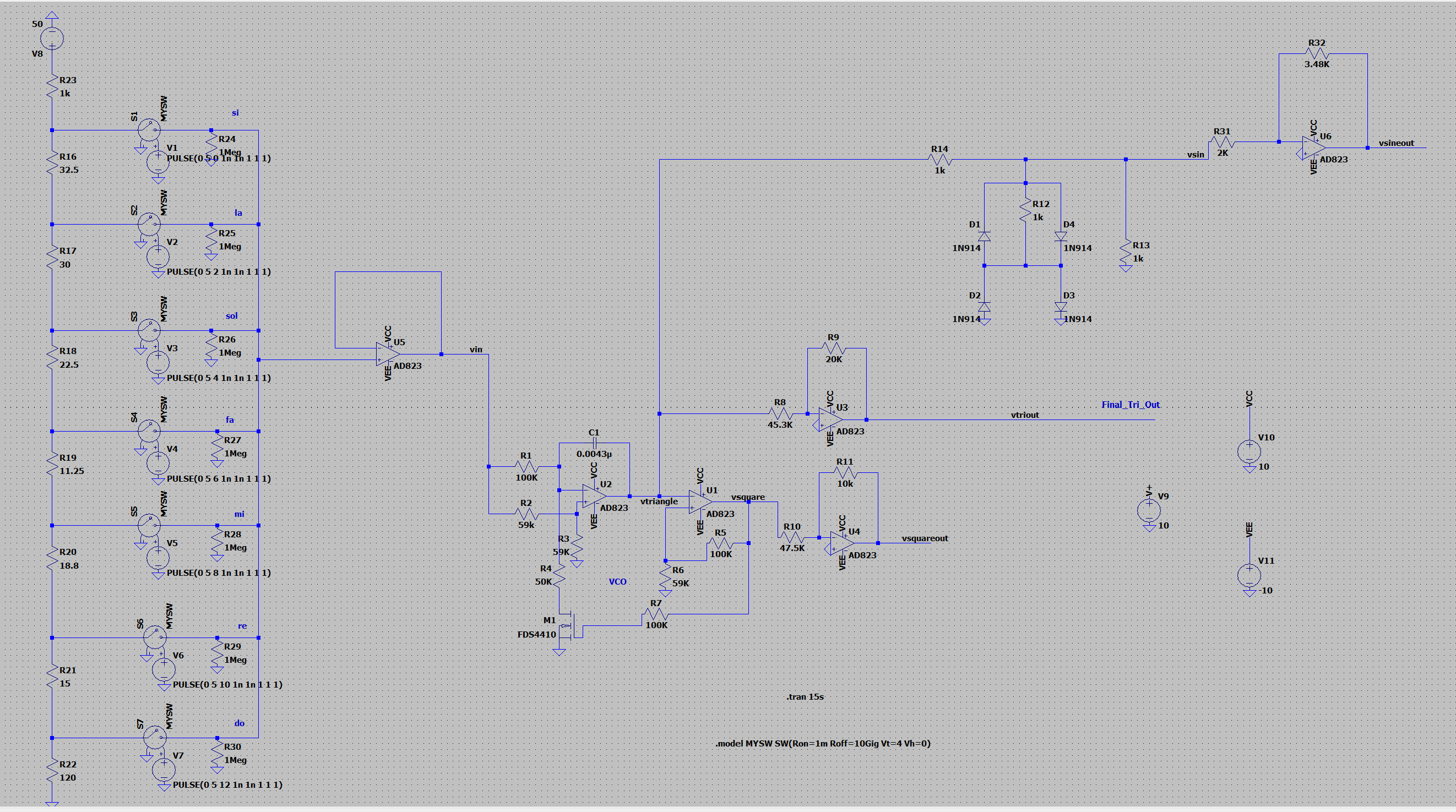
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**Gif[1].buttons of air fans**

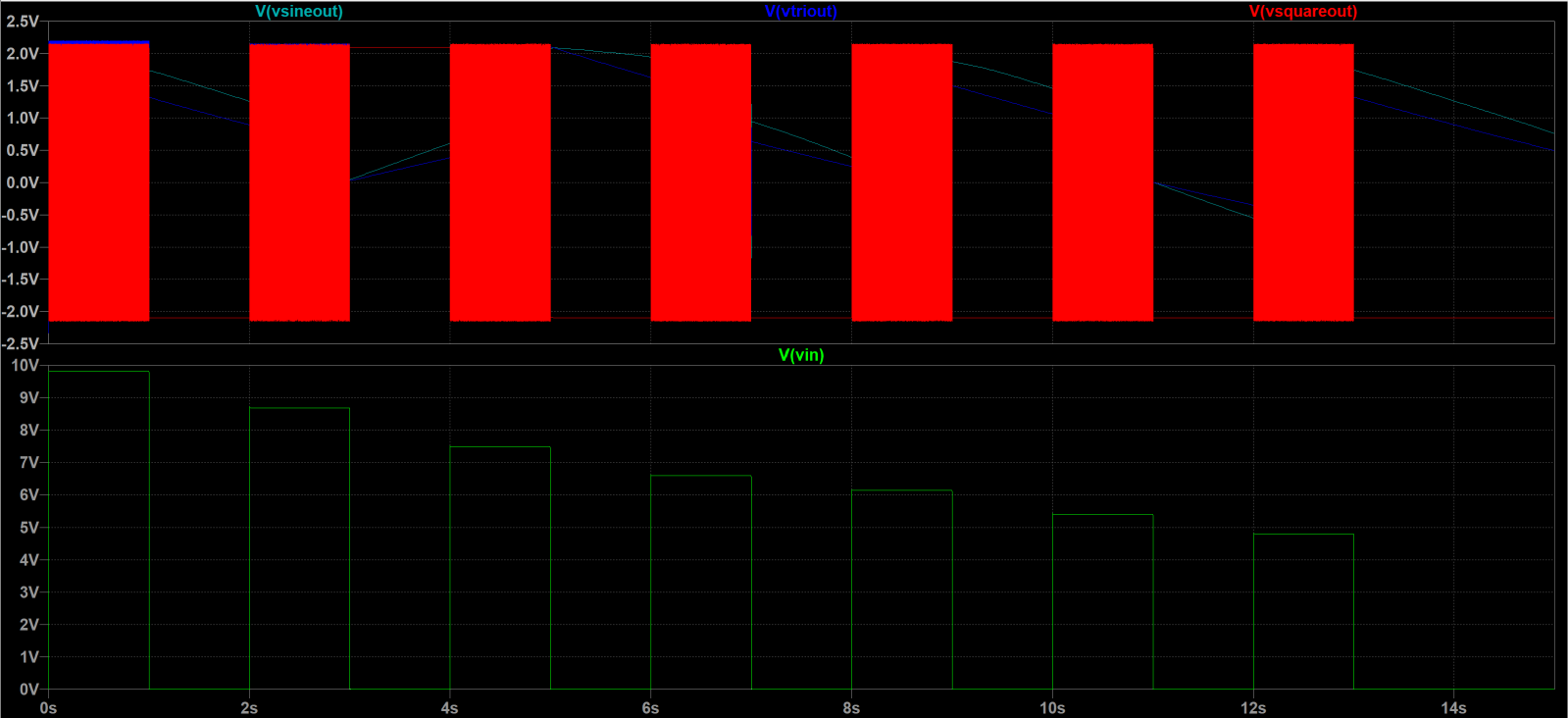
**(when one button is pressed, pressing another one will pop it up.**

**Gif found online)**

1. **Test with VCO**



**Figure 2-9. full schematic of keyboard connected to VCO**

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**Figure 2-10. simulation result of the connected circuit(top: outputs; bottom: input from keyboard)**

**Each square is a set of the three waves, frequency of each set is different**

From the simulation result we can see that 7 pulses were inputted to VCO from keyboard, representing each key being pressed in turns. And outputs were 7 sets of waves, each consists of the 3 waveforms and had different frequencies. This will be demonstrated in more detail in the video presentation.

**Voltage Controlled Filter [By Zhaoyu Wu]**

1. **Intro**

Filtering is not vitally needed like the oscillators in the synthesizer design. But their presence is still crucial in sound processing. A filter, with variable cutoff frequency, gives the synthesizer’s final audio output more variations. By filtering out some parts in the signal’s frequency spectrum, it makes the sound either deep and oppressive (usually low cutoff frequency) or bright and sharp (usually high cutoff frequency). Normally a well-functioning synthesizer consists of three types of filters: low pass, high pass and band pass (Twin-T notch type can also be seen in some modern synthesizers as they can filter out a harmonic wave with a specific frequency). Due to the time limit, a frequency adjustable low pass filter was considered to be built, as it could retain the fundamental component of the signal and it’s also widely used in lots of electric products.

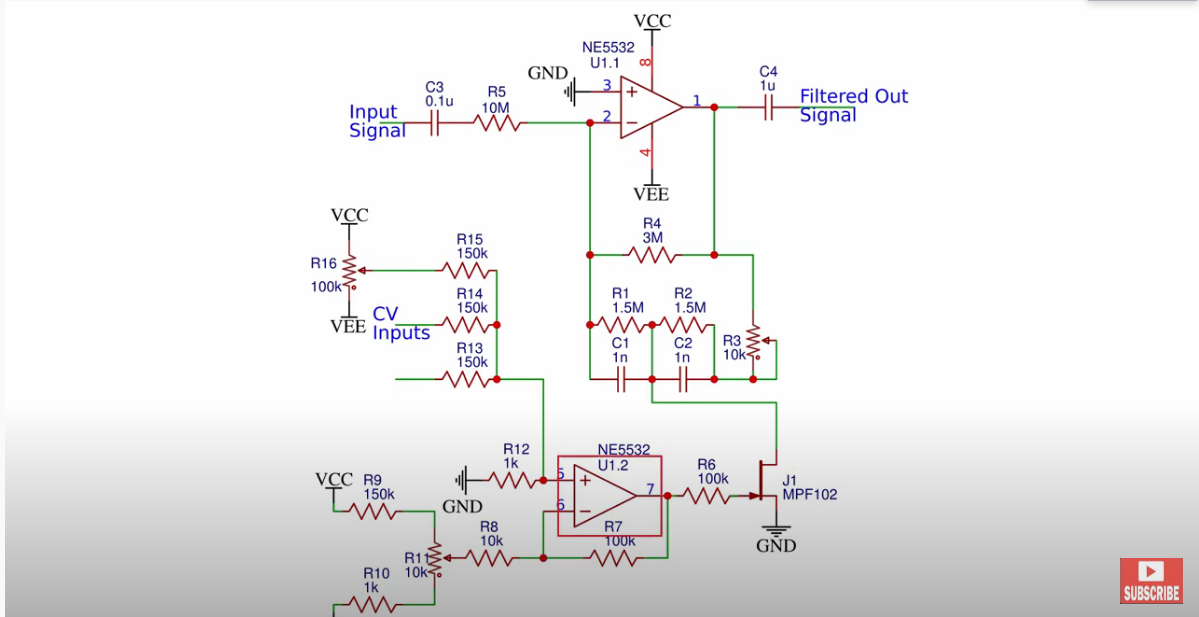
1. **Initial design**

Initially an RC filter was considered, as a prototype of the LP filter. This was the simplest filter that we’d already learned in college. Its formula is easy to derive and its cutoff frequency can also be controlled with precise calculation. The idea was that by changing the resistor into a potentiometer (which acts as a modifiable resistor, a user input), the user can change the value of the cutoff frequency by sliding up and down the potentiometer control. However a problem soon occurred that when an alternating signal (with fixed frequency) representing a curve outputted by VCO is fed into the filter input, the bode plot in AC sweep showed that the output amplitude varied significantly with resistor value (hence cutoff frequency). The reason is that the Fourier coefficients of different harmonic component of the inputting signal are different, with different components filtered out due to different cutoff frequency, the final output consist of varied signal components with diverse amplitudes. This is a critical issue for passive filters as they attenuates the signals. Another reason that this design is not adapted is that the cutoff frequency is controlled manually, rather than using voltage. So there’s no way to attach a LFO to it to give even more sound effects.

Hence an active VCF was to be designed. It needed to be active because this provides extra gain and negative feedback to ensure the output signal amplitude is stable. The VCF filters the signal with its cutoff frequency determined by the control voltage modified by users. The aim was to build a voltage controlled low pass filter with its cutoff frequency varying from about several hundred HZ to several thousand HZ, since the inputted signal frequency varies within 500HZ. Another goal was that the cutoff frequency must at least varies with the control voltage in a positive relationship.

1. **Final design inspiration**

After some researches online, we discovered a clever design from a YouTube website.



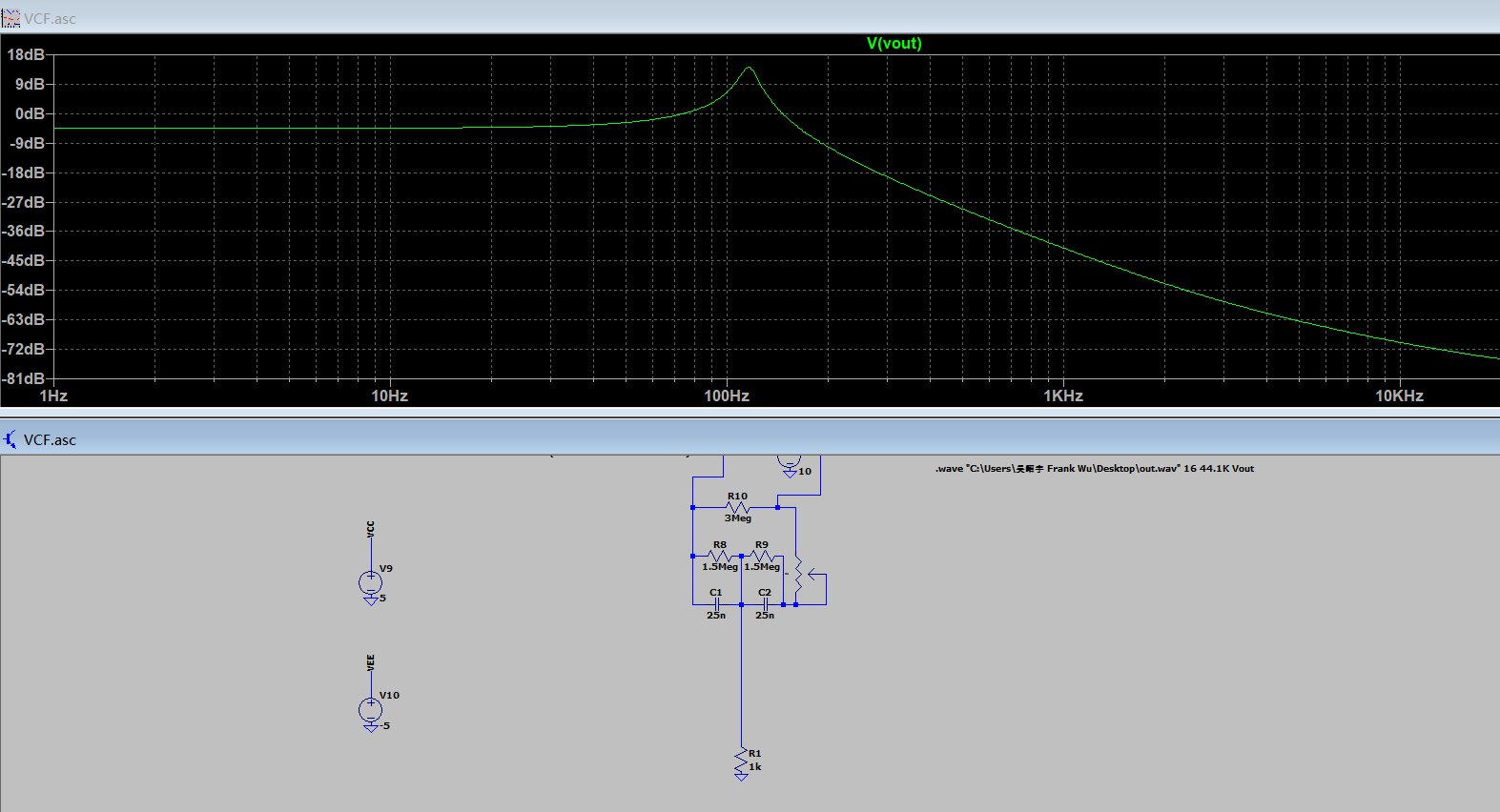
**Figure. 3-1**

**“DIY Analog Synthesizer Part 3: The Voltage Controlled Filter (VCF)”**

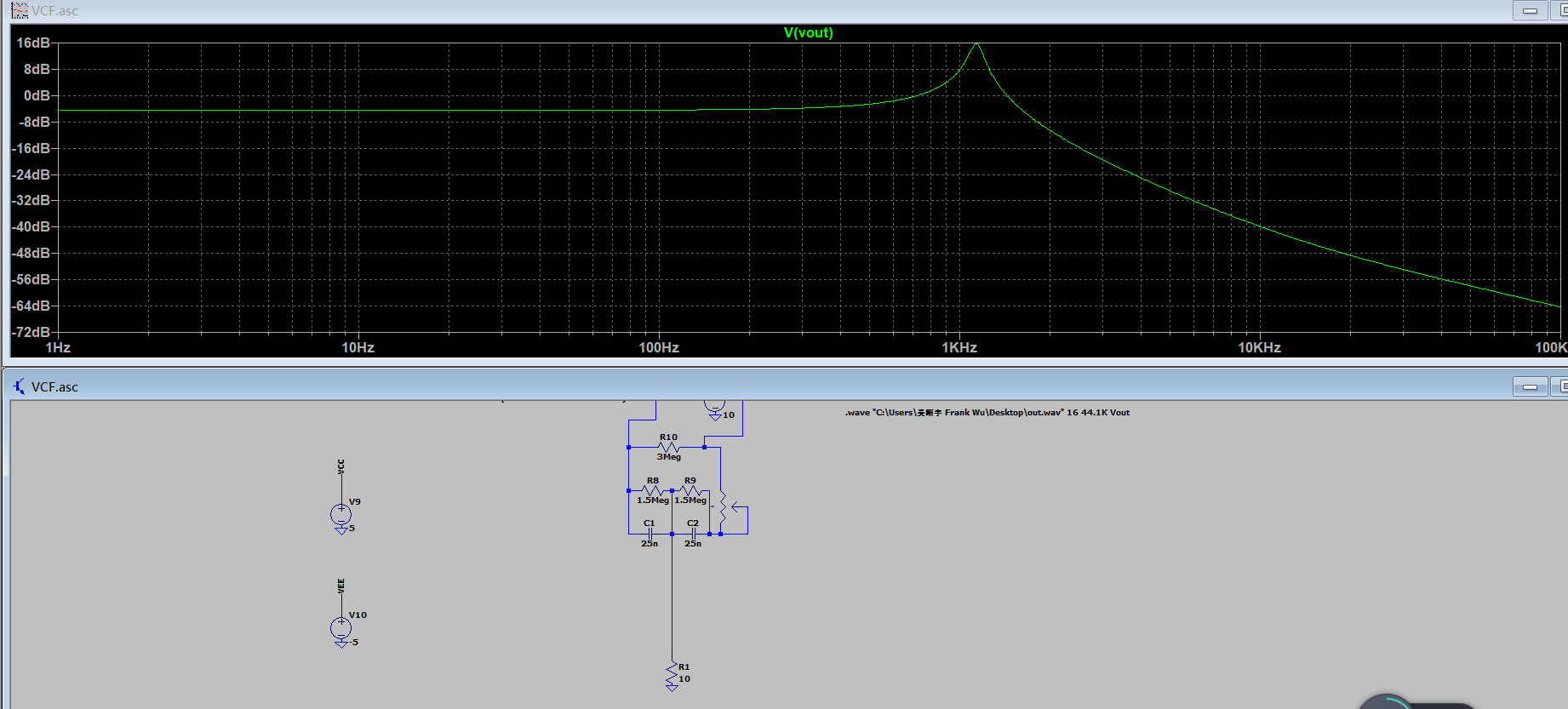
**(Ray Wilson , “VCF Four Pole 24dB/Oct With VC Resonance” as cited by Youtuber: Something's Gone Wrong!)**

The key to this VCF is the jfet J1, it acts as a voltage controlled resistor. Hence it should have something to do with the cutoff frequency. On its left is the whole circuitry used to provide the control voltage feeding into the gate of the jfet. What’s above the jfet’s drain terminal is the circuitry acting as the true active low pass filter. It has negative feedback to stabilize the output amplitude. This schematic is not exactly same as our VCF final schematic, since there’s no exact type of MPF102 jfet in LTspice library. Besides, it is discovered that, after copying this schematic to LTspice with some adjustments, other jfets in the library does not make the filter perform very well, the cutoff frequency does not vary much. This maybe because the threshold voltage is too low and the Vgs is negative for jfet. This design with jfet is not adapted also due to our lack of familiarity to jfets. Instead, we decided to first analyze the main filtering circuitry.

By taking node method and phase analysis at the top amplifier’s inverting terminal (with a voltage to be 0 due to the negative feedback), and regarding the jfet as an actual resistor with changing resistance, a rough transfer function regarding input and output was derived. It was rough because it would take tons of time to get the precise formula and the result may be very complicated. So instead only the factors related to jω and its higher orders are approximated. It is discovered that the numerator and denominator both have factors containing ( jω)^2, indicating that as the frequency is low and the gain would be a fixed constant. Combining this with later simulation results, they show that the design is indeed a low pass filter. The denominator (a quadratic factor) provides the resonance which boosts the amplitude of the output signal at cutoff frequency. And the peak in bode plot is controlled by the R3 potentiometer. This resonance phenomenon was observed and proved later in the tests and simulations. The cutoff frequency is controlled by changing how close the two capacitors are to ground, this is done by varying the resistance provided by the jfet.

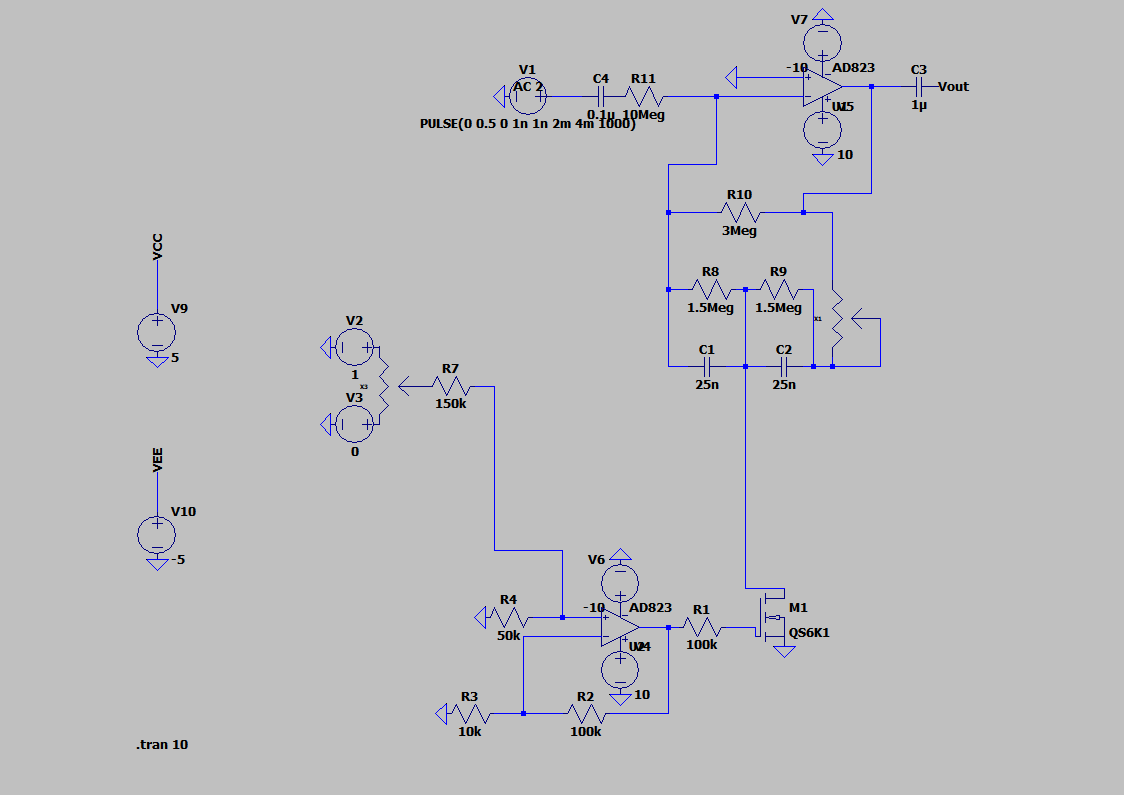
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**Figure. 3-2: Analyzing by replacing jfet with resistor: low cutoff frequency**

****

**Figure. 3-3: Analyzing by replacing jfet with resistor: high cutoff frequency**

By replacing the jfet with an actual resistor, for analysis purpose, the cutoff frequency indeed varied, in a significant way when the resistor value varies (from approximately 20 to 1k). However the relationship is negative, i.e.: when resistor value increases, the cutoff frequency drops. Additionally there’s a high peak at the cutoff frequency indicating resonance.

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**Figure. 3-4: Final VCF design**

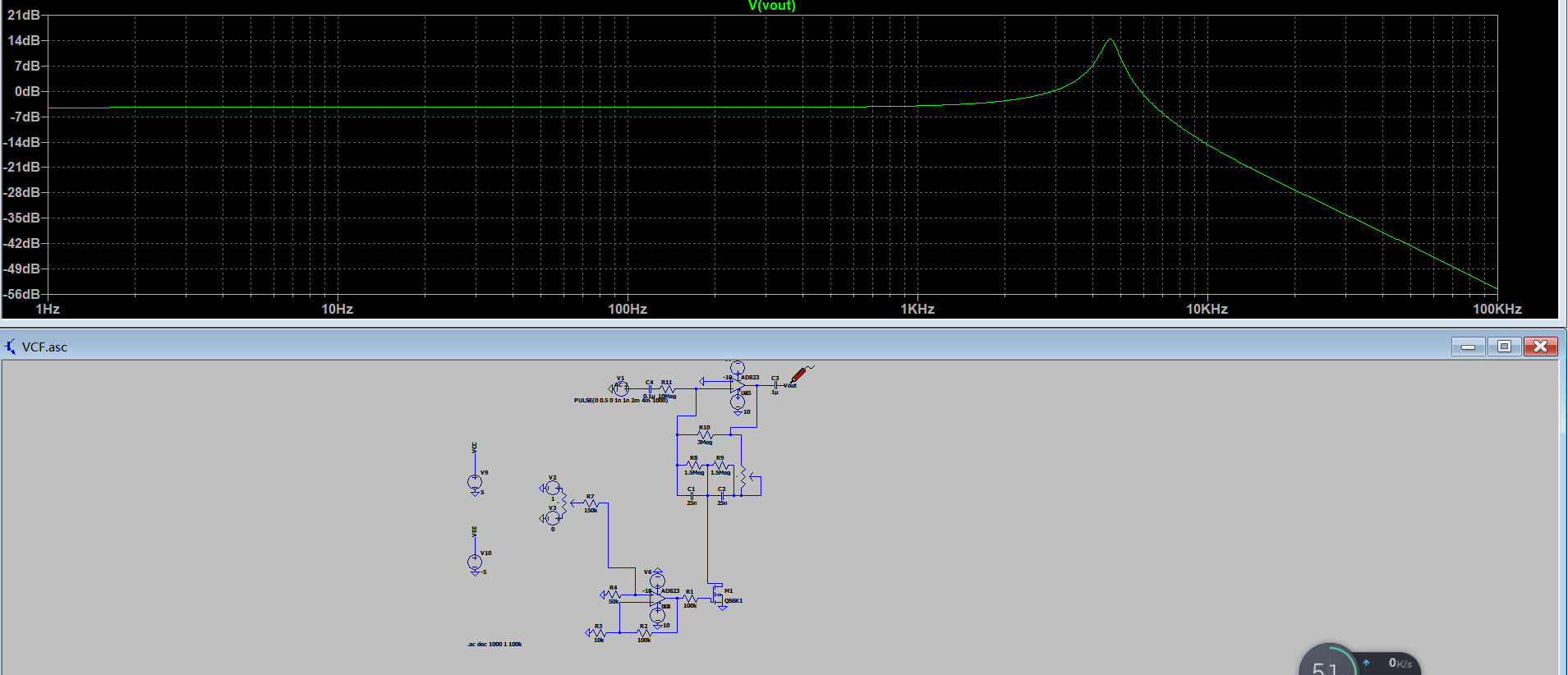
1. **Final design and working principle**

An idea of using mosfet as the voltage controlled resistor came to our mind. It resembles jfet very much and the Vgs is positive. According to lecture notes, when Vds is less than Vgs-Vt, the mosfet is in triode region with almost linear I-V relationship, indicating it to be a perfect voltage controlled resistor with a value of 1/2K(Vgs-Vt) where Vgs is the control voltage.This ensures the positive relationship between control voltage and cutoff frequency as when ramping up Vgs, the "resistance" of mosfet decreases and the cutoff frequency rises. Vgs has to be big (bigger than 0.5 to 1v which is the Vt according to QS6K1 datasheet) so that mosfet is still in triode region. The value of this “varying resistor” is desirable (big enough) for resembling the previous testing resistor since K is small.

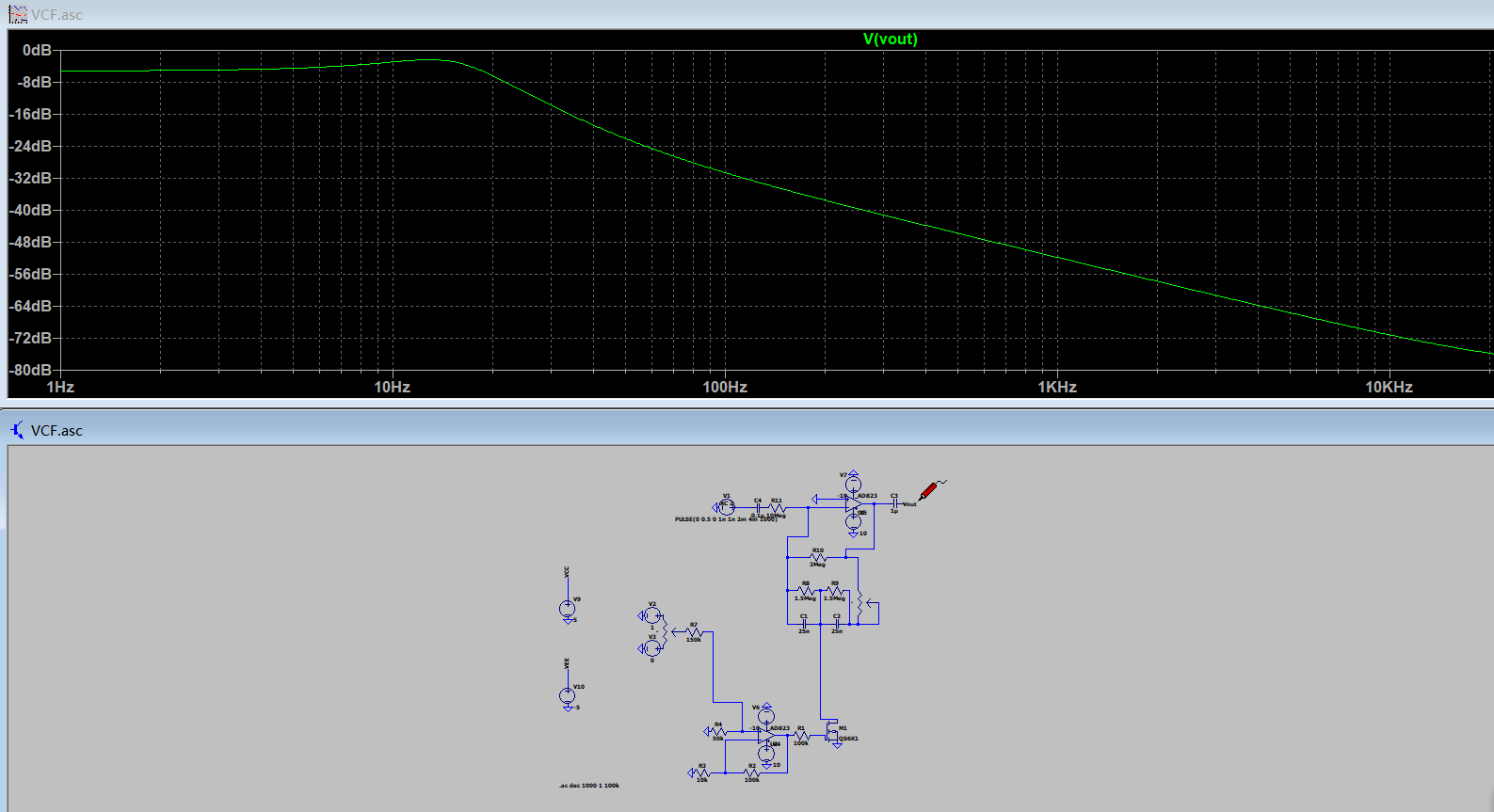
To get a relatively large Vgs, a non-inverting amplifier is used to amplify the DC voltage created by the potentiometer on the left and the 50k and 150k voltage dividers. This amplifier also acts as a buffer to ensure the output voltage is unaffected by other resistances and the mosfet in the circuitry. By adjusting the two capacitor values and the input control voltage values, after some trial and error, the final design of VCF was adapted, as shown in figure 4. The non-inverting amplifier has a gain of 11 so that the voltage at mosfet gate is approximately 1 to 2 volts. The R1 100k resistor is used to prevent the output of non-inverting amplifier being accidentally grounded, potentially ruining the AD823 op-amp and the mosfet. The potentiometer connect to R7 150k is the user control to alter the control voltage thus changing the cutoff frequency. The value of Vd is small shown in the simulation results, due to the large value resistors and 0.3v inverting voltage gain in the filer circuitry, so there was no need to worry about mosfet entering saturation region.

1. **Test results and future work**

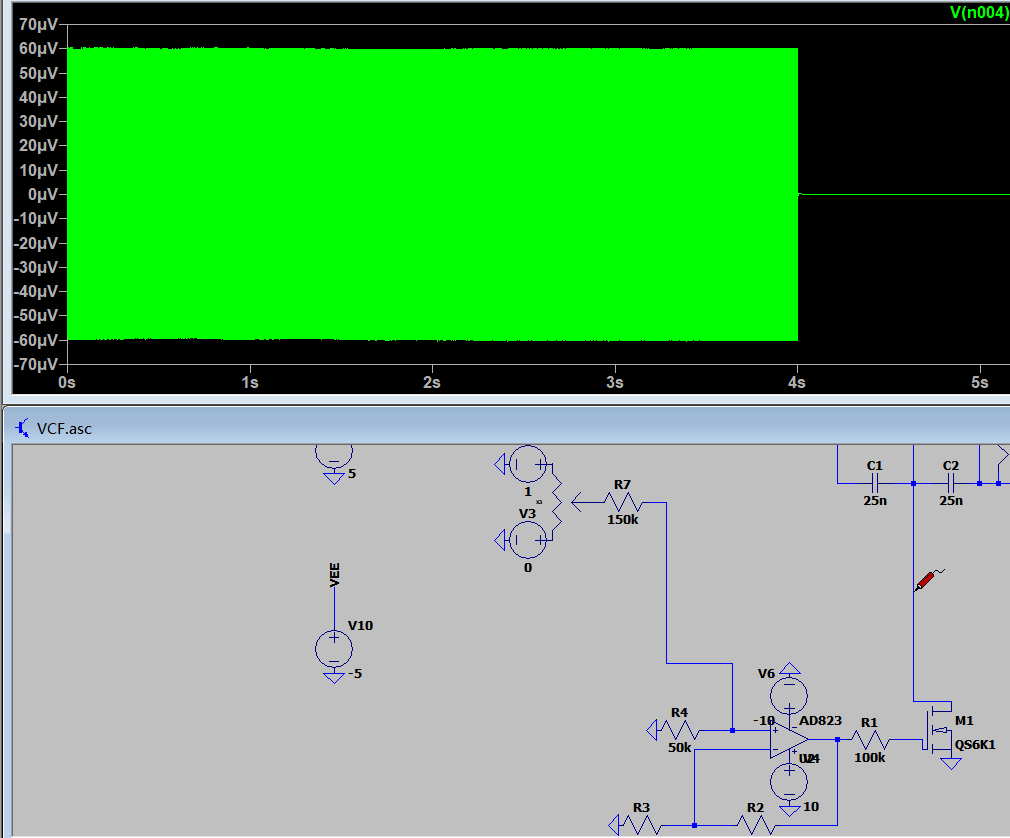
The overall simulation result (the bode plot) of the VCF was quite desirable. As we ramped up and down the cutoff frequency by changing the potentiometer ratio, the cutoff freuqncy, with resonance, changed clearly in the bode plots.

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**Figure. 3-5 high cutoff freq**

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**Figure. 3-6 low cutoff freq**

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**Figure. 3-7 value of Vd of the mosfet is low enough**

Due to the time limit, we did not design a high pass and band pass filter. But we believe that the basic ideas for these two filters are similar to the low pass VCF we designed. IE: the use of voltage controlled resistors, the mosfets, can be adapted to those designs to make their cutoff frequencies controllable by voltages.

Additionally, we did not derive a whole systematic formula or theory to describe the circuitry. In the future, if we have more time, we’ll look at it thoroughly and try to quantize every aspects in it.

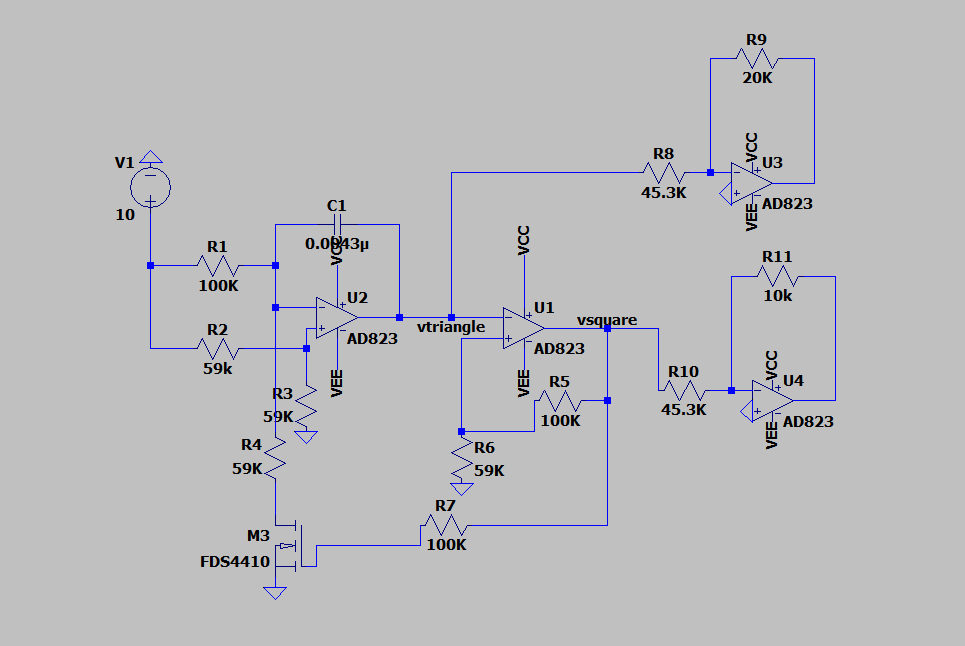
**Low Frequency Oscillator[by Zhaoyu Wu]**

1. **Intro and objectives**

In previous schematic of VCF, the control voltage is set manually. To give the final output even more flexibility, we can also make the voltage vary with time instead of being a constant.

The LFO in our design was used to provide alternating values for the control voltage in VCF. This creates a constant changing sound (usually with a “wawa” effect), since the cutoff frequency set by the VCF is now time-varying rather than being fixed at all time. The LFO is essentially an oscillator. However the signal frequency produced by it is much lower than that by a VCO. Usually the frequency by LFO is around 1 to 30HZ. It cannot be higher as then the sound would be filtered up and down in a very quick way and it will be blurred. The waveform outputted by LFO can be diverse, meaning it can be either a sine wave which provides a very smooth transition of cutoff frequency for VCF (from high to low), or a square wave that produces sharp transition. Additionally, The LFO signal amplitude should not exceed the VCF control voltage swings, i.e. 0 to 1v according to our VCF design.

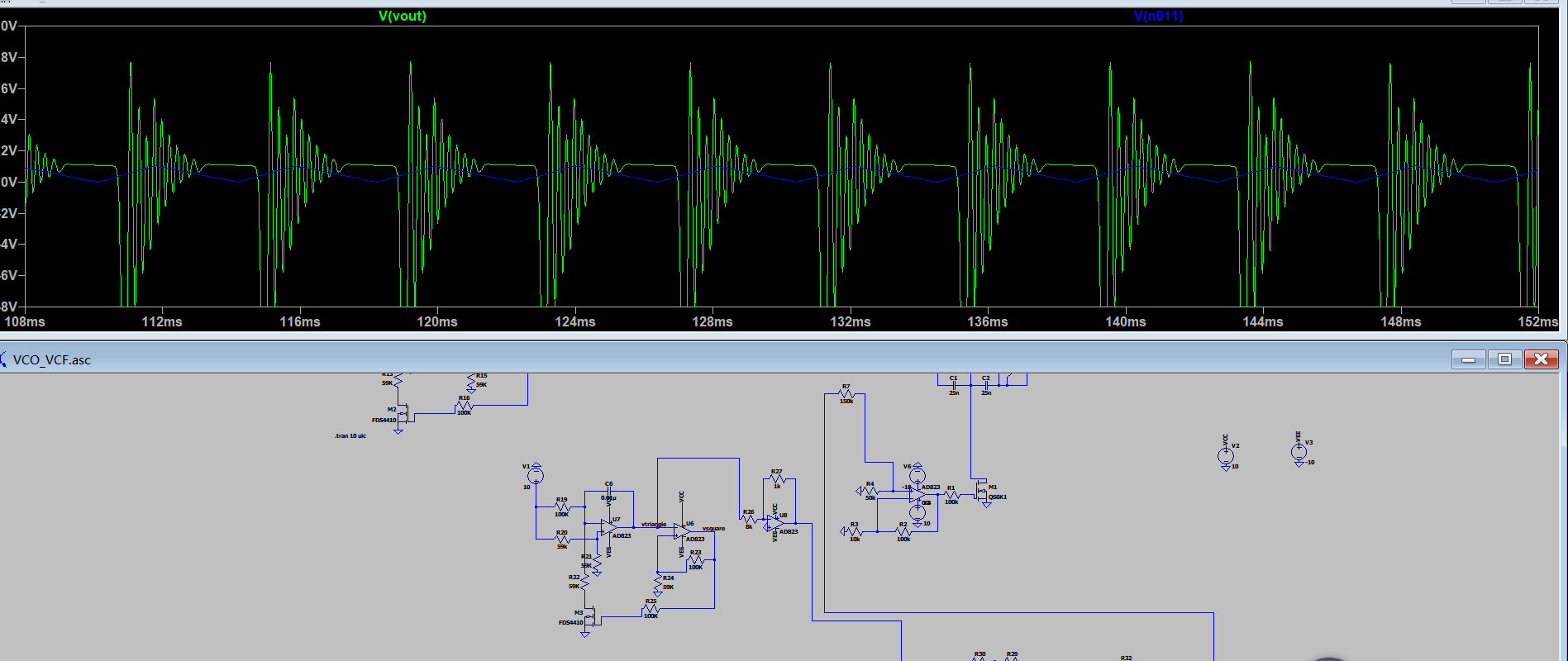
In this design the frequency of the LFO should be user controlled, thus a potentiometer should be adapted.



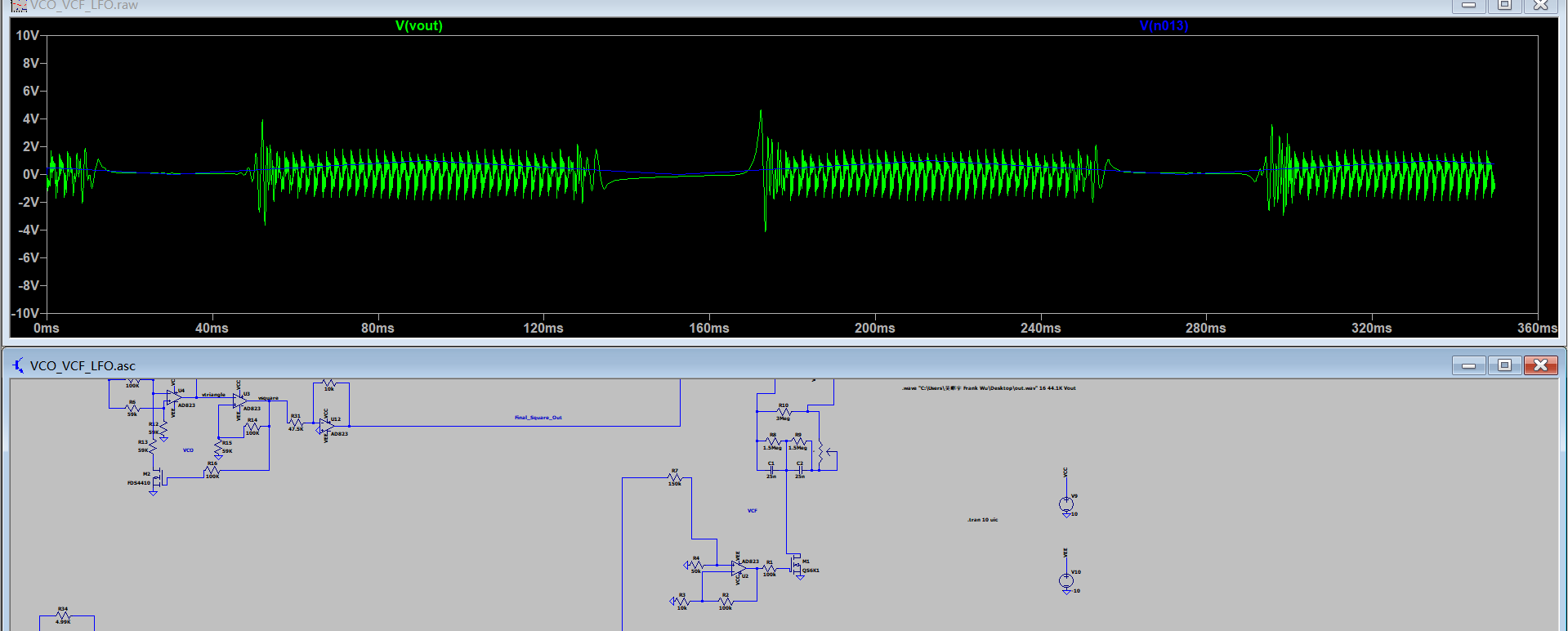
**Figure. 4-1 VCO initially designed to be directly used as LFO**

1. **Initial design**

The first thought was that the VCO previously designed could be transformed into a LFO, by adding a potentiometer at the control terminal of the VCO to provide adjustable voltage. And by adding inverting amplifiers (used to shrink voltage) and offset adders (essentially a summing amplifier), the output with desired frequency and amplitude could be obtained. The LFO designed in this way gave a good result by itself at the beginning, except for a little variation in duty cycles, that is , the square wave, for instance, was not a perfect square wave but with their humps being “squeezed” a little bit. This is due to the capacitor charging and discharging time difference caused by the active input voltage and the resistors (referring to formulae previously derived in VCO design, the rising gradient was (R1-R4)Vin/2CR1R4 and falling gradient was -Vin/2CR1) . This issue was not significant when the oscillator acts as an VCO. However when the LFO was attached to the VCF, and an AC voltage source was used to represent the input signal, the final wave waveform was bizarre, compared to the desired output using a behavioral AC voltage source as the LFO.

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**figure. 4-2 the bizarre output using initial LFO design**

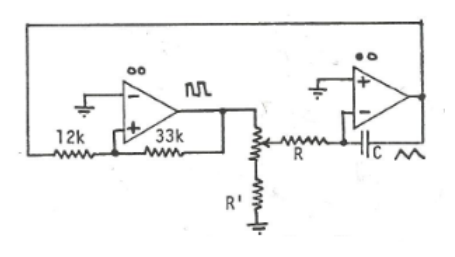
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**Figure. 4-3 the output using a behavioral AC voltage source to simulate LFO**

The reason why this problem occurred was not clear. It might be due to the unbalanced duty cycles or the repetition of similar design of oscillator in the same schematic, which caused subtle problems in simulation. Hence this design of LFO was not adapted, also because this initial VCO design took too long to simulate, adding one more VCO may make the time taken even longer.

1. **Final design and working principle**

Instead, after some research online a similar oscillator design was found. As shown in figure.4. , referring to the schematic provided by Bernie Hutchen (which was cited by Elliott Williams(2014) in his synthesizer project report) . This design was adapted to our final LFO design (shown in figure. 5) and it worked quite well. The principle was similar to VCO: it involves a schmitt trigger and an inverting integrator. The threshold voltage for the schmitt trigger, (or comparator), was set to be grounded (0v).



**Figure. 4-4 “analog Synthesizer Project 6.101- Final Project Report”(Lauren Gresko, Elaine McVay & Elliott Williams)**

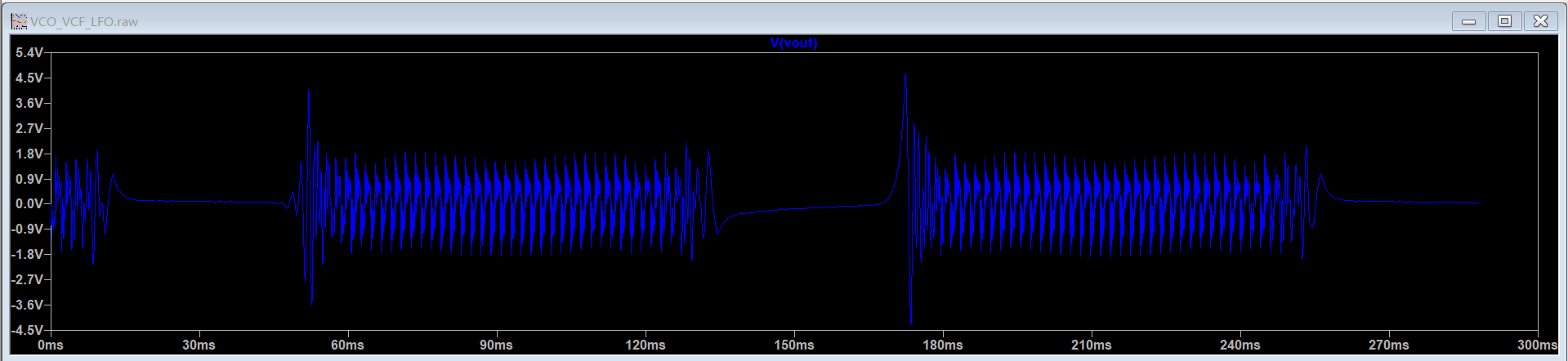
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**Figure. 4-5 final LFO design**

Suppose when the schmitt trigger output was high, in this case, 10v, the inverting integrator uses the 10v value, and values of its resistor and capacitor to form the negative triangle wave slope value, thus the value for triangle wave is decreasing. As it reaches a minimum value that makes the schmitt trigger’s non-inverting input to be less than zero volts, the comparator triggers to -10v, so that the input to the integrator is negative and the triangle slope becomes positive, resulting rise in its value until the comparator triggers again to 10v. The amplitudes of the square are just the two supply voltage of the schmitt trigger as it’s op-amp needs to be saturated to perform the triggering. The amplitude of the triangle wave is determined by the two resistors in the schmitt trigger and its saturation voltages. By performing node method at the non-inverting input of the schmitt trigger, it was discovered that the amplitude is, by formula, ±10/(R49/R48) (referring to Figure.5, the final LFO design). The frequency of the triangle and the square wave is determined (by the slope of the triangle wave, and hence) by the values of the resistor and capacitor of the integrator, with a formula easy to be derived using node method: Vout = -Vin/RC \* t where Vin is ±10 and Vout is the triangle wave. It’s important to note that the slope is negative when Vin is positive, just like the meaning of its name: inverting integrator. By adding a potentiometer as a variable resistor to the integrator input, the user could alter the frequency of the waveforms. Additionally the unbalanced duty cycle issue was solved as the gradients of the triangle wave when it’s rising and falling are the same due to the same absolute value of Vin (10v).

1. **Test results**

When we attached the final LFO schematic to the VCF (here we chose triangle waveform), and after some modification (the LFO output amplitude was reduced to 0.5v using inverting amplifiers, and an offset adder was added to ensure the wave varies between 0v to 1v) the result (VCF output) was quite desirable. The waveform was almost the same as the result outputted by using an ideal AC voltage built LFO. The sound it produced was within our expectations after exporting the .wav file. The “wawa” sound was nice and clear. When the frequency was alter to a very low level by adjusting the potentiometer value, it can be heard that the frequency of the sound changing became obviously lower. To conclude, this was a perfect LFO design.

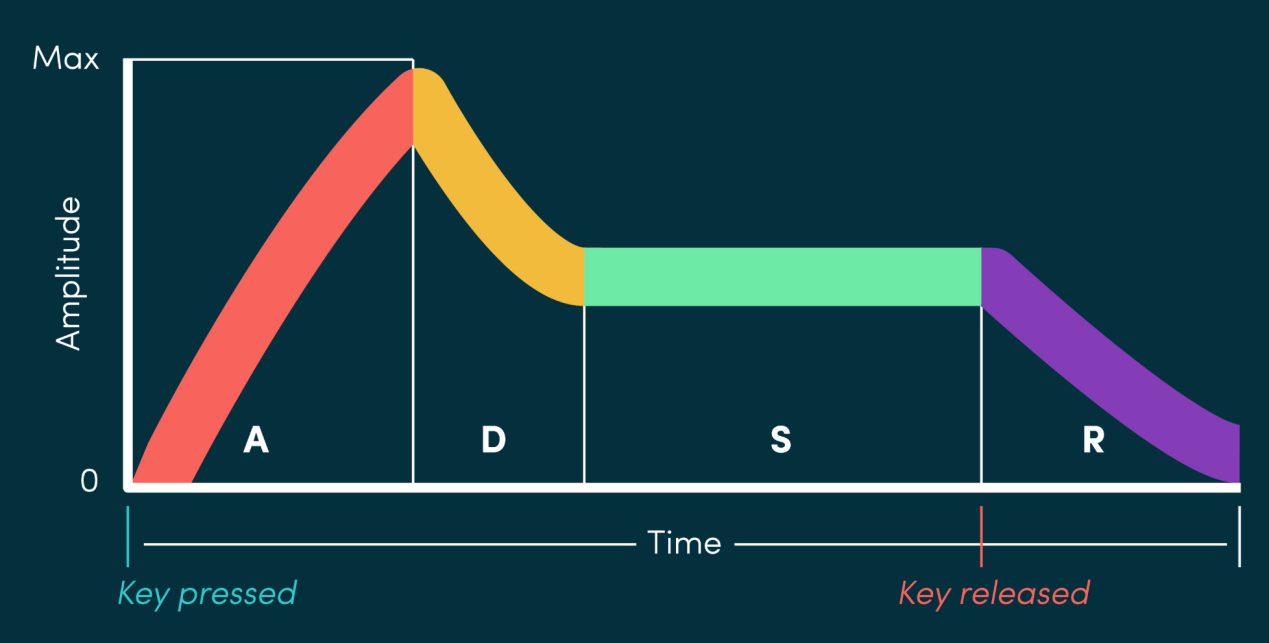
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**Figure. 4-6 the final LFO test result**

**Attack-Decay-Sustain-Release[By Jingyi Liang]**

ADSR is the Attack, Decay, Sustain and Release of a sound (seen in Figure 6-1). Together, they make up the ADSR sound envelope which describes how a sound changes over time. It is triggered by the keyboard. There are four user controllable parameters, so that users can vary the timbre by changing the shape of ADSR.

Attack is the time taken for synthesiser to reach its maximum volume, beginning when the key is pressed. Decay is the time taken for volume to run down from the attack level to sustain level. Sustain is the level during the main sequence of the sound’s duration when key is held. Release is the time taken for volume to decay from sustain level to zero after the key is released. Figure 6-3 shows the schematic of the ADSR module for this project.

****

**Figure 6-1: The ADSR envelope**

1. **Comparator**

The input from keyboard goes through a comparator (seen in Figure 6-2) before entering the ADSR generator. Comparator is powered with a 10V battery. Its V- end is connected to a potential divider, and its V+ end attached directly to the keyboard output. If V+ is greater than V-, the output of the op-amp will jump up to 10V, otherwise it will go down to 0V. Therefore, the trigger voltage goes into ADSR generator is a pulse of about 10V.

1. **ADSR working principle**

When gate signal is off, the base voltage of Q1 is zero, so Q1 is off. The base voltage of Q2 is 0.7V, so Q2 is on. Thus, reset of the 555 timer is held to ground, capacitor C2 is discharged, and the output voltage is zero.

When the gate signal is on, Q1 and Q3 is turned on, and Q2 is switched off. This causes the reset voltage to shot up to V+ (in this case 10V), and the trigger voltage to go down to 0V which cause the output of the 555 timer to go high. The time interval is set up by C2, and the Attack circuit attached to this output end. The Attack circuit consist of limiting resistor R11, potentiometer P1 and Diode D4. The potentiometer P1 controls the rate of charging of C2 which controls the length of the attack period. The decay circuit is not active at the time due to the reversed biased Diode D5. The release branch is connected to the reset, and the reversed biased Diode D3 keep it out of the circuit as well.

When C2 is charging, its voltage level is detected by THRS of 555timer. Once the voltage of C2 is charged up to about 8.6V, the 555timer toggles, it set its output back to ground. This prevents the Attack circuit to charge C2 further, because Diode D4 is in reversed biased state. When the output is set to zero, the DIS pin on 555timer is bought to zero in order to discharge the timing capacitor C2. The sustain circuit is made up of fixed resistor R13, AD823 and potentiometer P3, it attached to the DIS pin. This circuit controls the voltage level and the time interval for sustain. The wiper arm of potentiometer P3 moves from 10V to about 6.8V depending on where the potentiometer P3 is set to. Capacitor C2 has a threshold voltage of 10V, it permits current to flow through forward biased Diode D5, potentiometer P2 and resistor R9. These three components consist the decay circuit, and the decay rate from maximum voltage level to sustain voltage level is determined by the potentiometer P2.

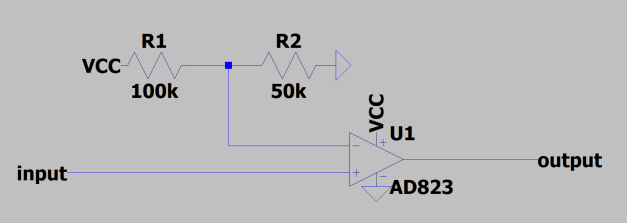
At last, the release circuit is comprised of fixed resistor R10, Diode D3 and potentiometer P4. As the trigger voltage drop back to 0V, C2 begins to discharge to ground at a rate selected by the Release potentiometer P4.

1. **Test result**

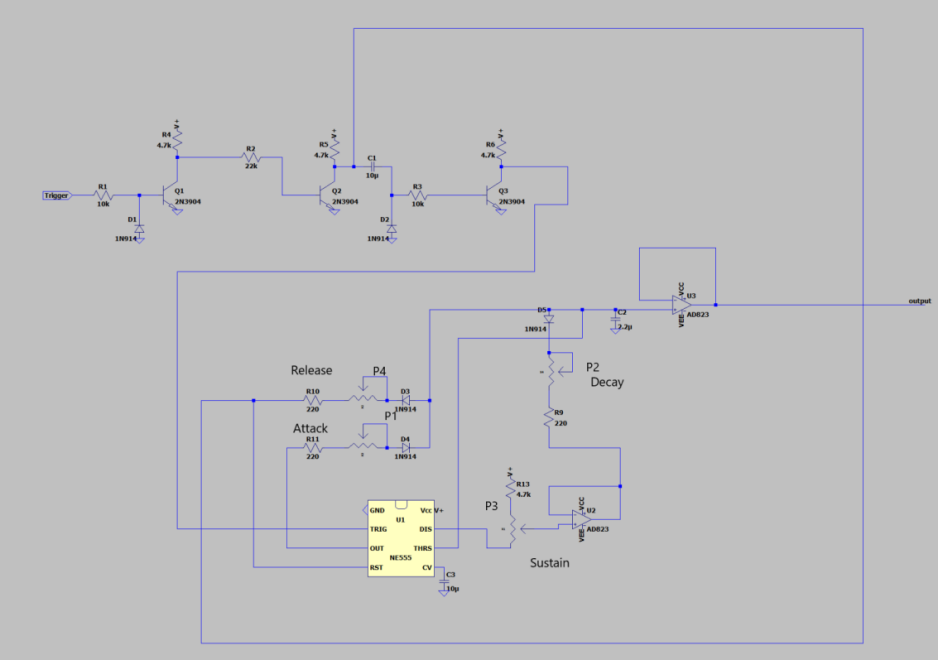
Time constant of capacitor is T=RC, C is fixed (2.2µ). Therefore, the smaller the R, the rate of charge and discharge would be faster. According to graph 6-4, value of P1, P2 and P3 in ADSR1 and ADSR2 are identical, P4 in ADSR1 is smaller than that in ADSR2. The capacitor c2 in ADSR1 discharged much quicker, and this is exactly what we expected. We have done the same test for other three parameters (attack, decay and sustain), and they all match up to what we envisioned.

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**Figure 6-4: simulation result**

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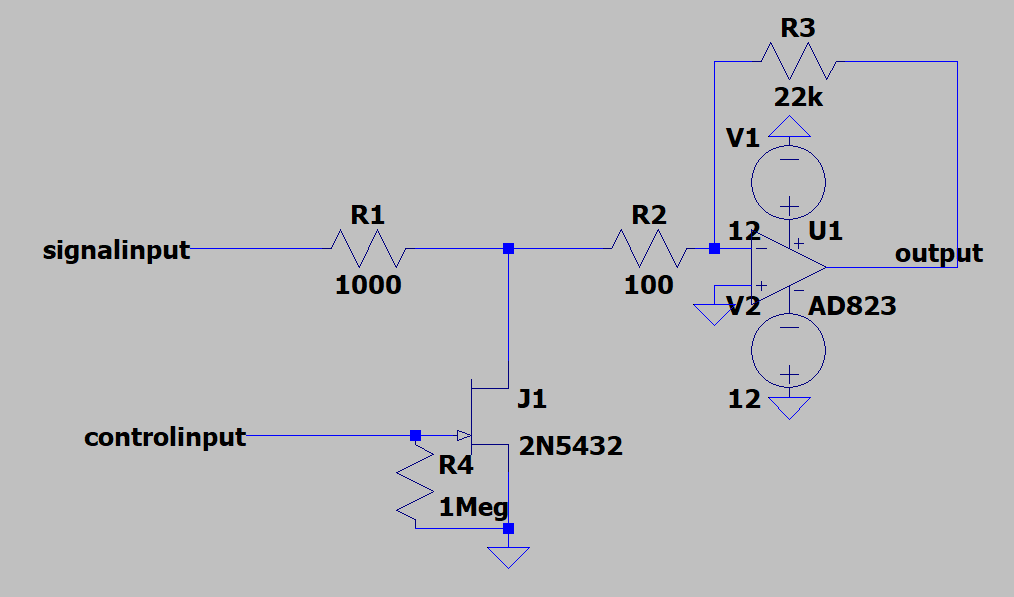
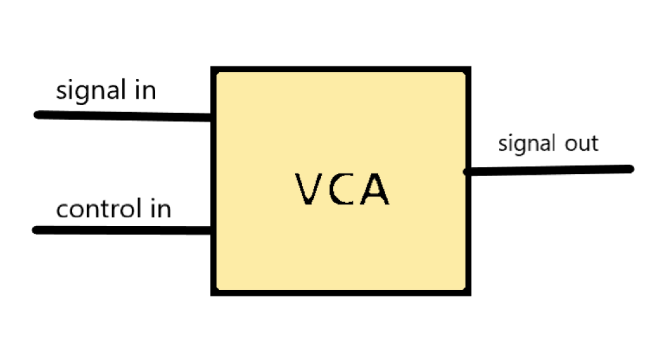
**Figure 6-2: schematic of comparator**

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**Figure 6-3: schematic of ADSR**

**Voltage Controlled Amplifier(analogue multiplier) [By Jingyi Liang]**

VCA stands for voltage controlled amplifier. The output gain of the amplifier can be controlled by an input signal. VCA usually has two inputs and one output (seen in Figure 5-1). Signal input comes from VCF, this is the main signal, and all the changes are made to this signal. Control input comes from ADSR envelope, this is the signal which provide the control voltage that can alter the gain of the amplifier.

****

**Figure 5-1: VCA Figure 5-2: VCA schematic**

1. **Working principles**

The most important component in this block is the N-channel JFET, it can be used as a voltage controlled resistor (VCR) which can adjust the gain of the inverting op-amp circuit. JFET should be operated in triode region in order to get linear relationship. The more on the JFET is (voltage closer to 0), the more signal get attenuated, and the lower the gain is. The more off the JFET is (voltage away from 0), the more signal gets through, and so it has a higher gain. The signal will go into the op-amp after coming out from JFET.

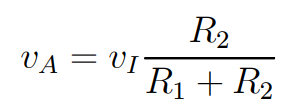
1. **JFET parameters:**

β -> transconductance parameter Vto -> threshold voltage (which is negative)

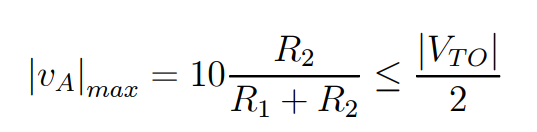
JFET drain current:

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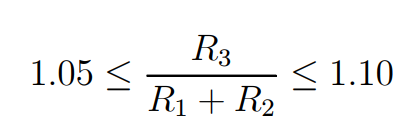
JFETsource-drain voltage:

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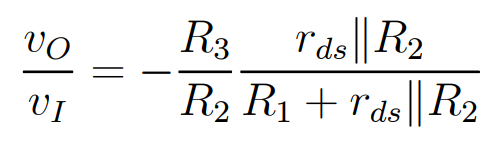
For JFET to be operated in triode region, the source-drain voltage should be smaller than threshold voltage. Therefore, the limit is taken at half the threshold voltage to ensure source-drain voltage stays in the safe range.



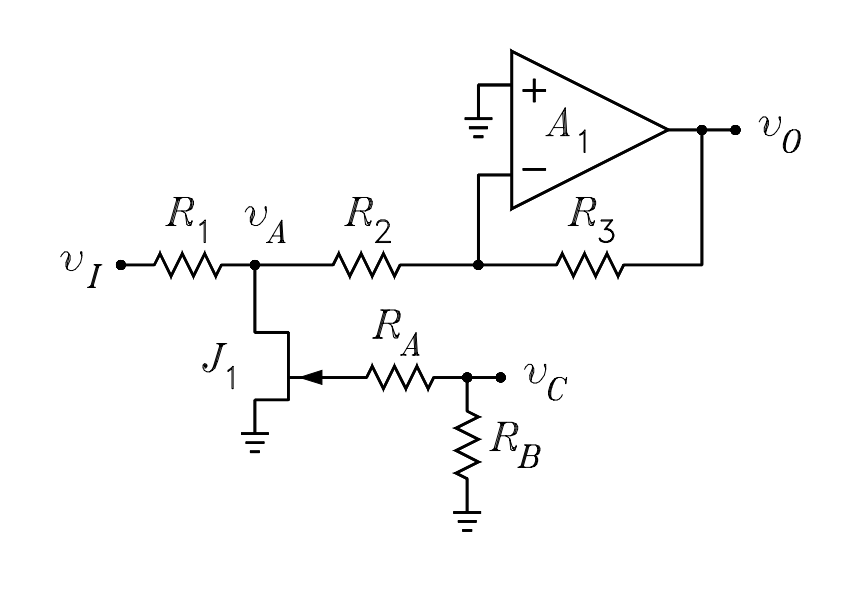
**When JFET enters cut-off region**, it is an infinite resistance, the circuit is to be designed so that it has a voltage gain that is 5% to 10% greater than unity (in the range of 1.05 to 1.10).



**When JFET is in triode region**, the gain of the circuit is:



Rds is the resistance from drain to source. When Rds is minimum, the attenuation is 26 dB (a linear factor of 1/20) lower than the gain when the JFET enters cut-off region.

****

**Figure 5-3: VCA circuit**

1. **Our design**

VCA schematic can be seen in Figure 5-2. 2N5432 JFET has gate source cut-off voltage from -4V to -10V, so its threshold voltage is -4V (seen in Figure 5-6).

Unity -> R3/(R1+R2) = 20

Minimum -> 1.1\*20/20=1.1

Theoretically, gain of the circuit can be varied between 20 and 1.1 over the range -4 ≤ control in ≤ 0.

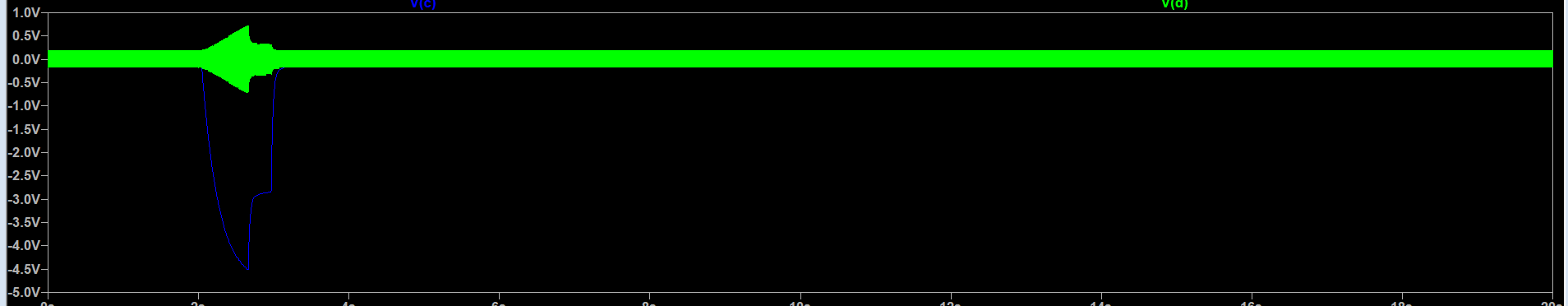
In reality, the JFET has noticeable change in gain from 0V to -6V, corresponding to gain from 2.38 to 20. The maximum gain can be increased by adjusting R1, R2 and R3, however the minimum gain can never drop to 0. (This is main issue)

1. **Main issue:**

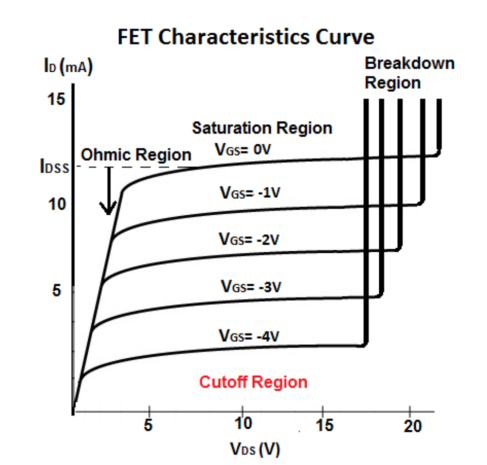
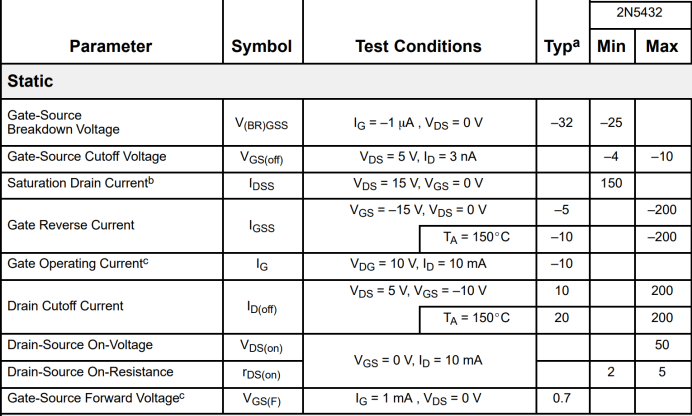
When ADSR envelope reaches 0V, the gain of the VCA is still quite large (about 2.38). Therefore, the background noise is really loud. It is not able possible to eliminate the background noise by setting dc offset to ADSR. When outputting the waveform as a .wave file, the note can be barely distinguished from the background noise although it has higher volume (seen in Figure 5-4).

* **N-channel JFET has other disadvantages:**

1. Firstly, it has linearly relationship only for small values of source-drain voltage, non-linear relationship appears as source-drain voltage approach the cut-off point (seen in Figure 5-5). Therefore, the control input from ADSR (originally 0-10V) need to be made smaller before putting into VCA.
2. Secondly, the more negative the voltage is, the higher the gain. Thus, the shape of ADSR need to be inverted using inverting amplifier or use a P-channel JFET instead.
3. Finally, the relationship between resistance to source-drain voltage is reciprocal.

****

**Figure 5-4: output waveform of ADSR and VCA**

** **

**Figure 5-5: FET Characteristics Curve Figure 5-6: 2N5432 datasheet**

**Analogue multiplier**

A better substitution to VCA is an analogue multiplier. In our design, we use AD633(seen in Figure 5-8). The output from ADSR goes through a potential divider (seen in Figure 5-7) to set its offset to zero volt, because the offset was originally at 44mV. Then, ADSR goes into the X1 input of the AD633. The main signal created by VCO passed through VCF and LFO, and finally goes into the Y1 input of the AD633. X2 input and Y2 input are both grounded, so that the product of X1 and Y1 is obtained. After that, the product is divided by 10. In the end, the value adds Z to give the output W. Z is set to zero, so the final output is (X1\*Y1)/10.

1. **Our design**

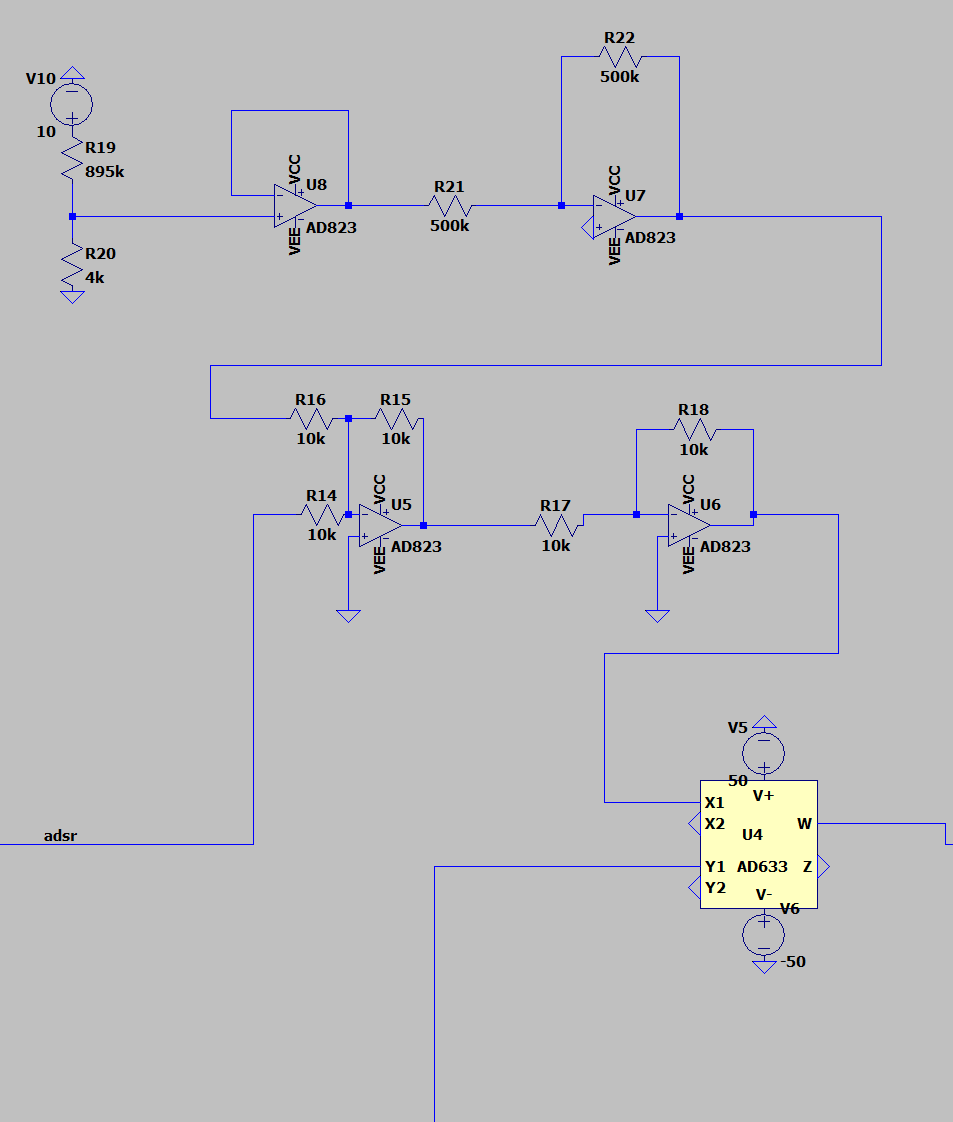
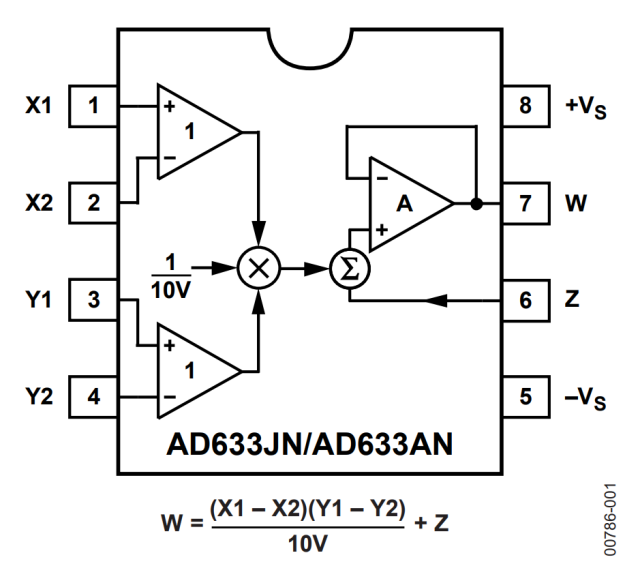
We import the CIR file of AD633 analogue multiplier into LTspice, and created a symbol for it. In order to set the offset of ADSR to zero, we wanted to make used of the Z value by letting it equal to negative 44mV using a voltage source. This can be achieved perfectly in LTspice. However, in reality, voltage source can not provide such a small voltage. It is a reference voltage, not a voltage supply.

* **Solution**

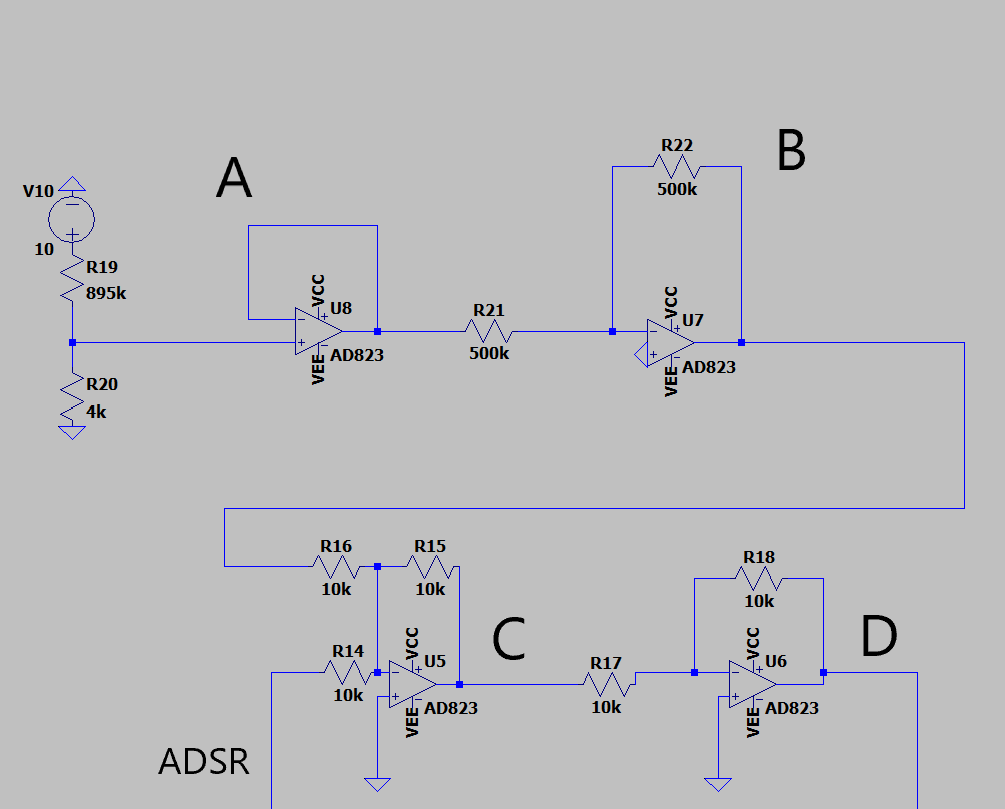
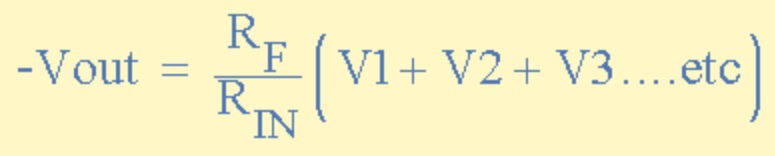
A potential divider and summing amplifier can be used to solve this problem (seen in Figure 5-9). The potential divider provides a voltage of 44mV, but there is hardly any current goes into amplifier A. Amplifier A is a voltage follower, this gives an efficient isolation of next stage from the potential divider. Then, 44mV enters amplifier B which is an inverting amplifier with the voltage gain of -1, so the output voltage is -44mV. Amplifier C is an inverting summing amplifier, current through each branch is isolated from each other. The equation can be seen in Figure 5-10. This adds up the ADSR value and -44mV, gives a voltage of –(ADSR-44mV). Finally, the voltage is inverted by an inverting amplifier D which turns it into the desired value (ADSR-44mV), and the offset of the ADSR envelope is approximately 0.

1. **Final result**

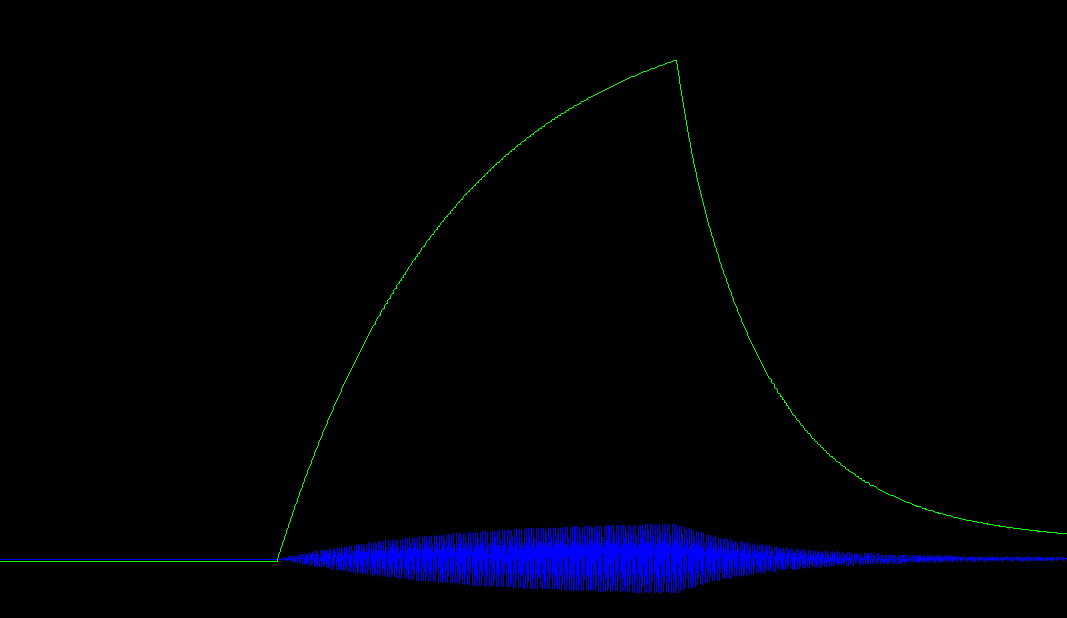
There is a great improvement, the AD633 amplifier eliminates the background noise as much as possible, so that we can hear the main notes clearly (seen in Figure 5-11).

** **

**Figure 5-7: schematic of analogue multiplier Figure 5-8: AD633**

** **

**Figure 5-9: schematic of potential divider Figure 5-10: inverting summing amplifier equation**

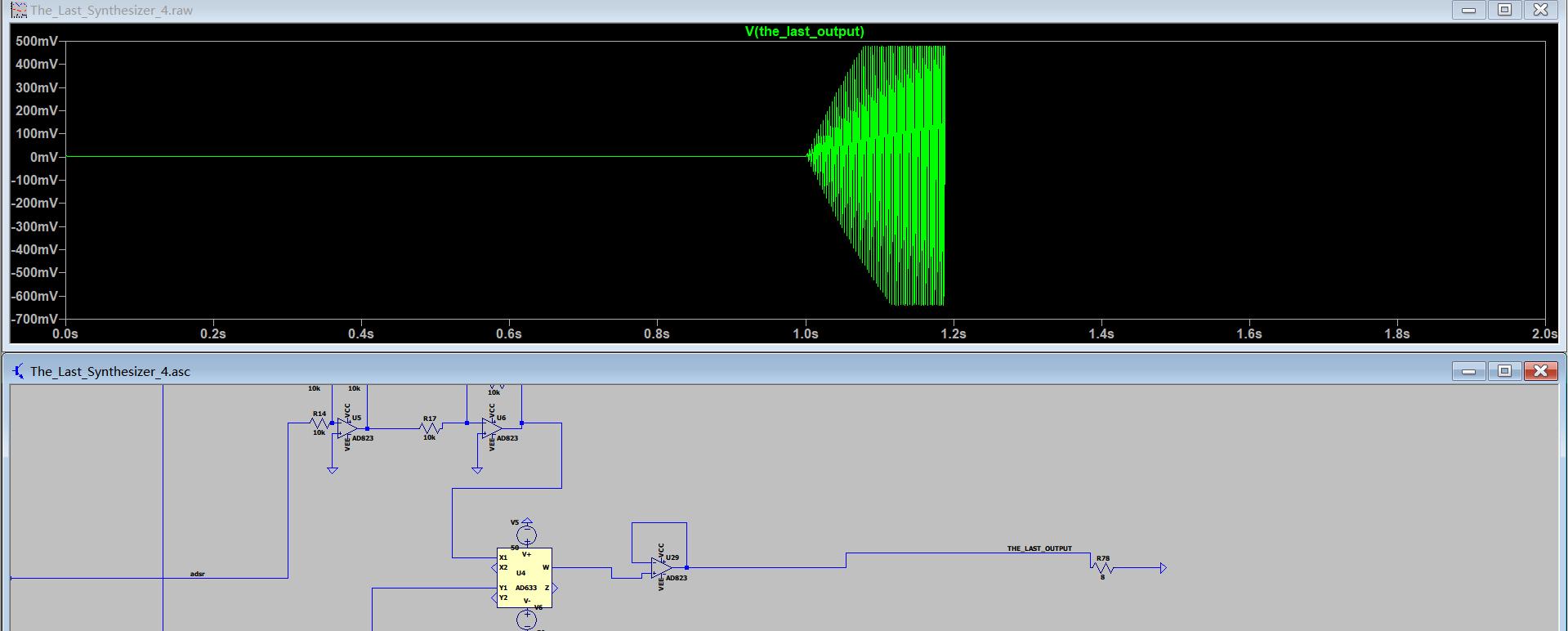
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**Figure 5-11: Final test result**

**Output Stage(class AB power amplifier) [by Zhaoyu Wu]**

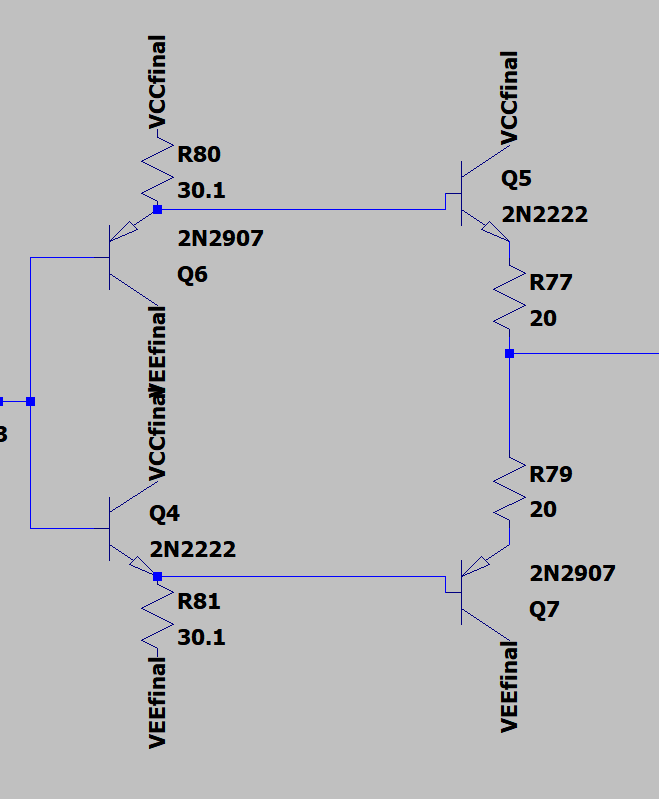
The output stage of the synthesizer is a class AB power amplifier directly adapted form college lecture notes. It’s used to amplify the power/current outputted from the analog multiplier (i.e. the sound processing stage).

The synthesizer is required to drive an 8 ohm microphone. If the voltage comes out from the sound processing stage is directly applied onto the speaker, distortion will occur (figure. 1) at some large voltages, since the speaker resistance is too small to be allocated with sufficient voltage (the speaker, compared to the output impedance, could be considered almost as the ground). Thus the current supplied by previous stage could be amplified in the load stage so that Rload can have larger voltage and power, reducing distortion.

****

**Figure. 1 Distortion: you can see the clipping when voltage is high**

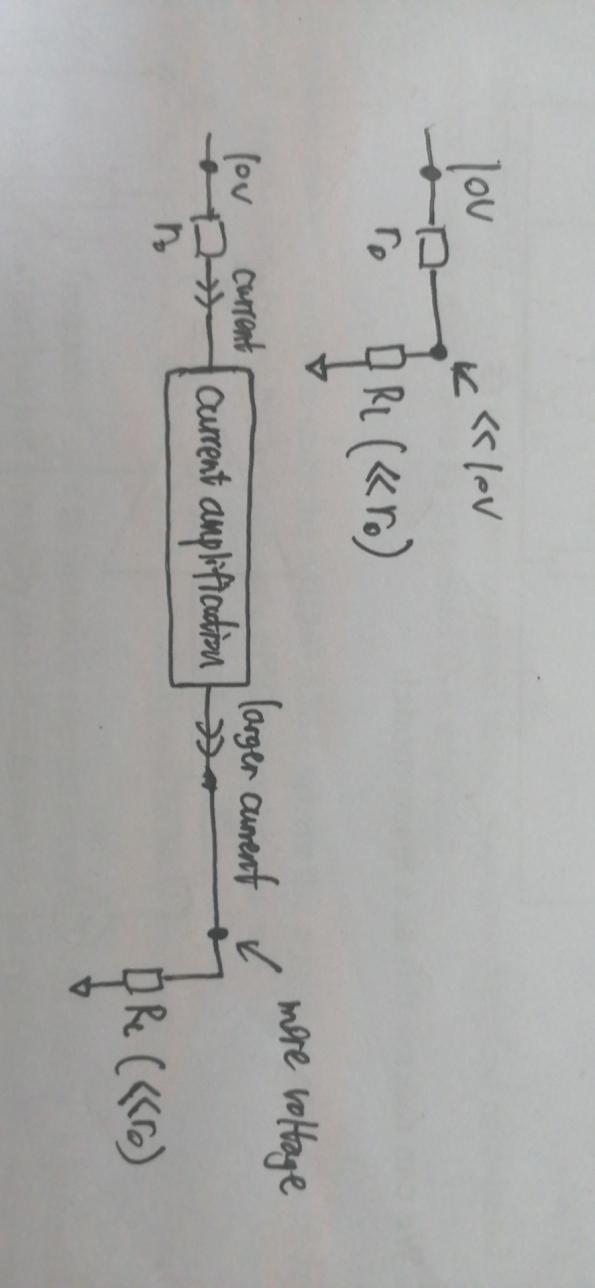
The schematic of the class AB design is shown in figure. 2. it’s exactly same as the college note design. The resistor values are kept small and supply voltage kept big (abs. 50v) in order to make the output current that can be supplied as high as possible. The choice of these values conform to the formula given in lecture notes. (figure. 3)

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**Figure. 2 the class AB schematic**

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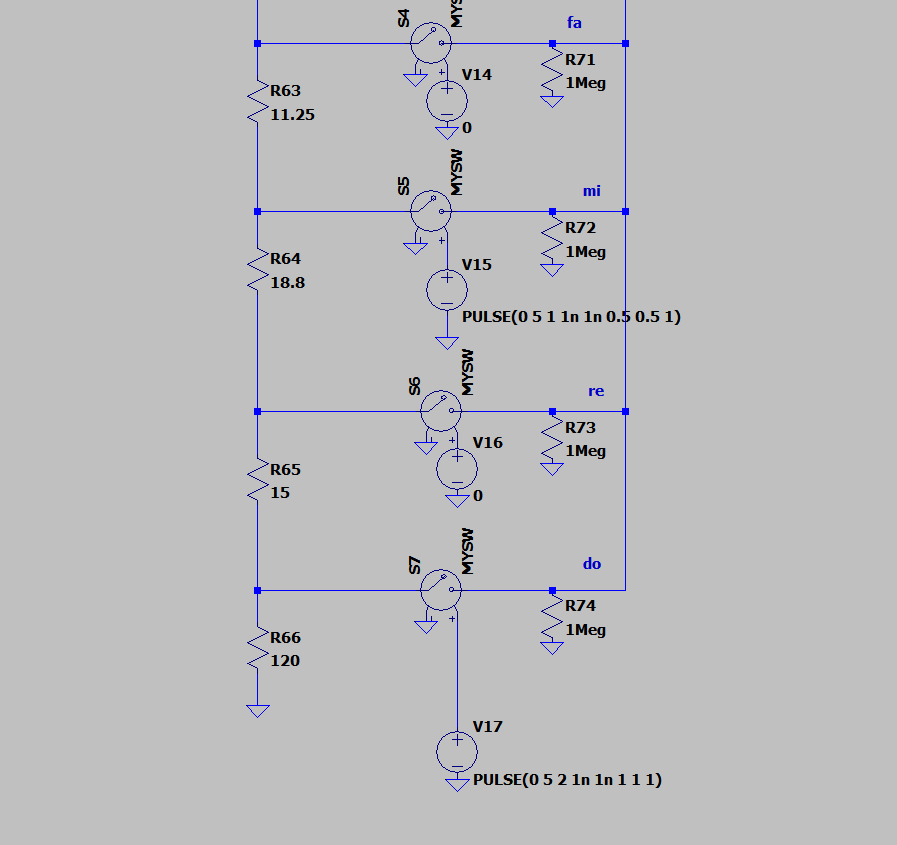
**Figure. 3 the formula in lecture note**

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**Figure. 4 brief illustration**

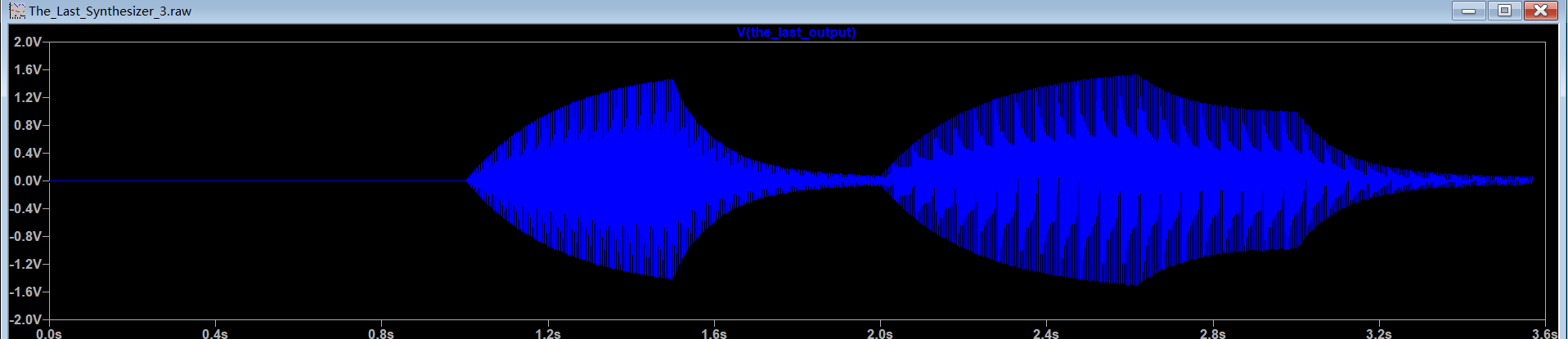
**Sample and Hold Circuit [By Zhaoyu Wu]**

1. **An unexpected error**

****

**Figure.1 Two keys pressed shown on keyboard**

The design of the sample and hold circuitry was unexpected. As we connected everything together, and set two square waves one after another representing note Mi played (key Mi pressed) first (in a short time period) then Do (key Do pressed)(in a longer time period). We expected to see a nice shaped waveform shown in figure.2.

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**Figure. 2 Waveform expected to see**

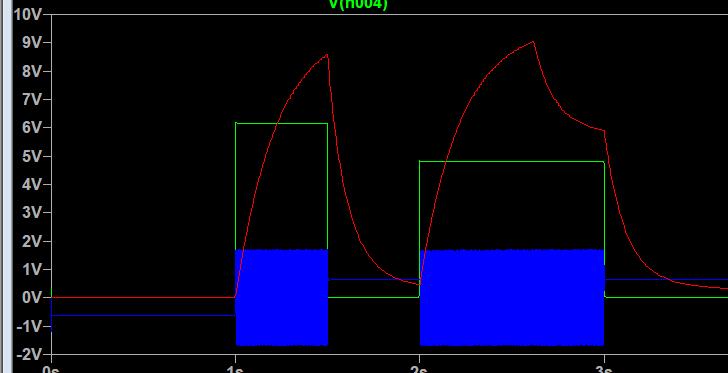
However, a weired thing happened that the waveform disappeared during ADSR’s release period.

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**Figure. 3 the wrong waveform**

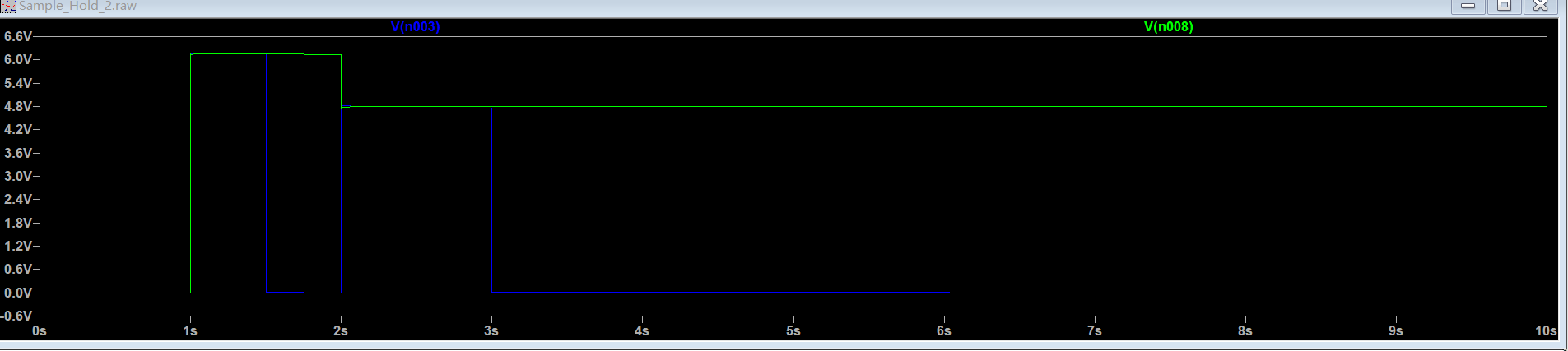
1. **The reason for the glitch**

After some debugging, we discovered the reason for this glitch. When a user presses down a key, a fixed value DC voltage is created. The user holds the key for some time and the value remain at that level. After the user releases the key, the DC voltage drops to 0. Thus one square wave element (only one cycle) with length determined by how long the user pressed down the key and its peak is the fixed DC value. A problem is that we cannot directly input this to the VCO (as the control voltage), because that would make VCO output a waveform (sine,square,triangle etc.) with it time length exactly the same as the time the user pressed down the key. I.e.: after the user released the key, the input to VCO would 0 and VCO's output would be a straight line (with value normally 0)(depends on the specific design of VCO). Here we inputted two square pulses as a simulation of user pressing down two keys over time (with a 0v interval to represent the time after the user releasing the first key and before pressing down the next key), and the alternating waveforms outputted by the VCO lasted for the same period of time as the “on” state of the square pulses.

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**Figure. 4 the waveforms for debugging**

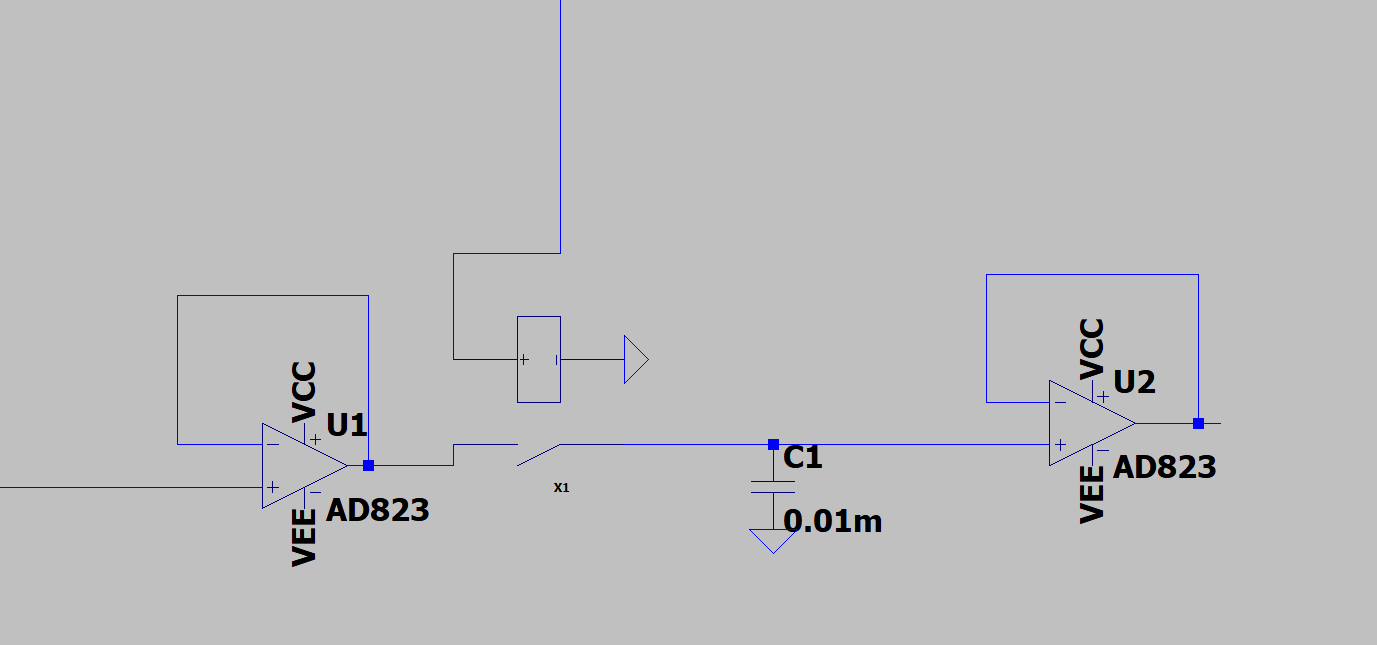
Now if the envelope from ADSR is multiplied by the VCO output, the release stage (ADSR) of the final output would not be an alternating curve but a straight line, since zero times any value is 0, then there's no sound in release stage ( but this violates the aim and criteria for building an ADSR ). This is because the ADSR release stage envelope is generated after the key is released, rather than during the user holding the key. So VCO should also be outputting waveform after user releases the key. That is, the sound should last forever even if the user releases the key. There should be no 0v intervals between these two square pulses. The first pulse should extend to the time at which the next pulse rises (figure. 5).

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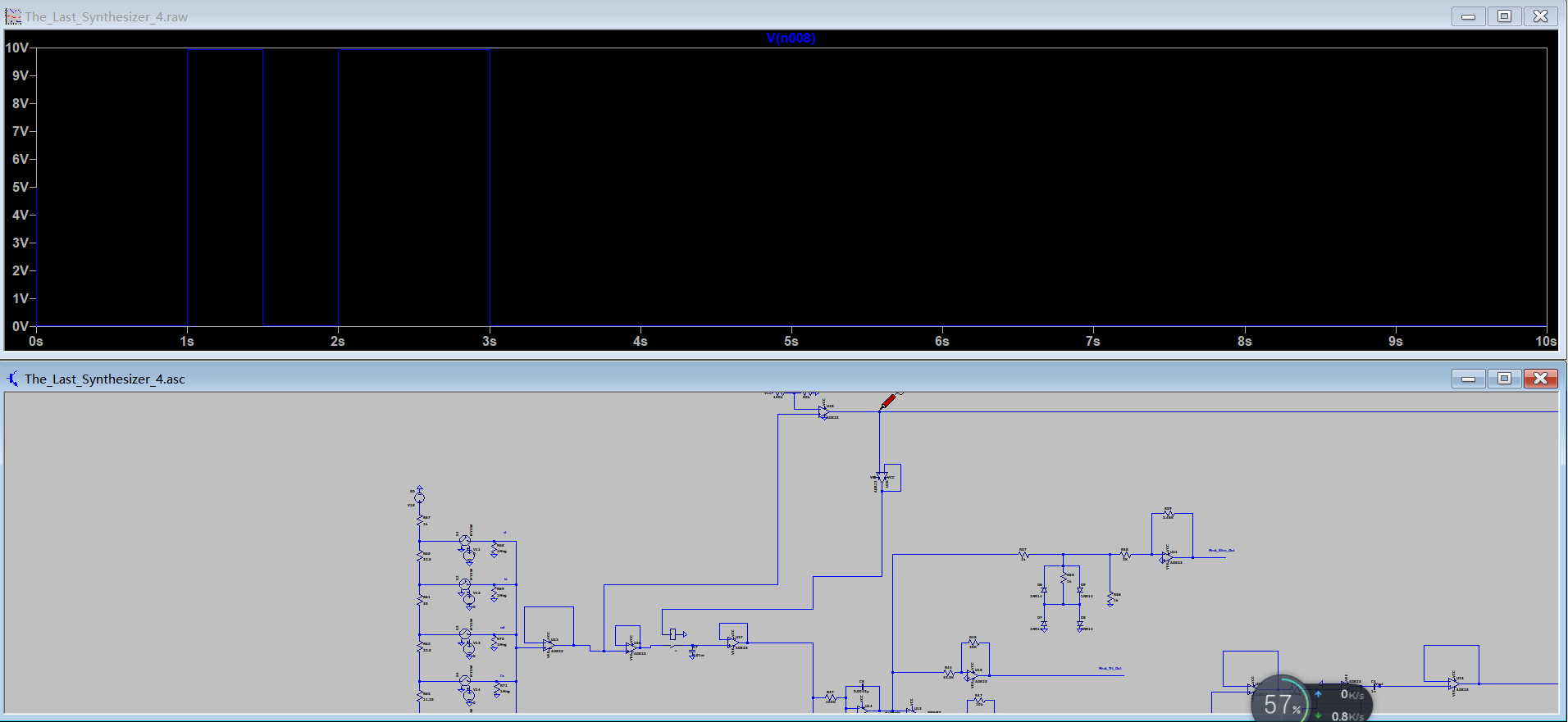
**Figure. 5 the correct input signals**

1. **The solution: Sample and Hold circuit**

The solution to this issue was incredibly simple. By introducing the sample and hold circuitry the value of the pulse could be first sampled during the pulse high time, then be held at that value during the pulse low time. The schematic just consists of a relay (which is regarded as a voltage controlled switch) and a capacitor (figure. 6), and two buffers to ensure the adjacent two stages won’t affect this circuitry. The relay’s control input was attached to the trigger input connected to ADSR, the trigger signal was just another version of the two pulses in our case but with same value of high voltage level. (see figure. 7) The trigger signal acts as the clock of the sample and hold circuitry.

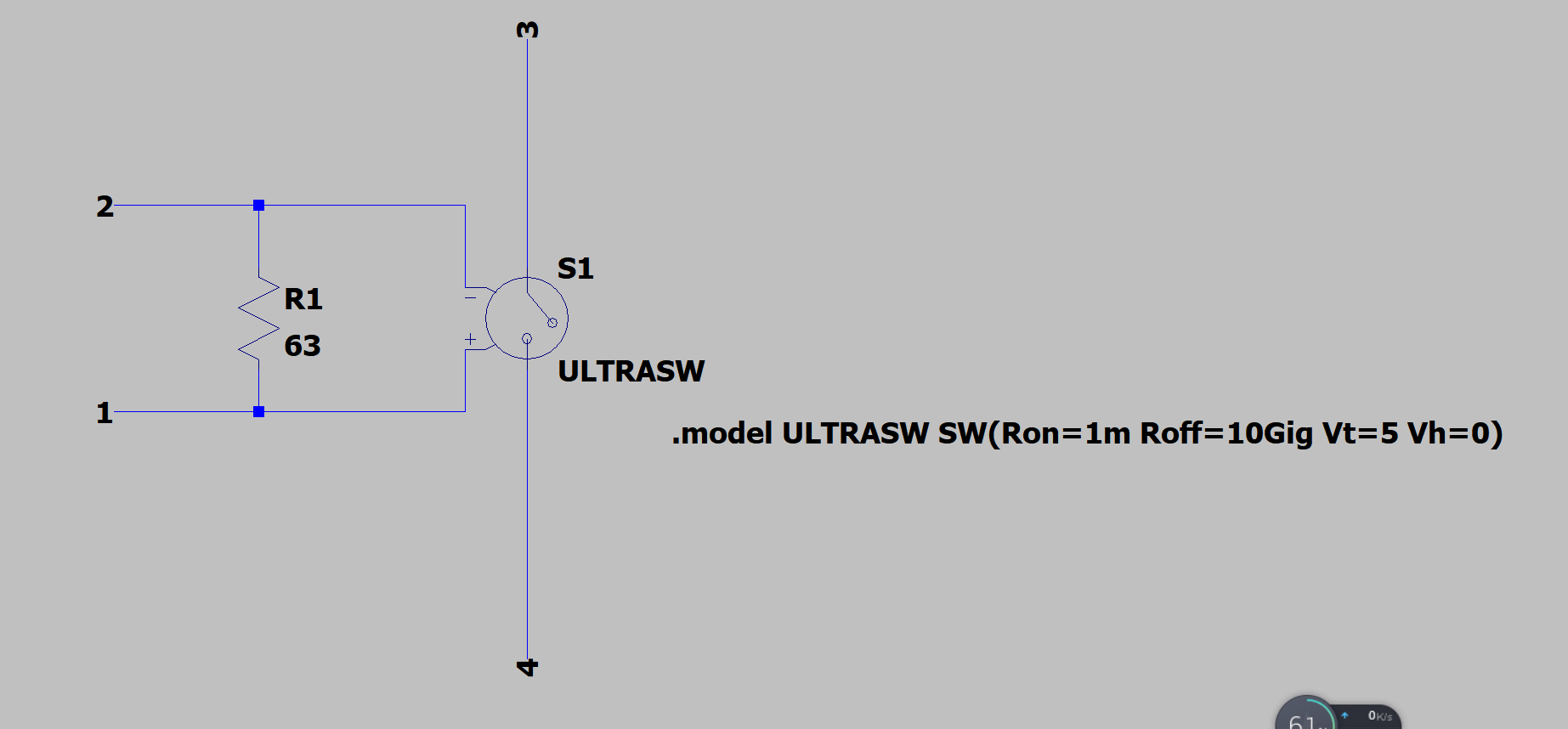
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**Figure. 6 the sample and hold circuitry**

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**Figure. 7 the clock signal into the relay’s control input**

When the first input pulse rises, the clock is high, the relay (switch) closes, and the capacitor is quickly charged to a voltage level same as the input pulse level-high voltage. When the first input pulse drop to 0, the relay is switched off, and the capacitor’s voltage remains at initial level since it has charges. So the voltage outputted during the input-pulse-low time is same as that during the initial input-pulse-high time, the voltage is retained until the next input pulse comes in. The relay is switched on again and capacitor is charged (in this case, discharge. Anyway the capacitor voltage level should be the same as the pulse-high voltage level) and the same process repeats. The relay is modeled using a voltage controlled switch and a resistor based on a real relay G5LE. It has 63 ohm coil resistance and 5v switching voltage. (Figure. 8)

****

**Figure. 8 the relay model**

1. **Test results**

The test result was just the same as figure. 5 that we’d predicted. And the result for the whole schematic was the same as figure. 2

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**Figure. 9 the test result of input signal after adding sample and hold circuit.**

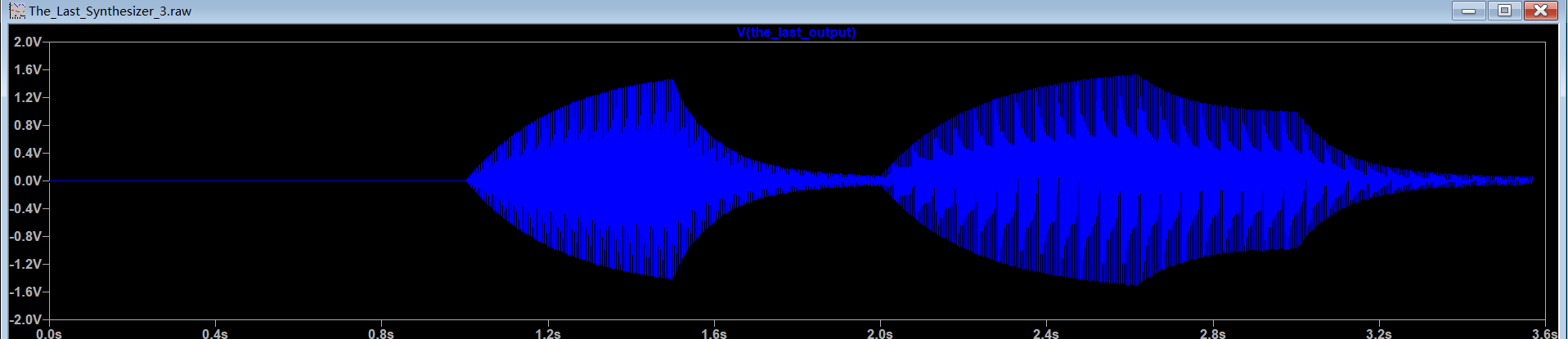
**Final Test Results**

1. **Final test results, conclusion and future expectation**

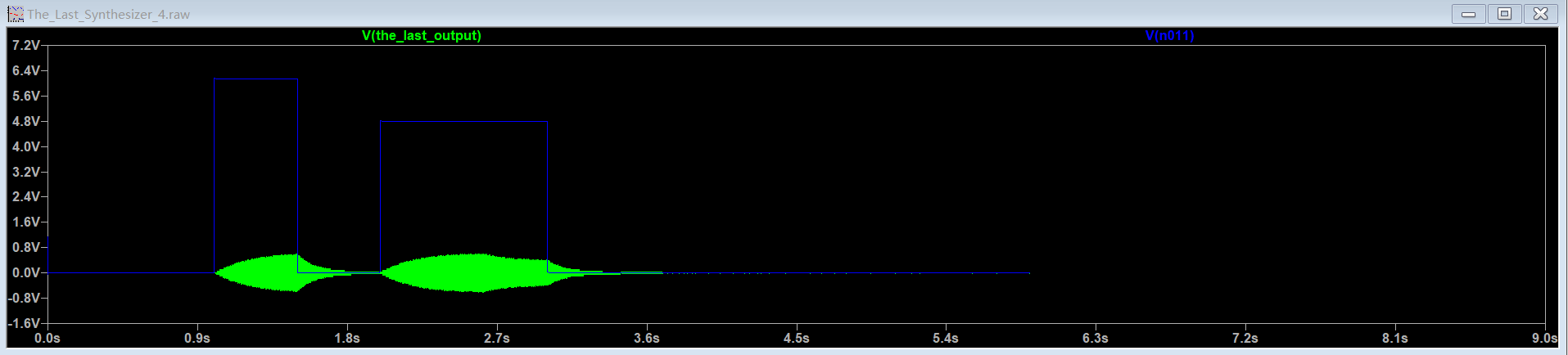
The synthesizer proved to be quite successful with all of the modules connected together (figure. 4). We performed the previous test by making the synthesizer play the first Mi note then Do note with a certain time interval. The final waveform remained undistorted and was within our expectation, and the sound outputted as .wav file was clear. The waveform shown as below. (figure. 1 & 2)

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**Figure. 1 the input signal from keyboard representing 2 keys pressed one after another**

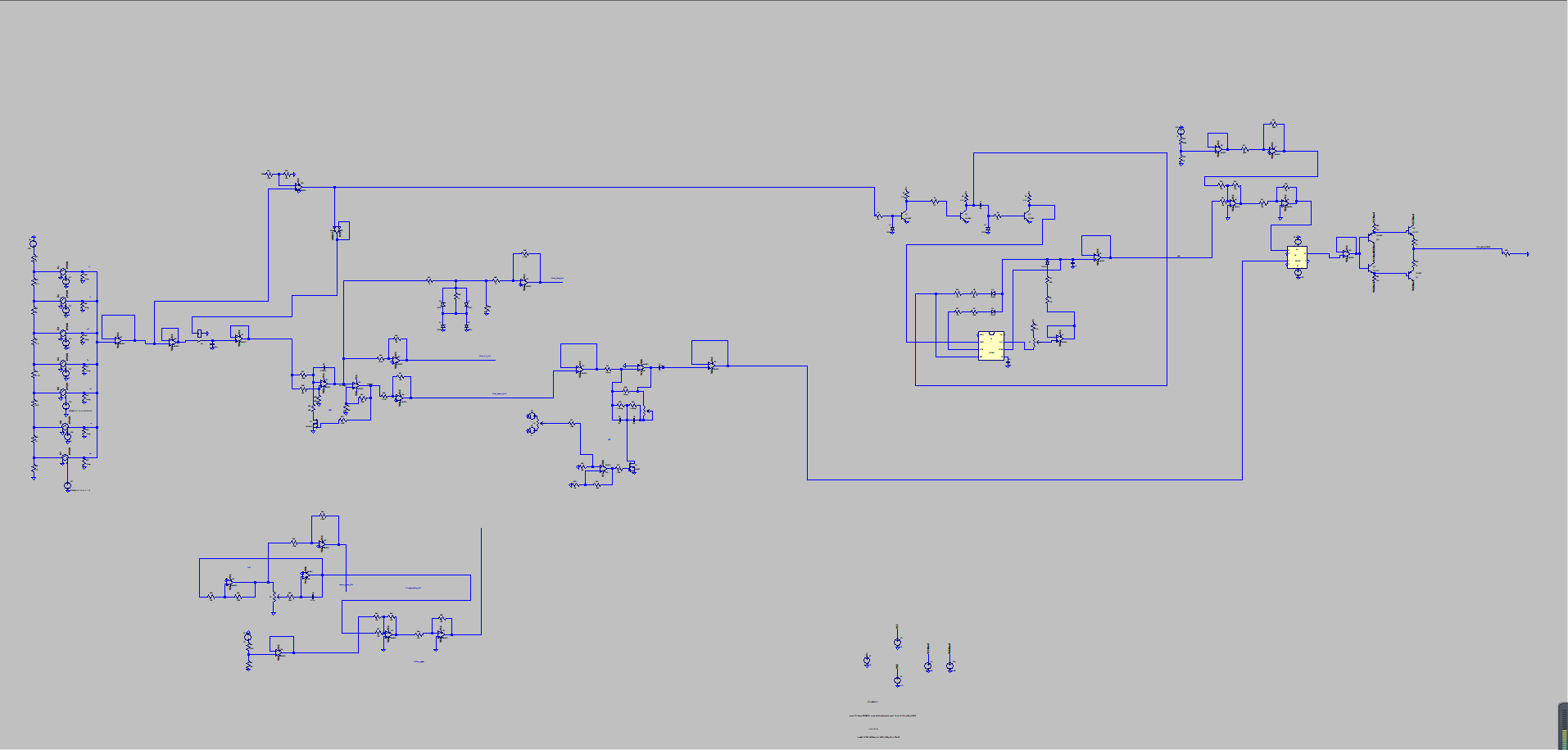
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**Figure. 2 the final waveform**

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**Figure. 3 combined showcase**

To conclude, our ELEC40006 synthesizer design went smoothly and the final result is generally satisfying. There' re certainly some trivial problems with this design. For instance, the ADSR envelope cannot go exactly to 0 (but very close) after the user releases the key for a long time, resulting small sounds could still be heard when listening to it very carefully. Due to the time limit, we did not fix these minor problems. Perhaps in the future our design could be improved by adding Arpeggiator and even more LFOs to give our synthesizer more features. Finally, many thanks to the instructors who helped with our design on pizza and through Teams consultation.

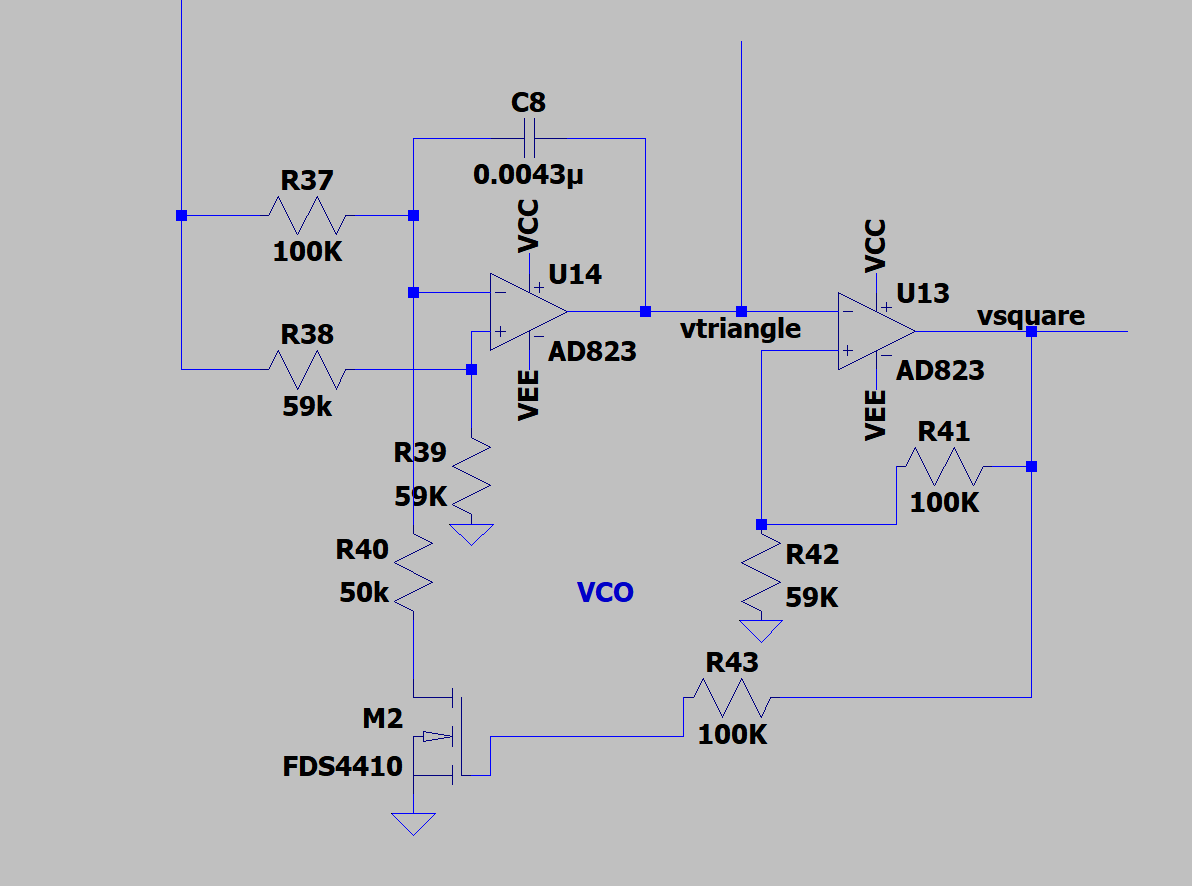
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**Figure. 4 total schematic**

**Tolerance estimation [By Zhaoyu Wu]**

Tolerance estimation is important as this would affect the actual product manufacture. If some resistances are a bit higher in reality (than their paper-based values), some components may malfunction or the results may not meet the user’s requirement. In our design, the most important part to be analyzed is the VCO, since it’s an oscillator that is required to output waves with precise frequencies. If they goes wrong due to biased resistors and capacitors, the note the synthesizer played would be out of tune. The estimation is not necessary to other modules like VCF or ADSR since they are designed to be adjusted in a very large scale by users so the biases in components have already contributed to these adjustments.

Suppose this is the final VCO design with all values set precisely to get expected results. Tolerance estimation is done by adding up all the percentage errors of the component values that appear in the formula of the period/frequency of the wave outputted. (This is basically what we’ve learnt in A-level physics.)

****

The formula for the period, after using node methods,is:

T = 2U/[Vin(R37-R40)/2C8\*R37\*R40] + 2U/[Vin/2R37\*C8]

Where Vin is the DC input voltage and U =±10\*R42/(R41+R42)

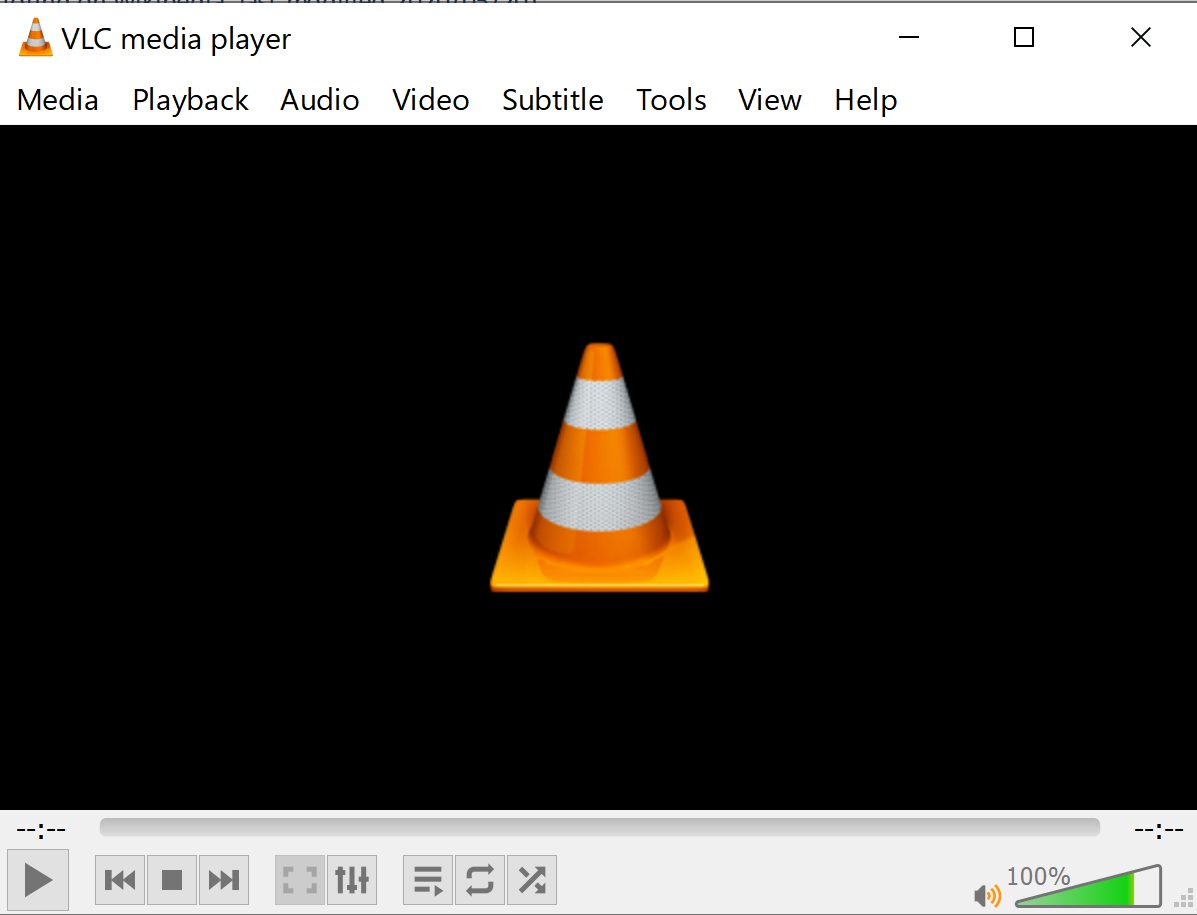
The tolerance for each resistor is (invariably) 1% and for capacitor C8 is 20%

The final percentage-period-deviation (also for the frequency) is 49% after some calculation. This value is huge, if a 500HZ (which is the highest note in the synthesizer) ideal wave is outputted, the actual wave would have a frequency of 745HZ and obviously the synthesizer is out of tone. This result represents the worst case that the synthesizer can get, and it gives a warning that extreme cares should be taken when choosing the capacitor.

**Evaluation points**

1. The quality of a music synthesiser is a subjective criterion, but try comparing the sound it makes with recorded samples of commercial synthesisers that you find on the internet.

Instead of using MATLAB to play the outputted wave as sound, we discovered a better software: VLC media player, that plays the .wav file directly without other operations.

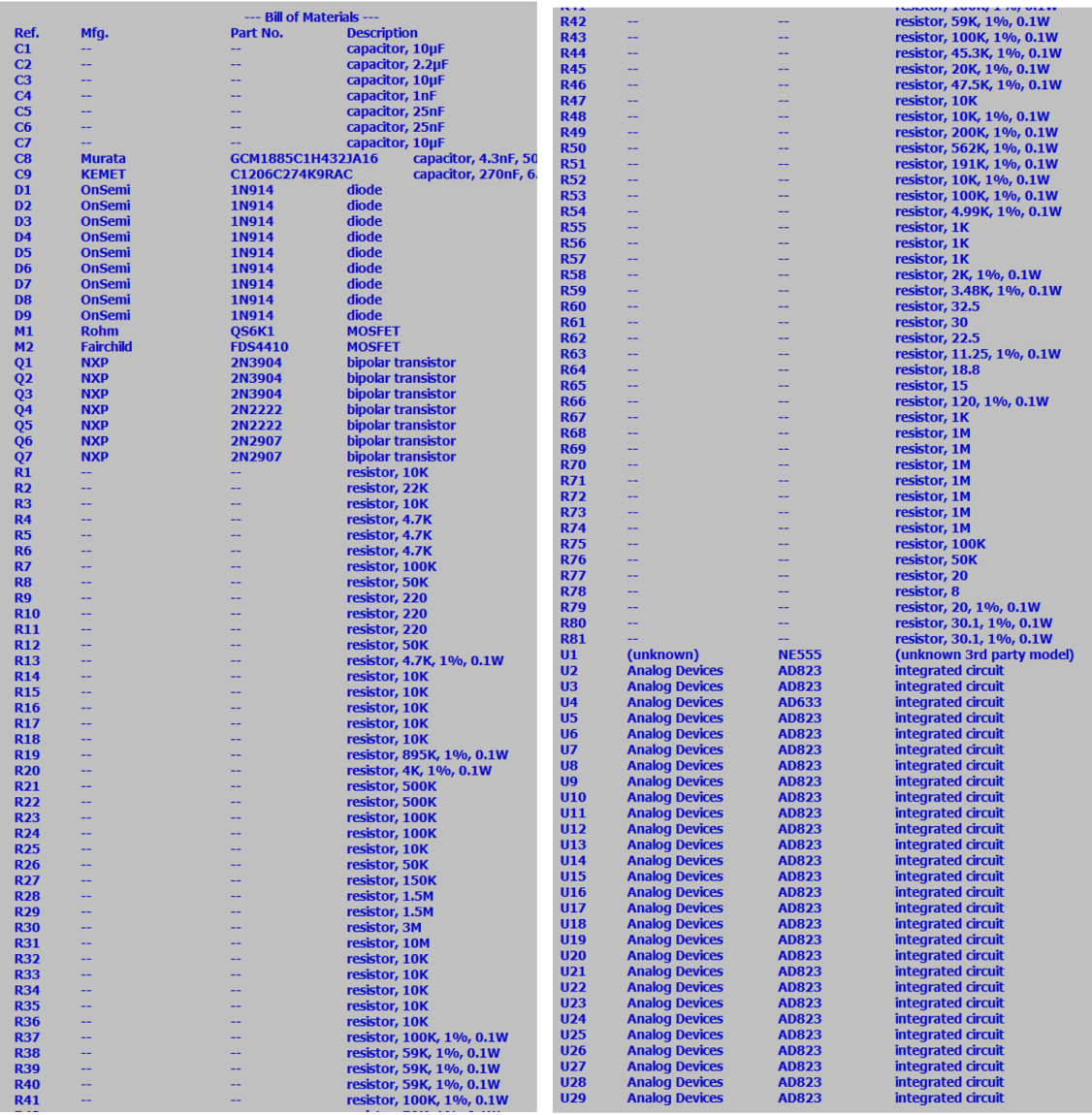


**The VLC media player**

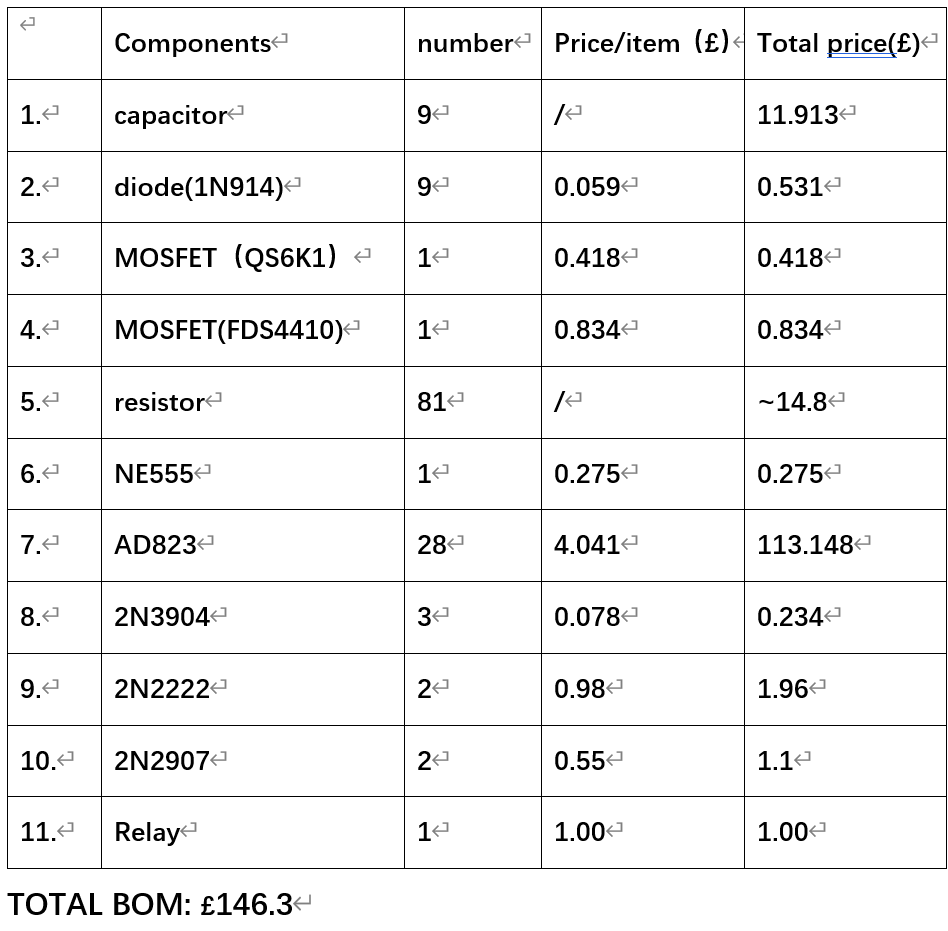
We compared the DO and MI notes to the that from a commercial synthesiser found on the internet(download link attached in appendix), the generated sounds did have similar pitches to the reference sounds. These two notes will be played in our video report.

1. Calculate the BOM (bill of materials) cost for your design by summing up the costs of all the components you have used.

We counted the number of each component from the list printed by LTSpice(see Figure A below), and took reference costing from 4 online shops. Figure B gives the final bill.



**Figure A. list of components**

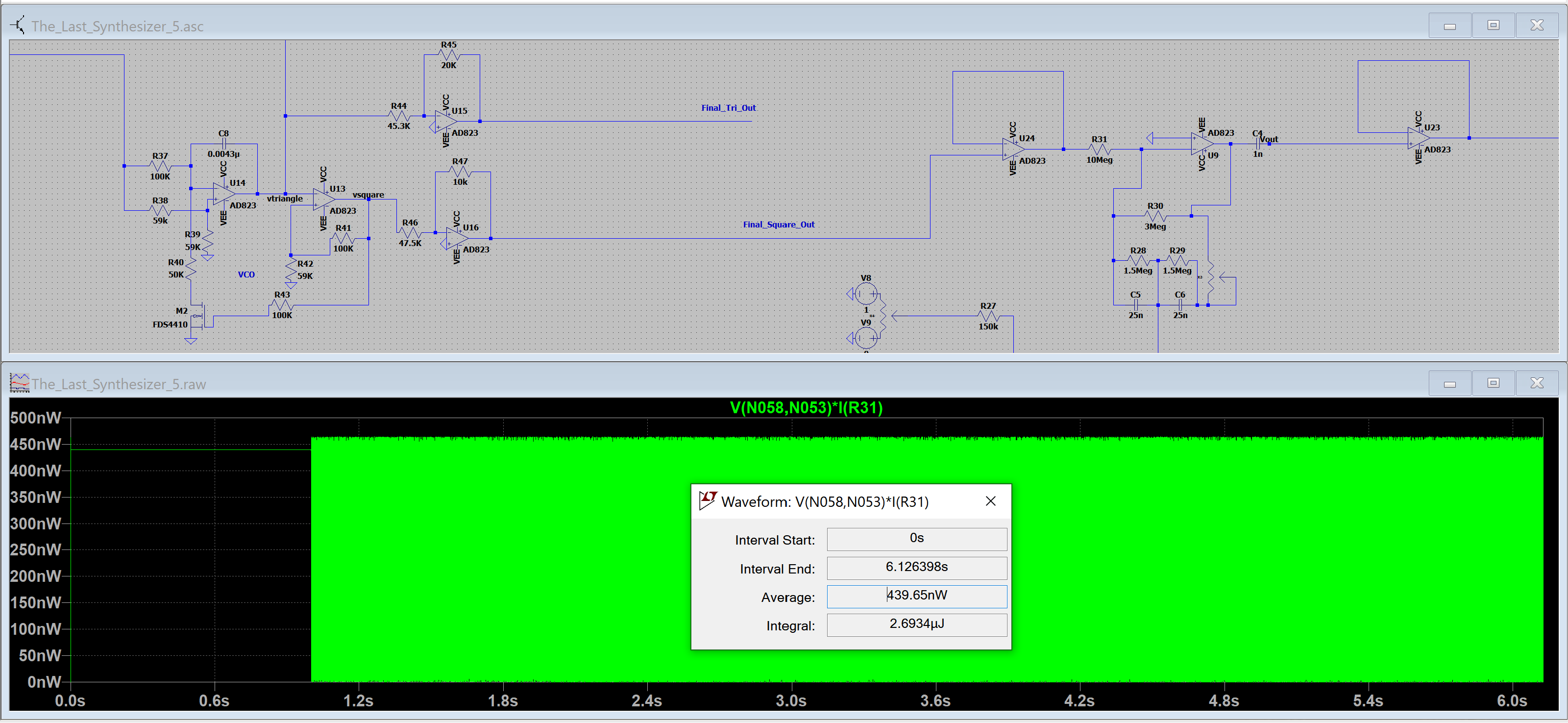
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**Figure B. BOM**

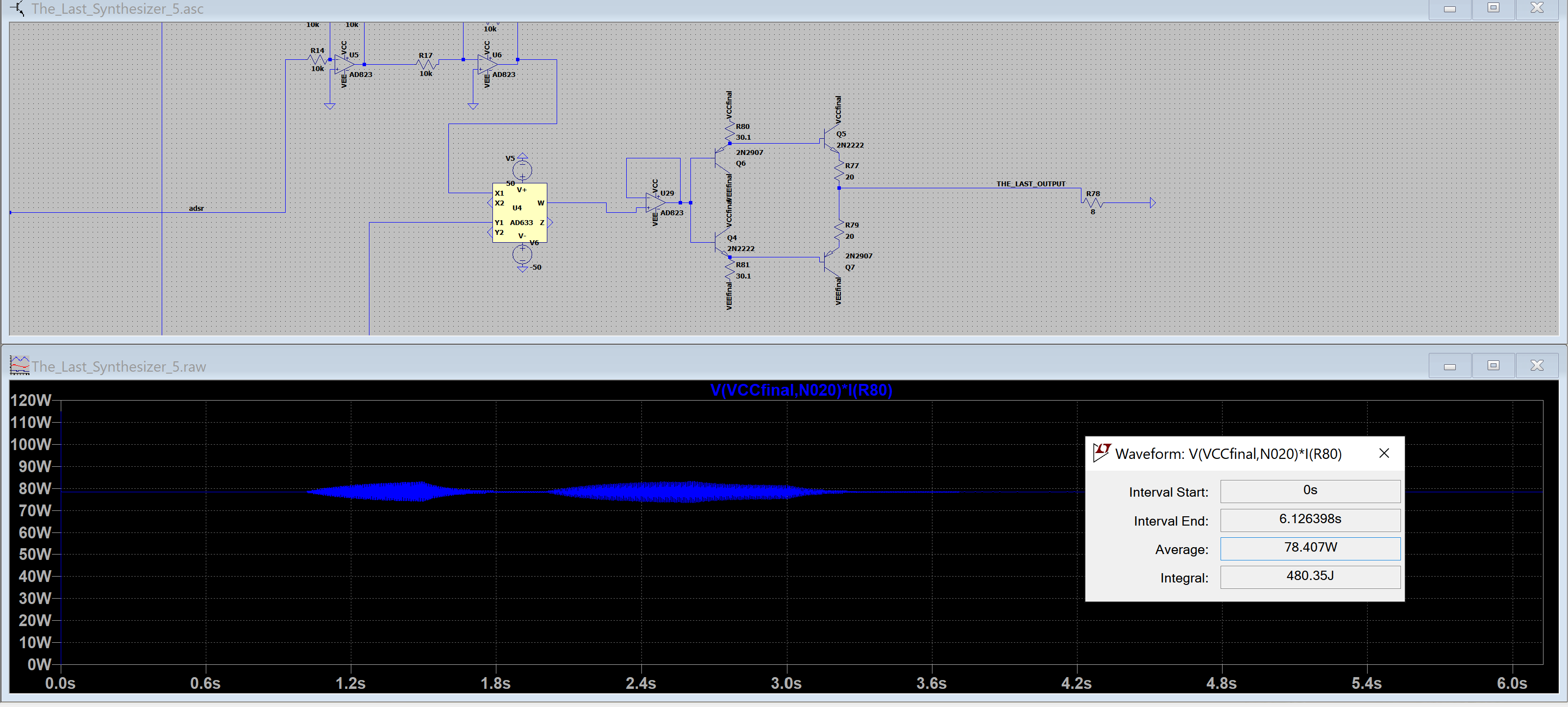
1. Find the power consumption of your design and investigate if it varies as you use different functions. Find how the power consumption breaks down between the different circuit blocks.

LTSpice has the function of calculating power of a component for us. Operation to do this was found online (<https://forum.allaboutcircuits.com/threads/show-the-power-in-ltspice.110252/>,by crutschow on Apr 24, 2015).

So for our circuit, we plotted the power of stages that had voltage sources as inputs : VCO and AB power amplifier, for the DO and MI notes. The resistors at output point of VCO(R31) and input of AB power amplifier(R80) were the measuring objects, as shown in Figure C and D.

****

**Figure C. average power of VCO(**

****

**Figure D. average power of**

From the graphs, we cans see that he power amplifier has very large power consumption, which is reasonable due to its large +-50V bias voltages, and that VCO has nearly no average power as it only supplies low voltages. The power when inputting triangle or sine wave is the same as this square wave value,and different notes also caused same power consumption.**Appendix**

**References:**

**-Introduction:**

(1) Scientific pitch notation(found on Wikipedia, Last updated June 05, 2020)

[https://wikimili.com/en/Scientific\_pitch\_notation](https://wikimili.com/en/Scientific_pitch_notation" \t "https://ukc-onenote.officeapps.live.com/o/_blank)

**-VCO:**

(1) Four-Diode Three-Segment Triangular To Sine Wave Shaper(created by GGoodwin on Feb/2018, on Multisim.com)

[https://www.multisim.com/content/ynUwgoTGbMjjpmcTZMLPsd/4-diode-3-segment-triangular-to-sine-wave-shaper/](https://www.multisim.com/content/ynUwgoTGbMjjpmcTZMLPsd/4-diode-3-segment-triangular-to-sine-wave-shaper/" \t "https://ukc-onenote.officeapps.live.com/o/_blank)

**-Keyborad:**

1. cax360 gif (by疯狂机械控, created on 2016-04-09 14:59)

https://www.sohu.com/a/68442498\_379180

**-ADSR:**

(1)Analog Synth - Dual ADSR Module(Last modified: 2012/05/16 by ve3wwg)

[https://www.experimentalistsanonymous.com/ve3wwg/doku.php?id=synth\_dual\_adsr](https://www.experimentalistsanonymous.com/ve3wwg/doku.php?id=synth_dual_adsr" \t "https://ukc-onenote.officeapps.live.com/o/_blank)

(2)Envelope generator(Last modified: 2010/12/31)

[https://www.yusynth.net/Modular/EN/ADSR/index\_new.html](https://www.yusynth.net/Modular/EN/ADSR/index_new.html" \t "https://ukc-onenote.officeapps.live.com/o/_blank)

(3)Envelope (music)(found on Wikipedia, last modified:2020/05/20)

[https://en.wikipedia.org/wiki/Envelope\_(music)](https://en.wikipedia.org/wiki/Envelope_(music)" \t "https://ukc-onenote.officeapps.live.com/o/_blank)

(4)Analog Modular Synthesizer(created by Dominik Martinez,2017/05/20)

[https://web.mit.edu/6.101/www/s2017/projects/dominikm\_Project\_Final\_Report.pdf](https://web.mit.edu/6.101/www/s2017/projects/dominikm_Project_Final_Report.pdf" \t "_blank)

(5)ADSR Envelopes: How to Build The Perfect Sound (created by Rory Seydel on 01.11.16)

[https://blog.landr.com/adsr-envelopes-infographic/](https://blog.landr.com/adsr-envelopes-infographic/" \t "_blank)

**-VCA:**

(1)A Voltage Controlled Amplifier(editor and date of publish unclear, found online)

[https://leachlegacy.ece.gatech.edu/ece4435/sp09/dp02a.pdf](https://leachlegacy.ece.gatech.edu/ece4435/sp09/dp02a.pdf" \t "https://ukc-onenote.officeapps.live.com/o/_blank)

(2)learning about electronics (editor and date of publish unclear, found online)

[http://www.learningaboutelectronics.com/Articles/What-is-the-cutoff-voltage-VGSOFF-of-a-FET-transistor](http://www.learningaboutelectronics.com/Articles/What-is-the-cutoff-voltage-VGSOFF-of-a-FET-transistor" \t "https://ukc-onenote.officeapps.live.com/o/_blank)

**-Analogue Multiplier**

(1)The Summing Amplifier(found on Electronics tutorials)

[https://www.electronics-tutorials.ws/opamp/opamp\_4.html](https://www.electronics-tutorials.ws/opamp/opamp_4.html" \t "https://ukc-onenote.officeapps.live.com/o/_blank)

**-VCF:**

1. DIY Analog Synthesizer Part 3: The Voltage Controlled Filter (VCF)

https://www.youtube.com/watch?v=EPUjrjAyfzU

**-LFO:**

1. lgresko\_Project\_Final\_Report(by Lauren Gresko,Elaine McVay and Elliott Williams posted on May 15, 2014)

<http://web.mit.edu/6.101/www/s2014/projects/lgresko_Project_Final_Report.pdf>

**-Evaluation points:**

1. Compare music quality:

Korg MonoPoly synth (product of Danny Wolfers’ studio, exact date of production unclear)

<https://beatproduction.net/korg-monopoly-samples/>

1. BOM

<https://www.cricklewoodelectronics.com/2N2222A.html?gclid=Cj0KCQjwrIf3BRD1ARIsAMuugNujGC2NoiO3UBYSly-dNWOOkCpmHV0-yCNfoNHXHeG5HSsAalsOdNYaAnhxEALw_wcB>

<https://uk.rs-online.com/web/>

<https://www.icompplus.com/en/transistors/3589/2N2907?gclid=Cj0KCQjwrIf3BRD1ARIsAMuugNsyHzUXcD7hIX-ZSSecIdAdeYXAY1X0T0IwjYMKX_f2k9INIIdoQ7caAsQSEALw_wcB>

https://www.mouser.com/ProductDetail/Omron-Electronics/G5LE-14-DC12?qs=VO24nqdQNUA5v9m0kcqpMw%3D%3D

**Data sheets:**

**-VCO:**

1. LM358(by National Semiconductor on Oct/2005, found online)

[https://www.sparkfun.com/datasheets/Components/General/LM358.pdf](https://www.sparkfun.com/datasheets/Components/General/LM358.pdf" \t "https://ukc-onenote.officeapps.live.com/o/_blank)

(2) FDS4410(by Fairchild Semiconductor on Apr/1998, found online)

[https://www.alldatasheet.com/datasheet-pdf/pdf/51465/FAIRCHILD/FDS4410.html](https://www.alldatasheet.com/datasheet-pdf/pdf/51465/FAIRCHILD/FDS4410.html" \t "https://ukc-onenote.officeapps.live.com/o/_blank)

**-VCA:**

(1) 2N5432(by Vishay Siliconix on Jun/2001, found online)

[http://www.bgmicro.com/pdf/2n5434.pdf](http://www.bgmicro.com/pdf/2n5434.pdf" \t "https://ukc-onenote.officeapps.live.com/o/_blank)

**-VCF:**

1. QS6K1 datasheet

[https://www.mouser.com/datasheet/2/348/qs6k1-210565.pdf](https://www.mouser.com/datasheet/2/348/qs6k1-210565.pdf" \t "https://ukc-onenote.officeapps.live.com/o/_blank)

**-Sample and hold:**

The G5LE relay datasheet (OMRON Corporation Electronic and Mechanical Components Company)

<https://omronfs.omron.com/en_US/ecb/products/pdf/en-g5le.pdf>

**-Analogue Multiplier:**

(1)AD633(by analogue devices on 2015,found online)

https://www.analog.com/media/en/technical-documentation/data-sheets/AD633.pdf