ENEE350
Final—Fall 2008
CLOSED BOOK AND NOTES
EXAM PERIOD 120 MINUTES

Instructions:

- Each problem is worth 5 points. No partial credits. The total score is 100 points + 5 bonus points.
- Use the space provided below each problem. if you need more space, please ask a proctor.
- Write your name and student id on the cover sheet.
- Promptly hand in your test to a proctor when the test is over.

NAME: _____

STUDENT ID: _____

Problem 1: Suppose that p and q are unsigned binary numbers, respectively. What will be the value of q after the following operation: $q = q << p$?

(a) $p \times 2q$	(b) $q \times 2p$	(c) $q \times 2^p$
(d) $p \times 2^q$	(e) none of the above	

Problem 2: The instruction repertoire of a certain computer consists of 128 instructions each of which uses one memory address and 64 instructions each of which uses two memory addresses. Assuming that the memory of this computer contains 2048 locations, what is the minimum number of bits needed to code all the instructions?

(a) 32 bits	(b) 30 bits	(c) 29 bits
(d) 16 bits	(e) none of the above	

Problem 3: Which of the following statements is not true regarding VESP 1.0 architecture?

(a) It has 8 instructions	(b) It does not have an IX register	(c) It supports indirect addressing
(d) It has a hardware stack	(e) none of the above.	

Note: (c) is not the correct answer as was suggested by a student during the lecture because you can implement indirect addressing in Vesp 1.0 through self-modifying code.

Problem 4: What instruction does the following describe in VESP 1.0?

```
vesp.MEMORY[vesp.IR&0x0FFF]=vesp.MEMORY[vesp.MEMORY[(vesp.MAR)+1]];
vesp.PC = vesp.PC + 1;
vesp.clock = vesp.clock + 2; break;
```

(a) Load immediate	(b) Move direct	(c) Store immediate
(d) Move indirect	(e) none of the above	

Problem 5: Suppose that p,q, and r are 16-bit 2's complement numbers. Computing the expression $5\times p + 8\times q - 4\times r$ on a processor which can add or subtract two 16-bit numbers in 1 clock cycle and shift a 16-bit number one bit to the left or to the right in 1 clock cycle, takes at least

(a) 5 clock cycles	(b) 8 clock cycles	(c) 6 clock cycles
(d) 10 clock cycles	(e) none of the above	

Problem 6: A stack program that computes the in-order expression a - b + c – d is

(a) PUS b; PUS a; SUS PUS d; PUS c; SUS ADD;	(b) PUS b; PUS a; ADD PUS d; PUS c; SUS SUS;	(c) PUS a; PUS b; SUS PUS d; PUS c; SUS ADD;
(d) PUS b; PUS a; SUS PUS c; PUS d; SUS ADD;	(e) all of the above	

Problem 7: A certain computer performs stack instructions to perform post-order expressions. If the stack pointer initially contains 15, what will it contain after the following expression is executed: ab+cef-+-

(a) 15	(b) 19	(c) 20
(d) 18	(e) none of the above	

Problem 8: The fetch-decode-execute cycle of a processor is shown below:
while (reset == 0) {MAR = PC; PC = PC + 1; read = 1; IR = RAM[RAM[MAR]];
switch(IR) {case 0: $R_0 = R_0 + R_1$;break; case 1: $R_0 = R_0 - R_1$; break;
case 2: $R_0 = R_0 \mid R_1$; break; case 3: $R_0 = R_0 \& R_1$; break;} }

How many clock cycles does the fetch-decode-execute cycle take?

(a) 1	(b) 2	(c) 3
(d) 4	(e) 5	

The binary codes for the vesp instructions are given below in hexadecimal notation:

ADD: 0, CMP: 1, LDA: 2, MOV: 3, JMP: 4, JEZ: 5, JPS: 6, HLT: 7, INC: 8, DEC: 9, AND: A, IOR: B, SHL: C, SHR: D, MXF: E, MXT: F.

Problem 9: What will be the decimal value stored in the A register after the following vesp program, which is written in hexadecimal notation, is executed? (All the numbers are in hexadecimal format)

Location 100: 2001 Location 101: 0011 Location 102: 2000 Location 103: 0101
Location 104: 0000 Location 105: C000 Location 106: 9000 Location 107: 7000

(a) 7	(b) 15	(c) 31
(d) 63	(e) none of the above.	

Problem 10: What will be decimal value of the PC after the following vesp program is executed? (Locations are shown in decimal format)

Location 100: 2000 Location 101: 1100
Location 102: 606A Location 103: 4068
Location 104: 1000 Location 105: 7000
Location 106: 6068 Location 107: 7000

(a) 103	(b) 105	(c) 107
(d) 106	(e) none of the above.	

A microprogrammed processor uses the following 16-bit microinstruction format and operations:

ABUS select	BBUS select	OBUS	Destination	Branch condition	Branch address
1 bits	1 bit	3 bits	3 bits	2 bits	6 bits

ABUS select	Code	BBUS select	Code	OBUS	Code	Destination select	Code
A	0	B	0	ABUS	000	A	000
PC	1	MDR	1	BBUS	001	B	001
				ABUS + BBUS	010	MDR	010
				ABUS + ~BBUS + 1	011	PC	011
				~ABUS	100	IR	100
				~BBUS	101	IX	101
				1	110	MAR	110
				0	111		

Branch condition	Code	Branch condition	Code	Branch condition	Code	Branch condition	Code
A>0	00	A=0	01	0	10	1	11

Problem 11: Which of the following hexadecimal microprograms performs the computation: IX = A - B;

(a) 1A00	(b) 1C00	(c) 1D00
(d) 1B00	(e) none of the above.	

Problem 12: Which of the following micro-operations cannot be performed on this micro-programmed processor?

(a) MAR = IR	(b) PC = PC + 1	(c) A = A - MDR
(d) IX = MDR;	(e) none of the above.	

Problem 13: What will be the decimal value stored in the B register after the following microprogram (written in hexadecimal) is executed?
location 0: 32C1 location 1: 30C2 location 2: 59C3 location 3: 34C4

(a) -2	(b) 0	(c) 1
(d) 2	(e) none of the above.	

Problem 14: A processor executes four instructions in the time it fetches and decodes one instruction. If it takes 10^{-10} seconds to fetch and decode an instruction, and if the speed of the execution unit is doubled, How much speed-up will we get?

(a) 1.25	(b) 1.33	(c) 1.75
(d) 1.11	(e) none of the above.	

Problem 15: A computer is designed as a cascade of A, B, and C units. Its operations are carried out by cycling through each of these three units repetitively where all units carry their part of the computation in the same amount of time. If A and B can be speeded up by a factor of 2 each, but C cannot be speeded up at all, what will be maximum speed up that this computer can have?

(a) 1	(b) 1.5	(c) 2
(d) 3	(e) none of the above.	

Problem 16: The following blocks of memory are cached into a 4-frame cache from left to right using the OPT replacement algorithm. What four blocks of memory will reside in the cache after the last block is referenced? 8 1 3 1 3 8 6 5 7 1 2 4 3

(a) 1,3,5,7	(b) 1,2,3,4	(c) 5,6,7,8
(d) 2,4,6,8	(e) none of the above.	

Problem 17: A set associative cache memory uses 2 sets of 2 frames each to hold blocks of 256 words which are loaded from a memory of 8,192 words. How many blocks will be assigned to each set?

(a) 64	(b) 16	(c) 32
(d) 128	(e) none of the above.	

Problem 18: An interrupt service circuit uses a dynamic algorithm to adjust the priorities of two devices *x,y* that can interrupt a computer. Each time it examines the interrupt requests, the circuit services the devices as follows:

(1) If no device has interrupted, nothing is done,

(2) If only one device has interrupted, that device is serviced, and the priorities are left unchanged,

(3) If two devices have interrupted the device that has interrupted with high priority is serviced and the priorities of the two devices are switched.

Assuming that *x* is assigned the high priority (priority 1), *y* is assigned low priority (priority 2) when the circuit begins first its operation, which of the following sequences of services are rendered for the sequence interrupt requests x, y, xy, x, y, xy, xy, y, x?

(a) x,x,y,x,y,x,x,y,x	(b) x,x,y,x,x,y,x,y,x	(c) x,y,x,x,y,x,x,y,x
(d) x,y,x,x,y,y,x,y,x	(e) none of the above.	

Problem 19: If pipeline A has 5 stages and operates at a clock rate of 4 GHz and pipeline B has 10 stages and operates at a clock rate of 8 GHz, which of the following statements are true?

(a) B is not as highly utilized as A does.	(b) A and B are equally fast.	(c) B is twice as fast as A.
(d) A is not as highly utilized as B does.	(e) none of the above.	

Problem 20: A 6-stage instruction pipeline executes a mix of programs that contains 20% load and store instructions, each taking 3 clock cycles, 60% arithmetic instructions, each taking 3 clock cycles and 20% conditional branch instructions, each taking 2 clock cycles. Assume that all stages take one cycle. If every conditional branch instruction stalls (delays) the pipeline by 1 cycle to determine if the branch should be taken and no other instruction stalls it, how much speed-up would this pipeline provide in executing the given mix of programs over a serial processor assuming that both are clocked at the same frequency?

(a) 1.33	(b) 2.33	(c) 1.67
(d) 2.67	(e) none of the above.	

Problem 21: Write a multiple choice problem which covers your favorite material in the course, and mark the correct answer. (without using any of the problems in the test.)

Have a great winter break!