Random Telegraph Noise in 45-nm CMOS: Analysis Using an On-Chip Test and Measurement System

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Abstract

RTN measurements in 45-nm CMOS across device bias and geometry using an on-chip characterization system are reported. An automated methodology for extracting RTN levels, amplitude and dwell times is developed. Complex RTN magnitude is statistically modeled, and device size and bias parameter dependencies of the developed model are examined.

Introduction

Random telegraph noise (RTN) has been a source of growing concern in recent years, as its effects are beginning to seem comparable to traditional sources of device variability, such as random dopant fluctuations, at small geometries [1]. New methods for measuring and modeling RTN are necessary to gain more understanding of the statistics of RTN (number of observable traps, fluctuation amplitudes, and dwell times) as a function of bias and device size. In this work, we describe a fully integrated on-chip measurement system that allows fast and accurate I-V characterization of large transistor arrays without need for external test and measurement equipment; digital interfaces make the circuits compatible with digital in-line test. An automated methodology is developed to extract RTN levels and dwell times from extensive time domain data. A lognormal model for single-trap RTN amplitude distributions is developed and used to derive cumulative distribution functions (CDFs) across device bias and geometry.

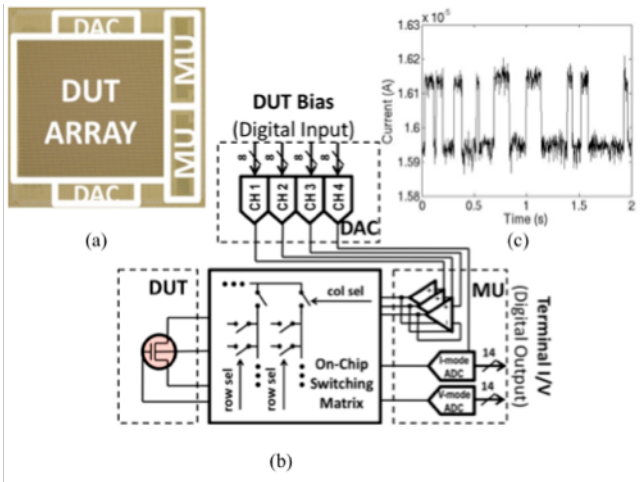


Fig. 1 On-chip measurement system in 45-nm CMOS: (a) die photo; (b) high-level system schematic; (c) typical RTN waveform.

Measurement System

A fully integrated on-chip measurement system (Fig. 1) in bulk 45-nm CMOS allows fast and accurate I-V characterization of a large transistor array (nearly 2200 nFET transistors) integrated on the same die. Current and voltage measurements performed using on-chip ADCs are combined in a Kelvin-sensing configuration to cancel out the resistances of the on-chip switching matrix; a four-channel DAC is used to supply device bias. Transistors are characterized in weak to moderate inversion (V_{GS} between 0.56V and 0.72V, with V_{SB} = 0.2V and V_{DS} = 50mV), where the RTN drain current amplitude fluctuations ($\Delta I_D/I_D$) are found to be largest [2,3]. At the corresponding I_D levels of 2-25 µA, the on-chip system can operate at a sampling rate of 50 kSample/s with an LSB of 2.44 nA; voltage measurement resolution exceeds 1 mV. A typical RTN waveform is shown in Fig. 1c.

Data Analysis

In order to analyze RTN time domain waveforms, we use time lag plots (TLPs) [3], augmented to include information on the relative frequency, with which each point of the TLP is occupied. The TLP in this case is a two-dimensional histogram with one LSB of separation between individual bins (ΔI_D = 2.44 nA; Δt = 20 µs). Our modified approach (Fig. 2) allows us to accurately discern RTN levels that

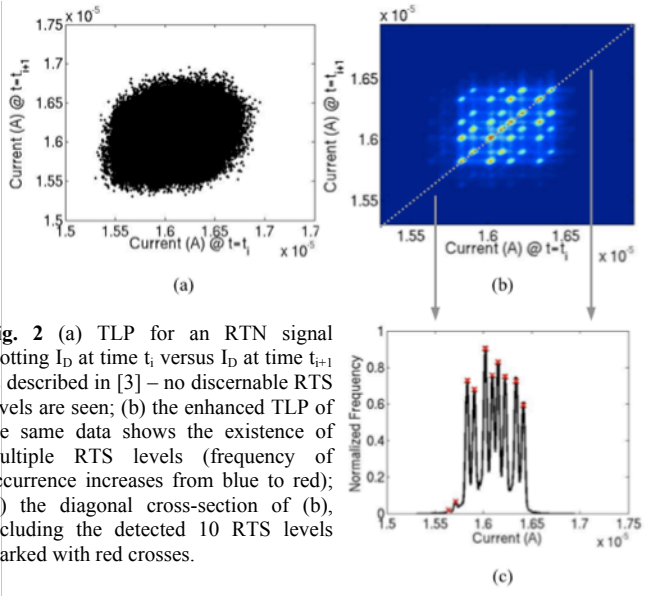


Fig. 2 (a) TLP for an RTN signal plotting I_D at time t_i versus I_D at time t_{i+1} as described in [3] – no discernable RTS levels are seen; (b) the enhanced TLP of the same data shows the existence of multiple RTS levels (frequency of occurrence increases from blue to red); (c) the diagonal cross-section of (b), including the detected 10 RTS levels marked with red crosses.

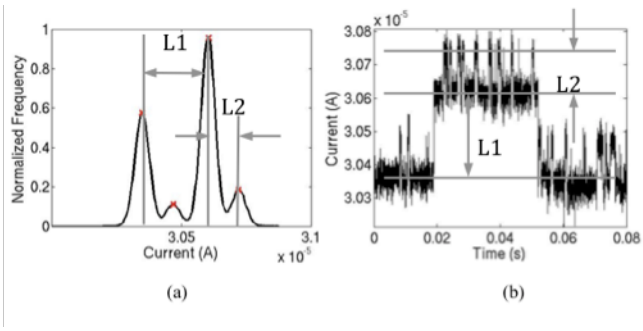


Fig. 3 Single-trap RTN magnitude extraction from a dual-trap RTN signal: the most intense and least intense levels in the TLP diagonal plot are mutually exclusive (i.e. traps occupied in one of the states are unoccupied in the other and vice-versa); the spacing of either one of the two extreme levels to the intermediate two gives the magnitude of each of the two traps.

would have otherwise remained undetected. After taking a cross-section along the diagonal of the TLP, simple thresholding can be used for level detection as shown in Fig. 2c. The number of detectable traps can be estimated as N_T = ceiling($\log_2(N_L)$), where N_L is the number of detected levels. The amplitude ($\Delta I_D/I_D$) of an individual trap is given by the spacing between the two maxima along the TLP diagonal. Fig. 3 gives an example of such an extraction for the case of two traps. Time domain analysis is performed using a hidden Markov model (HMM) [4] to detect transitions (Fig. 4a); characteristic dwell times are extracted by fitting measured rate histograms to an exponential distribution (Fig. 4b).

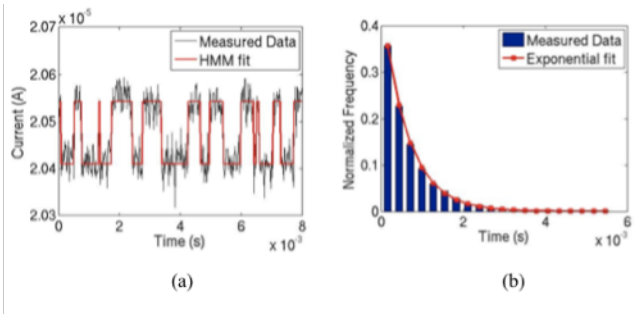


Fig. 4 (a) Using HMM modeling software to generate idealized RTN waveforms from noisy measurement data; (b) extracting capture/release rates from rate histograms generated from the idealized RTN waveforms.

Statistics for N_T

N_T has a different Poisson distribution for each bias point and device size (Fig. 5) [3,5]. Fig. 6 shows the average number of detectable traps (λ) as a function of gate bias for different device sizes. The number of detectable traps increases with increasing V_{GS} as the average trap energy is lowered closer to the Fermi energy, increasing the probability that a trap changes state during the measurement window [6]. λ does not scale proportionally to device area, as suggested in [5]. Increasing the device length decreases the number of detectable traps, even though device area is

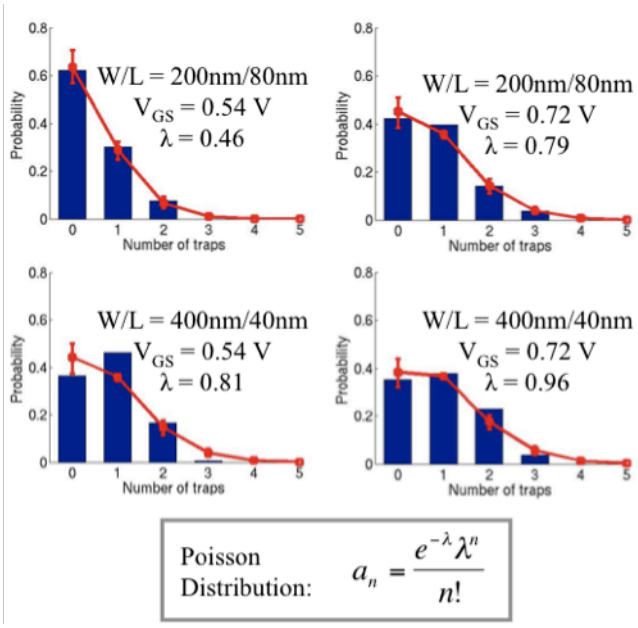


Fig. 5 Examples of Poisson distribution fits for different device sizes and biases; in all cases the Poisson PDFs (red lines) match well to the measured distributions (solid bars).

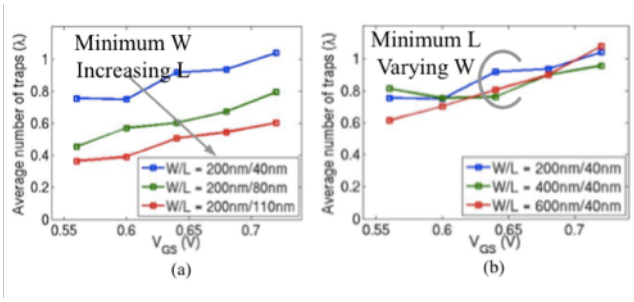


Fig. 6 Extracted average number of traps (λ) as a function of gate bias (a) for a set of minimum-width devices with varying lengths and (b) for a set of minimum-length devices with varying widths; λ appears to be inversely related to the length of the device and relatively independent of its width.

increasing. This indicates that smaller-length devices are more susceptible to RTN.

Statistics for $\Delta I_D/I_D$ for Individual Traps

We extract the amplitude distribution across gate bias for over 70 devices of each type that have one or two observable traps. We find (Fig. 7) that the amplitude distribution is better represented by a lognormal distribution [1] than an exponential distribution [3,5]. Fig. 8 shows the mean single-trap RTN magnitude (Λ) as a function of V_{GS} and device size. The single-trap RTN decreases with increasing V_{GS} [2,3]. Across device width, for minimum-channel-length devices, Λ decreases with increasing device area [5]. Across different lengths, we find that the minimum-length devices show a considerably higher single-trap RTN, even when equal area devices are compared.

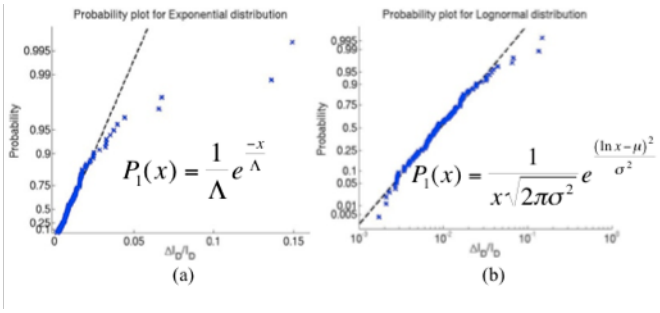


Fig. 7 Comparison between (a) exponential and (b) lognormal fits for $\Delta I_D/I_D$ for single-trap RTN; blue crosses represent measured data, dashed reference lines represent ideal fits; example is representative of all measured data and clearly shows the lognormal distribution to be a better fit.

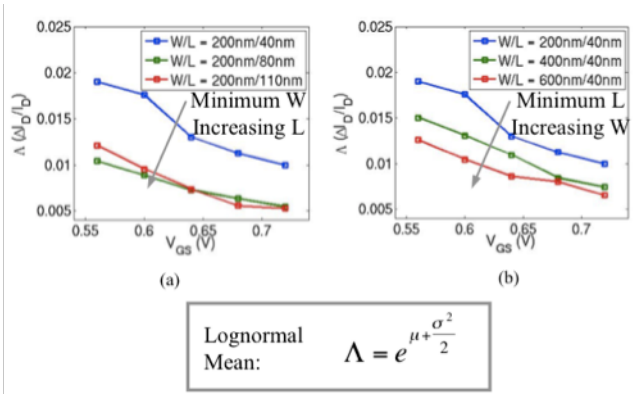


Fig. 8 Mean single-trap magnitude (Λ) as a function of V_{GS} across minimum-width devices with different lengths (a) and minimum-length devices with different widths (b); comparing devices of equal area (green line in (a) and (b)), minimum-length devices exhibit considerably greater single-trap RTN amplitude.

Dwell Time Analysis

Analysis of the capture and release rates of individual traps across bias allows us to distinguish between the characteristics of individual traps. We find that $\Delta I_D/I_D$ fluctuations are determined primarily by observable traps that are either neutral (Fig. 9a) or bistable (Fig. 9b) [6]. Bistable traps (typically rare [6]) are primarily observed.

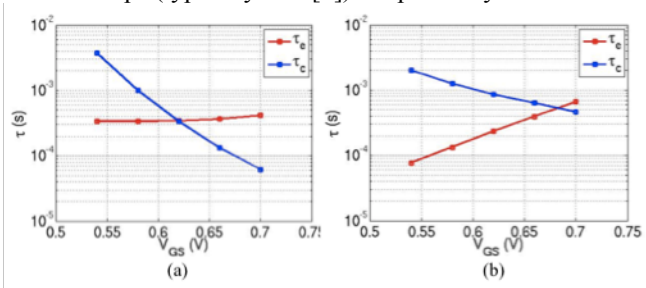
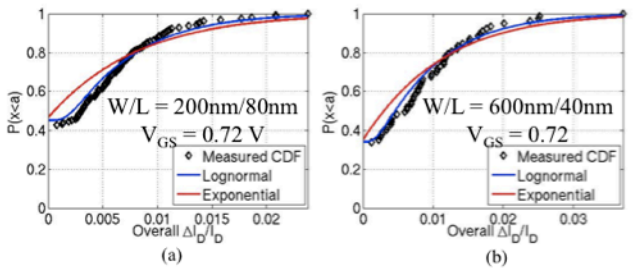


Fig. 9 Example measurements of observed types of traps: neutral traps (a), characterized by a constant emission rate and a capture rate, which decreases with carrier density, and bistable traps (b), characterized by symmetrical capture and release rates.



RMS Error	Plot (a)	Plot (b)
Lognormal $P_1(x)$	5.3%	6.5%
Exponential $P_1(x)$	14.3%	15.2%

Overall $\Delta I_D/I_D$ Amplitude Model [4]:

$$P_n(x) = \int_{-\infty}^{\infty} P_{n-1}(x-t)P_1(t)dt$$

$$P(x) = a_0\delta(x) + \sum_{i=1}^{\infty} a_i P_i(x)$$

See Fig. 5 and Fig. 7b for definitions of a_n and $P_1(x)$

Fig. 10 Examples of CDF plots comparing the effect of using an exponential and a lognormal fit in the model for determining the overall RTN amplitude.

CDFs for $\Delta I_D/I_D$

Modeling the CDFs for $\Delta I_D/I_D$ is important for circuit applications and may need to be a feature of future compact models. Using the distributions extracted for N_T and $\Delta I_D/I_D$ for individual traps, we are able to calculate the CDFs for $\Delta I_D/I_D$, comparing the modeled results with measured statistics [3]. Fig. 10 shows an example comparison using both a lognormal and an exponential PDF to model single-trap $\Delta I_D/I_D$ variations. Across all devices and gate biases, the average rms error is 4.3% for the lognormal distribution (compared with more than 10% for an exponential distribution). Fig. 11 shows a comparison between measured and modeled overall RTN magnitude at the 95-percentile

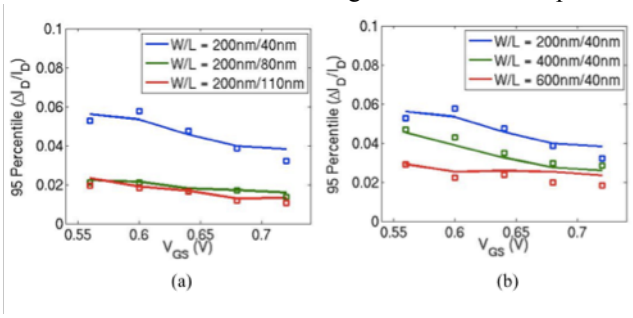


Fig. 11 Comparison between measured (squares) and modeled (solid lines) 95 percentile bound for overall RTN amplitude variation across gate bias for (a) minimum-width devices with varying lengths and (b) minimum-length devices with varying widths; in both cases good agreement between measured and modeled results is observed.

level, demonstrating our ability to accurately model the tails of the complex RTN CDF.

Conclusion

Measurements of complex RTN noise across gate bias and device geometry in a 45-nm CMOS process have been reported. A lognormal amplitude distribution and a Poisson number distribution have been combined to model complex RTN $\Delta I_D/I_D$ fluctuations. Analysis of dwell times has revealed the presence of both neutral and bistable traps. RTN magnitude has been shown to be more sensitive to reduction in device length than width, due to a relative increase in both λ and Λ.

Acknowledgments

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References

[1] N. Tega, et. al., "Increasing Threshold Voltage Variation Due to Random Telegraph Noise in FETs as Gate Lengths Scale to 20 nm", *Symposium on VLSI Technology*, pp. 50-51, 2009.

[2] A. Lee, et. al., "Random Telegraph Noise in 30 nm FETs with Conventional and High-κ Dielectrics", *Journal of Computational Electronics*, vol. 3, pp. 247-250, 2004.

[3] T. Nagumo, et. al., "New Analysis Methods for Comprehensive Understanding of Random Telegraph Noise", *International Electron Devices Meeting (IEDM)*, pp. 31.1.1-31.1.4, 2009.

[4] L. Rabiner, "A Tutorial on Hidden Markov Models and Selected Applications in Speech Recognition", *Proceeding of the IEEE*, vol. 77, number 2, pp. 257-286, February1989.

[5] K. Takeuchi, et. al., "Single-Charge-Based Modeling of Transistor Characteristics Fluctuations Based on Statistical Measurement of RTN Amplitude", *Symposium on VLSI Technology*, pp. 54-55, 2009.

[6] H. Muller, M. Schulz, "Individual interface traps at the Si—SiO_2 interface", *Journal of Material Science: Materials in Electronics*, vol. 6, number 2, pp.65-74, April 1995.