

Hybrid CMOS/GaN 40-MHz Maximum 20-V Input DC–DC Multiphase Buck Converter

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Abstract—This paper presents a 40-MHz hybrid CMOS/GaN integrated multiphase dc–dc switched-inductor buck converter with a maximum 20-V input voltage. The half-bridge switches are realized using lateral AlGaN/GaN HEMTs, while the drivers and other circuitry are implemented in standard 180-nm CMOS. The interface between the CMOS and GaN dice is achieved through face-to-face bonding, reducing inductive parasitics for the connection to less than 15 pH. A capacitively coupled level shifter provides the gate drive for the high-side GaN switch using 5-V CMOS devices. The converter demonstrates 76% efficiency for 8:1 V conversion and over 60% efficiency for conversion ratios up to 16:1.

Index Terms—Capacitively coupled level shifter, CMOS/GaN face-to-face bonding, gate drive for GaN, integrated voltage regulator (IVR), power electronics.

I. INTRODUCTION

A LARGE portion of global energy consumption can be attributed to electronics appearing as dc loads to the power grid (e.g., computers and servers, LED lighting, and electric cars), and an increasing part of electricity supply and generation is of dc nature (e.g., batteries, photovoltaics, and fuel cells). While dc supply voltages for modern microprocessors are moving well below 1 V for state-of-the-art integrated circuit cores, input dc voltage levels are either remaining fixed, as determined by battery supplies, or are increasing in order to reduce overall current levels in the power distribution networks (PDNs). All of these applications require high-efficiency dc–dc converters and regulators that must handle increasingly higher input voltages and lower output voltages, resulting in higher overall conversion ratio requirements.

In data centers, for example, dc–dc down conversion is traditionally performed in multiple steps, adhering to a set of standard intermediate voltages that enables compatibility across vendors and systems [1], as shown in Fig. 1(a). At the end of this conversion chain is a point-of-load (PoL) converter, which performs conversion close to the load. Increasingly, however, this multi-step voltage down-conversion approach is being challenged both by the desire to run larger parts of the PDN at higher operating voltages (to reduce the PDN impedance

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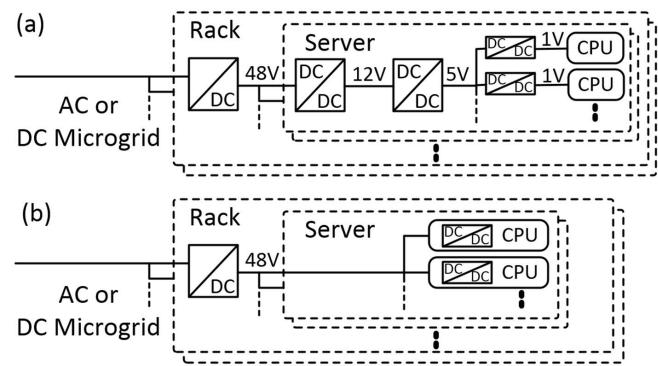


Fig. 1. Power distribution approaches for the data center. (a) Typical server power distribution scheme showing four steps of conversion to intermediate voltages between the high-voltage grid and the low-voltage components. (b) Alternate approach employing a CMOS/GaN integrated voltage regulator, reducing the number of conversion stages to two steps by utilizing a 48:1 converter.

requirements) and by the advantages of reducing the number of converter steps in improving overall conversion efficiency. This requires high-conversion-ratio, high-input-voltage PoL converters, such as that developed in this paper. For example, replacing three converters with a single converter as shown in Fig. 1(b) allows the overall conversion efficiency to be improved from 73% to 90% if each converter is 90% efficient, while allowing much of the PDN to operate at 48 V, a well-established voltage standard. Even higher input voltages could gain popularity as dc micro-grid standards emerge [2], [3].

Converters with 48 V (or higher) input voltages require high-voltage switches that traditionally allow maximum switching frequencies in the few hundreds of kilohertz, although the exact switching frequency and supported input voltage depend on the choice of switches, such as vertical diffusion MOS (VDMOS), trench MOS, or high-voltage laterally diffused MOS (LDMOS) silicon devices. On printed circuit boards or similar substrates, discrete (i.e., individually packaged) power transistors serve as the switching elements and are combined with switch driver chips, large board-level passive reactive components for energy storage (inductors and capacitors), and controller chips to realize a full system. Larger passive components are required because of the relatively low switching frequencies supported by these switch technologies.

PoL devices are traditionally switch-mode, medium-frequency (typically from 100 kHz to 2 MHz), and non-isolated dc–dc converters operating at sub-48-V input voltages. Board-level-integrated or package-integrated designs

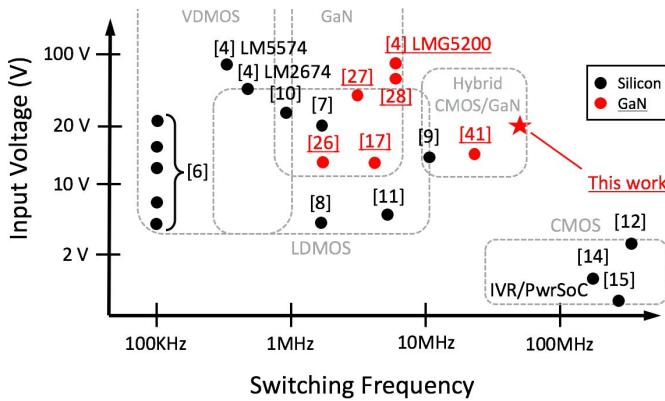


Fig. 2. Input voltage and frequency ranges of low output voltage regulators including VDMOS switches [4], [6] LDMOS switches [7]–[11], or GaN switches [7], [26]–[28]. Emerging CMOS IVR solutions allow higher switching frequencies at low input voltages [12], [14], [15]. This work is a demonstration of an integrated converter with both higher input voltage and higher switching frequency using GaN switches.

are commonly used. Power-supply-in-package examples can function at frequencies up to 8 MHz, but most still operate at <1 MHz [4] to keep switching losses low. However, board-level and package-level-integrated solutions remain difficult to miniaturize, limiting the number of supplies and the supply transient performance achievable for state-of-the-art computing systems [5]. Fig. 2 shows some representative published converter designs that are either board-integrated or package-integrated, using either VDMOS or LDMOS silicon switches [4], [6]–[11].

Very recently, integrated-voltage-regulator (IVR) converters, built on the same die as the load, have been pursued as replacements for traditional PoL converters. Reduction in interconnect parasitics [12], [13] allows IVRs to operate at much higher frequencies (generally 100–300 MHz [14], [15]) compared with non-integrated converters, with a consequent reduction in the size of passive components. IVRs are increasingly being pursued [14], [15] to provide high spatial and temporal granularity for controlling supply voltages to enable improved energy efficiency in microprocessors and other computing devices through dynamic voltage and frequency scaling. IVRs generally use CMOS devices for both the controlling circuitry and the power train switches [16], which limits the input voltage to 2.5 or 3.3 V (if thick-oxide transistors are employed in the power train). Some representative published CMOS IVRs are also noted in Fig. 2 [12], [14], [15].

GaN high-electron-mobility transistors (HEMTs) have emerged as a replacement for silicon-based power devices [5], [17]–[20], outperforming silicon switches with a combination of high breakdown voltages (up to 600 V), low specific on-resistance (< 0.2 mΩ · cm² [21]), and low gate charge requirements [22]. Although board-level converters with conversion ratios as high as 400:1 V [23] have been demonstrated with GaN HEMT switches, the inductive interconnect parasitics in these converters limit achievable switching frequencies to 5–10 MHz [24], [25]. Representative board-integrated GaN-based power converters are also noted in Fig. 2 [17], [26]–[28].

In this paper, we seek to combine the switching-frequency and integration advantages of CMOS IVRs with the input voltages achievable with GaN HEMTs through the on-die integration of GaN and CMOS, as shown in Fig. 2. Since GaN HEMTs achieve low on-resistance with low gate charge requirements, a GaN HEMT half-bridge can meet efficiency targets while switching at frequencies significantly higher than high-voltage silicon LDMOS half-bridges. The switching frequencies achievable with GaN switches can also be fully realized in these IVRs through dramatic reductions in the interconnect parasitics between the switches and passives [29]–[32]. The resulting converters offer high conversion ratio and high input voltage for PoL modules, enabling architectures such as that shown in Fig. 1(b).

There are several ways to realize higher levels of CMOS and GaN integration. Attempts at monolithic heterogeneous integration through the growth of GaN in windows on silicon-on-insulator have been reported [33], [34] as well as integration through substrate removal and wafer bonding (including layer transfer of GaN transistors) [35]. In both cases, the two technologies co-reside on the same substrate and share the same back-end interconnect metallization. This provides a major reduction in interconnect parasitics between the GaN and Si system blocks, but necessitates major modifications to CMOS fabrication practices and protocols, which makes the adoption of those approaches challenging.

Here, we demonstrate the integration of lateral AlGaN/GaN HEMTs with 180-nm CMOS circuitry through face-to-face bonding and use this technology to create a multiphase, 40-MHz buck converter supporting a 20-V input supply. Our Au–Au interconnects between the GaN chiplet and the CMOS substrate are 30 μm in diameter, and the die-to-die standoff distance is 50 μm, resulting in an interconnect inductance of less than 15 pH. In comparison, state-of-the-art packaging standards for discrete GaN transistors add interconnects inductance on the order of 100 pH from the package alone [36], and board interconnects typically result in total parasitic inductances in the nH range [37].

In Section II, we discuss the requirements on switches to achieve efficient dc–dc conversion in hybrid GaN/CMOS architectures. In Section III, we discuss the design of the prototype GaN/CMOS converter developed here. Section IV presents the experimental results from the demonstrator prototype. Section V concludes this paper.

II. EFFICIENCY CONSIDERATIONS IN THE DESIGN OF HYBRID GAN/CMOS CONVERTERS

The dominant conduction (P_{cond}) and switching (P_{sw}) losses in the transistors of a half-bridge step-down multiphase buck converter, neglecting any diode and inductor losses, can be expressed using the closed-form expressions [38]

$$P_{\text{cond}} = \left(1 - D - \frac{D}{R}\right) \cdot \frac{4}{3} \cdot I_o^2 \cdot R_{\text{DS(ON)}} \cdot N \quad (1)$$

$$P_{\text{sw}} = \left(\frac{1+R}{2}\right) \cdot V_{\text{GS}}^2 \cdot C_{\text{iss}} \cdot f_s \cdot N \quad (2)$$

where $I_o = I_{\text{max}}/2$ is the average current through the transistor of one phase in the ON-state, half the transistor maximum

TABLE I
DESIGN POINT GOALS FOR THE GaN/CMOS BUCK CONVERTER PROTOTYPE, AND SWITCH LOSS PARAMETERS

Converter	Number of phases	8
	Conversion ratio D	0.125
	Total converter (load) current	3 A
	Phase current	375 mA
	Input voltage	20 V
	Output voltage	2.5 V
GaN	On-state resistance $R_{DS(on)}$	3.47 $\Omega \cdot \text{mm}$
	Input capacitance C_{iss}	0.195 pF/mm
Si	On-state resistance $R_{DS(on)}$	9.07 $\Omega \cdot \text{mm}$
	Input capacitance C_{iss}	2.16 pF/mm

current I_{\max} . This assumes that the converter is operating on the boundary between continuous-conduction-mode and discontinuous-conduction-mode (CCM/DCM). $R_{DS(on)}$ is the low-side (LS) transistor ON-state resistance in a half-bridge topology, R is the width ratio of the high-side (HS) transistor to LS transistor, D is the conversion ratio, N is the number of phases, V_{GS} is the transistor gate drive voltage, C_{iss} is the transistor input (gate) capacitance, and f_s is the switching frequency. The converter efficiency (η_{sw}), as determined by switch losses alone, is then given by

$$\eta_{sw} = \frac{P_{\text{load}}}{P_{\text{load}} + P_{\text{cond}} + P_{\text{sw}}} \quad (3)$$

where $P_{\text{load}} = I_{\text{load}} \cdot V_{\text{load}}$ is the power delivered to the load.

Table I defines the specifications for the converter designed in this paper. Power-train-switch transistor parameters are also shown in Table I for both the GaN HEMTs used in this paper and typical 36-V LDMOS devices to be used as a point of comparison. Transistor switch loss parameters are derived from measurements of the fabricated GaN die employed here, and Silicon values are derived from a typical 36-V 0.13-m LDMOS transistor model. In both cases, converter operating parameters are identical, which justifies the assumption that for the purpose of the comparison, the converters are operating on the CCM/DCM boundary. The channel length is 150 nm for the GaN HEMTs and is 800 nm for the LDMOS devices. Fig. 3 shows the maximum achievable efficiency as a function of switching frequency for a converter meeting these specifications using either GaN HEMT or LDMOS switches. The high-to-low-side-transistor-width ratio R is selected such that the HS transistor is 1/D smaller than the LS transistor. In both cases, we choose transistor widths such that $P_{\text{cond}} + P_{\text{sw}}$ is minimized with the resulting switch widths noted in Fig. 3. The inferior switching performance of the LDMOS devices makes these devices very inefficient at the high switching frequencies characteristic of IVRs. In this comparison, it is important to note that the LDMOS transistors are rated for a breakdown voltage of only 36 V, while the GaN transistors employed here have a considerably higher breakdown voltage. In these GaN devices, lower breakdown voltage could have been traded off for even lower on-resistance, for example, by engineering the level of carbon-doping of the

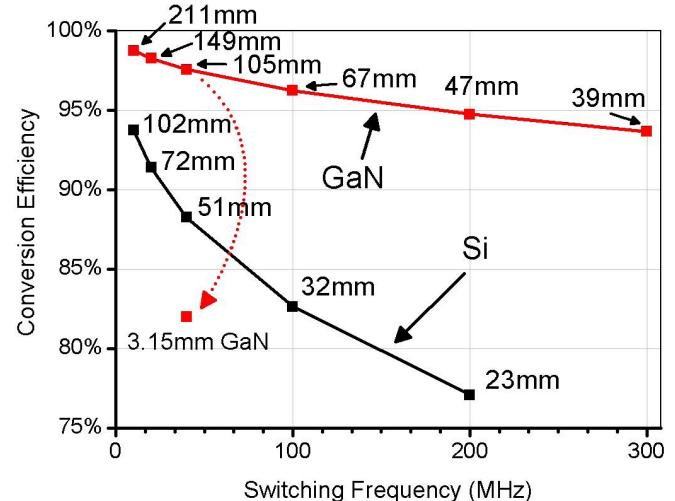
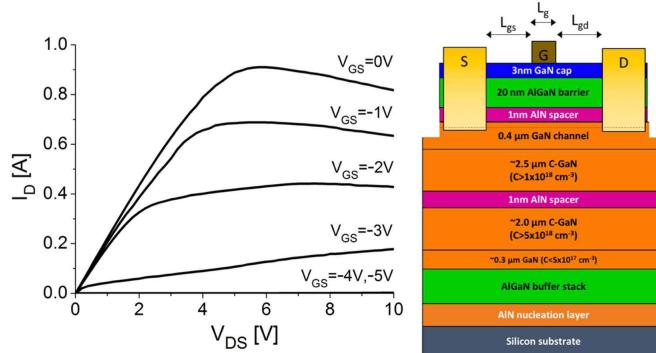


Fig. 3. Maximum achievable efficiency considering switches losses only. Results for a voltage converter utilizing GaN transistors and a voltage converter utilizing Si LDMOS transistors are shown using the transistor parameters defined in Table I. Data-point labels denote optimized LS transistor widths in millimeters. Also shown are the GaN switch sizing, switching frequency, and maximum efficiency achieved in the converter design designed and measured in this work.

GaN buffer layers [30]. Sizing down the HS switches, in general, reduces switching losses while increasing conduction losses. For the case of silicon LDMOS converters, efficiency is little changed, or even improved, by this down-sizing because improvement in switching losses effectively counters any increase in conduction losses. For GaN converters, which are dominated by conduction losses, efficiency is degraded by this down-sizing.

Reduction in the HS switch width, however, brings other advantages. While transistor widths can be chosen to maximize efficiency, as shown in Fig. 3, additional considerations go into the determination of switch sizing in practice. Availability of active area is an additional concern, and it is important to achieve target efficiencies without over-designing switches and increasing the overall cost. Switch utilization can be defined as the ratio of total load power P_{load} divided by the sum of active switches stress $S = \sum_j V_j I_j$, where V_j is the peak voltage applied across switch j in the circuit and I_j is the rms current through switch j [38, Ch. 6]. Motivated by this, we define a per-device utilization (U) as the average current delivered to the load through the transistor ($I_{D,\text{avg}}$) to the transistor's maximum drain current ($I_{D,\text{sat}}$): $U = I_{D,\text{avg}} / I_{D,\text{sat}}$. Here, a high per-device utilization implies that the load power is maximized relative to the maximum stress to which the device could be subjected.

In addition, the conversion ratio (D) is proportional to the ratio of $I_{D,\text{avg}}$ to the maximum current that the HS transistor is required to provide under all converter operation conditions ($I_{D,\text{max}}$). That is, $D \propto I_{D,\text{avg}} / I_{D,\text{max}} = U \cdot (I_{D,\text{sat}} / I_{D,\text{max}})$ [39]. Maximizing U for a given D would require maximizing transistors stress by minimizing $I_{D,\text{sat}}$. In this paper, we set the LS transistor width to 3.15 mm to balance efficiency and utilization. The HS switch, which should have been set 1/D times smaller, was instead set

Fig. 4. $I-V$ curve and GaN HEMT structure.

to the same width in this implementation ($R = 1$). This sizing results in U of 0.42 and converter power density of 0.55 W/mm^2 , which includes switches and all of the driver circuitry, but excludes any passives. These transistor widths limit the achievable converter efficiency due to switches losses (which at 40 MHz frequency are dominated by switches conduction losses) to approximately 82% as noted on Fig. 3. If active device area is not a concern, choosing an optimal width of 105 mm (at $R = 1$) allows the converter efficiency to be as high as 98%, although the output power density would be only 0.017 W/mm^2 with a U of only 0.014. If instead we sized down the HS switches, setting $R = 1/D$, power density would have improved to 0.032 W/mm^2 and the U would have improved to 0.026. The additional conduction losses associated with the smaller HS switch, however, would have resulted in a slight decrease in efficiency to 97%. Similarly, the data points on Fig. 3 are generally characterized by low utilization values, as transistor widths are chosen to optimize the efficiency, although at higher frequencies switches utilization increases as the efficiency-optimized widths are lower.

III. HYBRID CONVERTER DESIGN

Sixteen depletion-mode AlGaN/GaN multi-fingered HEMTs were fabricated on a single 1-mm-by-2-mm chiplet with 150-nm gate lengths and 3.15-mm gate widths. The epitaxial structure (Fig. 4) was grown on a 200-mm Si substrate. The individual transistors are isolated through mesa etching and feature Ti/Al/Ni/Au source-drain ohmic contacts with Ni/Au Schottky contact gates. Plasma-enhanced-chemical-vapor-deposited silicon nitride serves as the passivation layer. A Ti/Al layer serves to provide both the multi-finger interconnects and the interconnection pads. A single device displays an approximate gate capacitance C_g of 0.61 pF (capacitance per transistor length of 0.195 pF/mm and area-normalized capacitance of 2.6 nF/cm^2) and a maximum R_{ON} of 1.4Ω .

The die-attach processes used to mate the GaN chiplet to the CMOS die involves two steps. First, target aluminum pads on the 2-mm \times 4-mm CMOS chip are thermosonically bonded with Au bumps. Then, dual-heated 260°C Au–Au thermocompression face-bonding is used to form the contacts to matching Au finished pads on the smaller GaN die, as shown in Fig. 5. An image of an assembled converter can be seen

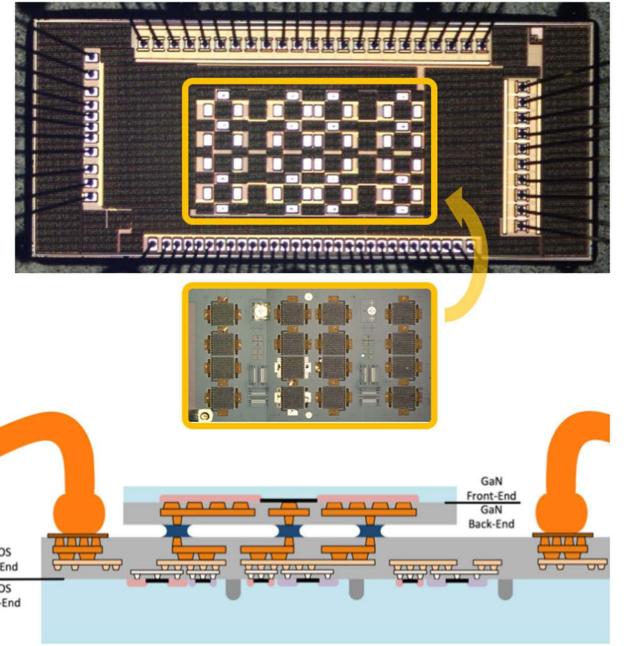


Fig. 5. Annotated micrograph of silicon die (top), GaN die (middle), and Au–Au thermocompression illustration (bottom).



Fig. 6. Image of assembled hybrid converter of GaN chiplet on CMOS die (left) and section of the prototype PCB (right) showing converter socket in the center and inductors above.

in Fig. 6. The inductors in the demonstrator prototype are implemented as on-board discrete 150-nH air-core inductors (Coilcraft P/N 1812SMS-R15JLB), but fully integrated IVRs that take advantage of the high switching frequencies enabled by the GaN switches will ultimately pursue on-chip inductor technologies [40].

The circuit topology for this hybrid GaN/CMOS converter is shown in Fig. 7. A variable synchronous pulsewidth-modulated (PWM) signal generation block is implemented to create eight evenly distributed phase-shifted signals for the eight converter phases (Fig. 8) using eight identical digitally controlled delay line (DCDL) elements. Generating each phase signal using a delay element from a previous phase guarantees robust matching of the multiphase currents. Each DCDL includes a four-bit fine-delay element (8-ns maximum delay, 500-ps resolution) and an eight-bit coarse-delay element (1- μs maximum delay, 4-ns resolution), enabling switching-frequency operation in the range between 1 and 200 MHz, and allowing a granular 6-bit resolution around the frequency

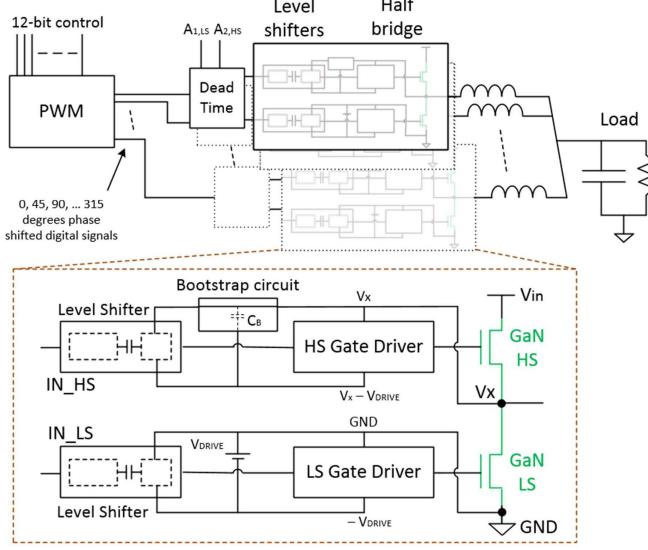


Fig. 7. Overall block diagram of the converter. Inset: half-bridge block diagram with drivers supply voltages annotated and capacitively coupled level-shifters.

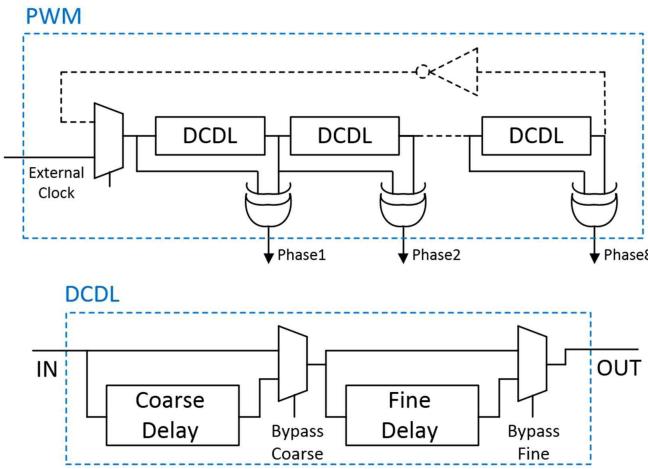


Fig. 8. Top: PWM block diagram with external clock input selection, external or autonomous feed. Bottom: DCDL block diagram.

in which the converter operates (20–40 MHz). Current-starved buffers serve as fine-delay elements, and minimum-sized buffers with sized capacitive loads serve to realize the coarse element as shown in Fig. 9. An adjustable dead-time (Fig. 10) delay module allows for fine-tuning adjustment of the duty cycle and of the dead-time between the HS switch and LS switch turn-ON times (minimizing shoot-through current in the half-bridge). The half-bridge conversion ratio is set through off-chip control of the digital PWM lines and the dead-time module analog lines.

Driving the depletion-mode n-type GaN HEMTs from 5-V tolerant CMOS devices is a key design consideration. The HS switch driving circuitry needs to follow the source of the HS GaN switch, which is tied to the switching node V_X as shown in the inset of Fig. 7. This node alternates between 0 V and the ground-referenced 20-V input voltage at the system switching frequency.

To address this, a floating bootstrapping capacitor C_B is used to provide the V_{drive} supply for the HS gate-driver. The bootstrapping capacitor and circuit are shown in Fig. 11. When V_X is pulled up to the converter input voltage by the HS switch, the diode turns on to charge C_B from the switching node itself, while $V_{in} - V_{drive}$ is supplied externally in this prototype. The diode and bootstrapping capacitor value (10 pF) are designed such that in steady state, the voltage over C_B remains at V_{drive} and the voltage droop during a single switching cycle is negligible. Since charging the bootstrap capacitor occurs only after the converter begins switching, startup charging is accomplished with a 1-MΩ resistor, which guarantees that the current through the resistor under normal operating conditions remains negligible, while achieving startup delays below 100 μs. Shunt regulators do not allow the floating voltage domain to charge up to voltages higher than 5 V, preventing oxide-breakdown failure events if the converter does not start switching immediately upon power-up.

IV. CAPACITIVE-COUPLING-ISOLATED LEVEL SHIFTER

Key to interfacing CMOS to high-voltage GaN devices is the challenge in level-shifting the 0–1.8-V controller signals to a range where they will be able to control the gate-drivers in the floating supply domains, as shown in the inset of Fig. 7. Referenced to the system ground, the HS driver supply transitions between $-V_{drive}$ and 0 V (when $V_X = 0$ V) and 20 V – V_{drive} and 20 V (when $V_X = 20$ V, the input voltage) synchronously with V_X . The LS driver operates between $-V_{drive}$ and 0 V, utilizing the same level shifter for HS/LS symmetry. Fig. 12 (left and right) shows the level shifter circuit, highlighting the pre-coupling fixed supply domains and post-coupling floating supply domain, respectively, isolated through identical high-voltage-tolerant coupling capacitors C_I .

The level shifting is performed in stages. First, in the pre-coupling fixed domain (see the left inset of Fig. 12), the 0- to 1.8-V signal is converted to a 0- to 5-V signal using a standard cascode voltage switch logic level shifter. This resulting signal is buffered and driven across the isolation capacitors C_I , producing differential voltage pulses on latch nodes D_1 and D_2 in the floating supply domain (see the right inset of Fig. 12) of magnitude

$$V_{pulse,cc} = 5 \text{ V} \cdot \frac{C_I}{C_I + C_D} \quad (4)$$

where C_I is the capacitance of the isolation capacitors and C_D is the capacitance of node D_1 or D_2 . The latch switches appropriately when the amplitude of the pulse is sufficient to get both nodes D_1 and D_2 beyond the metastable point of the latch ($V_{drive}/2$), as shown in Fig. 13(a).

For the HS level-shifter, common-mode pulses are also induced on D_1 and D_2 upon transitions of V_X , as shown in Fig. 14(a). In addition to common-mode rejection at the latch, additional logic and an additional latch, shown in Fig. 12, serve to further reject those false trigger (FT) events.

In order to tolerate 20 V, the C_I are implemented using back-end vertical natural capacitors with a nominal $C_I = 82$ fF, which unfortunately proved to have a die-to-die 3σ variability of 31%. This affects proper switching of

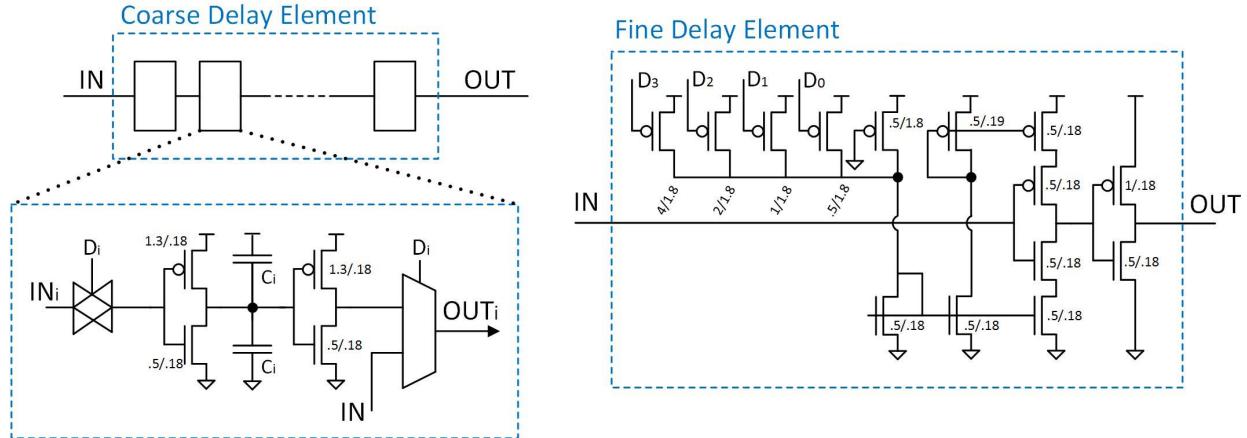


Fig. 9. Left: coarse delay element with 8-bit weighted capacitor-loaded buffers. Right: current-starved 4-bit fine delay element.

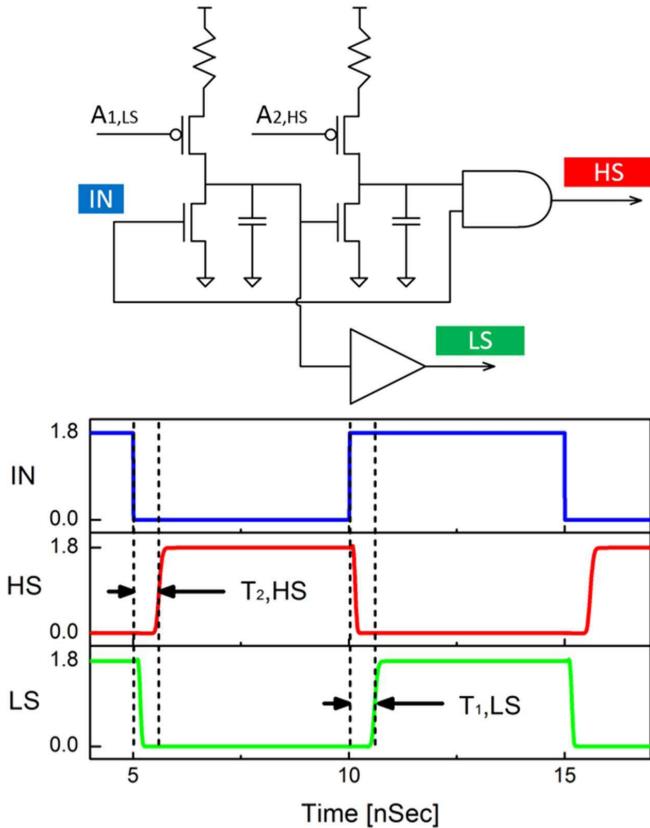


Fig. 10. Top: adjustable delay module sets the dead-time between the ON state of the HS and LS transistors to minimize shoot-through. Bottom: simulation result.

the level-shifter latch. Fig. 13(b) demonstrates that with a 3σ -worst-case magnitude for C_I of 56 fF, $V_{pulse,cc}$ is of insufficient magnitude to switch the latch. Increasing the nominal design value of C_I is a possible way to overcome these shortcomings, but increasing C_I also increases $T_{recovery}$, the time it takes the nodes D_1 and D_2 to recover from an FT event, which limits the maximum practical operating frequency of the level shifter and, consequently, the overall switching frequency of the converter. Fig. 14(b) shows an

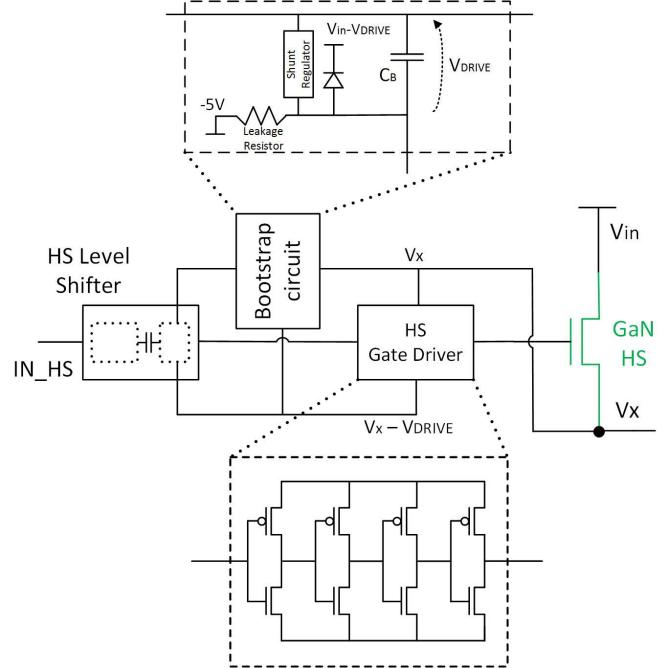


Fig. 11. Circuit of the HS NMOS GaN transistor driver with bootstrapping circuit (top inset) and gate driver power train (bottom inset).

excessive long $T_{recovery}$ in the case that C_I is increased to 164 fF. At this value of C_I , the switching frequency of the 12:1 converter is limited to $f_{max} = 1/(D \cdot T_{S,min}) \cong 10$ MHz, since $T_{S,min}$ is required to be greater than $T_{recovery} \cong 8$ ns.

V_{drive} can be reduced to help with latch switching at lower than expected values of C_I , effectively lowering the latch switch point. However, this increases latency through the level shifter, reducing the achievable switching frequencies. In addition, since V_{drive} is also used for the gate drivers, lowering it reduces the turn-off voltage for the GaN switches, leading to increased off-state leakage currents in the switches.

V. EXPERIMENTAL RESULTS

CMOS and GaN dies were tested individually before assembly. GaN device yield combined with C_I -variability

Level Shifter

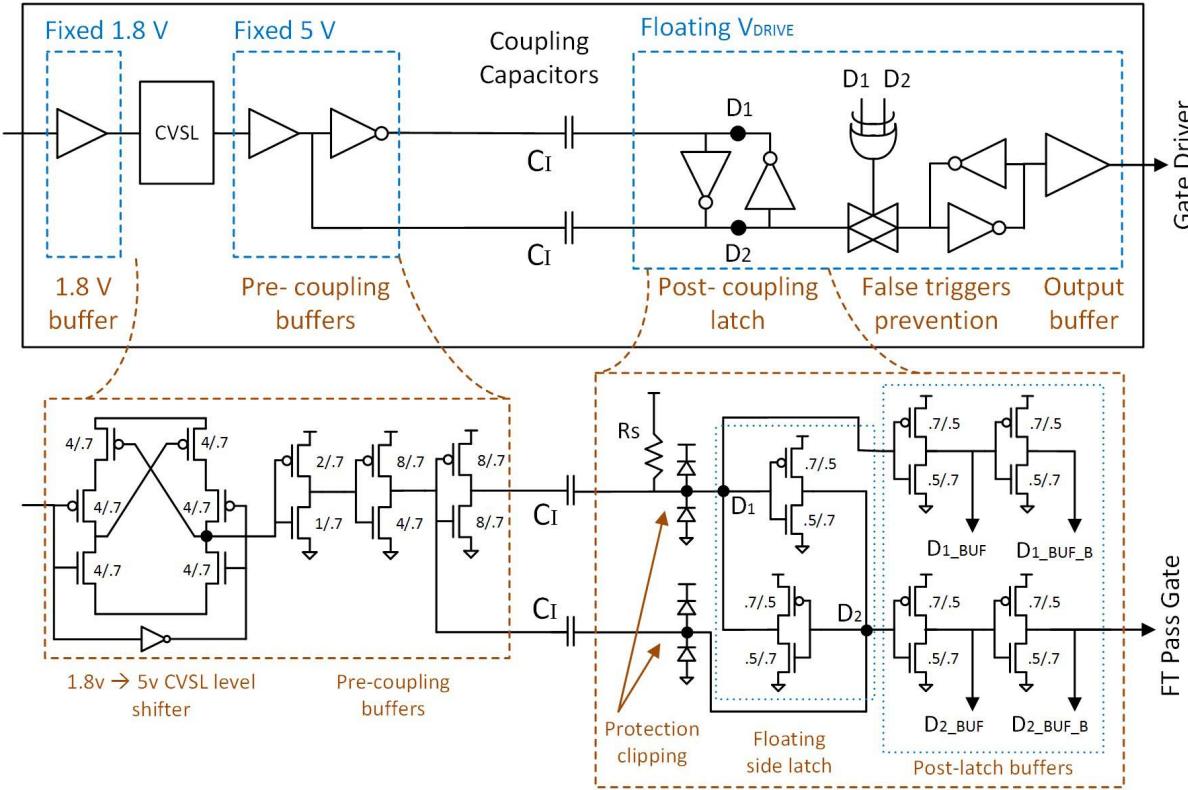


Fig. 12. Block diagram of the capacitive-coupling-isolated level shifter.

TABLE II
SUMMARY OF CONVERTER RESULTS

Measurement	1	2	3	4
V_{in}	12 V	8 V	20 V	16 V
V_{out}	1 V	1 V	2.5 V	1 V
Conversion Ratio	12:1	8:1	8:1	16:1
Frequency	40 MHz	40 MHz	40 MHz	20 MHz
# of Phases	3 phases	3 phases	1 phases	7 phases
Max load current	204mA	198mA	30mA	825mA
Max efficiency	68% at 50mA	76% at 51mA	65% at 30mA	62% at 104mA
V_{drive}	>3.5 V	>3.5 V	=5 V	>2.5 V

issues in the level-shifter prevented certain phases from being functional, depending on operating conditions. Missing or disconnected gate fingers constituted the biggest yield detractor for the GaN chiplets. Each GaN chiplet has 16 transistors (HS and LS for each of eight phases) and each transistor has 18 gate fingers for a total of 288 gate fingers. Since the transistors are depletion mode, a faulty gate finger results in a normally-on channel, shorting the input rails under regular converter switching conditions, making that phase of the converter inoperable.

Table II shows a summary of measurements results from four different combinations of input and output voltages, switching frequencies, the number of converter phases, and V_{drive} values. If C_1 -variability was too high for a specific level-shifter to function correctly with the default V_{drive} value

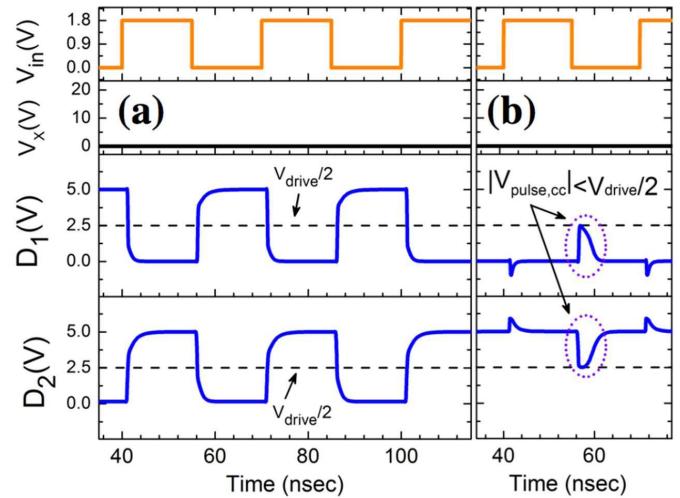


Fig. 13. Capacitive-coupled-isolated level shifter latch nodes responses. (a) Correct switching for $C_1 = 82 \text{ fF}$. (b) Failure for $C_1 = 56 \text{ fF}$.

of 5 V, V_{drive} is reduced until level-shifter functionality is restored. In many cases, the required V_{drive} was substantially lower than 5 V as noted in Table II. For Measurement 4, this drove the switching frequency down to 20 MHz.

Fig. 15 shows the efficiency as a function of output load current for a three-phase configuration operating at a switching frequency of 40 MHz and the conditions noted in Table II for Measurements 1 and 2. 76% efficiency are demonstrated for

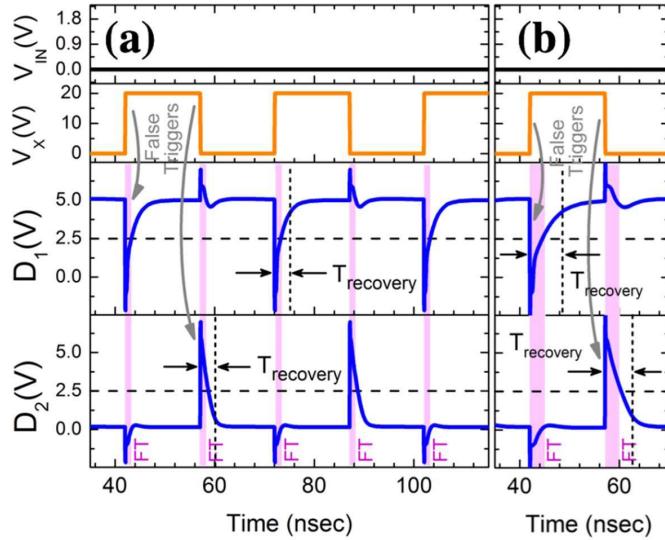


Fig. 14. Capacitive-coupling-isolated level shifter latch nodes responses. (a) FT $T_{recovery}$ for $C_I = 82$ fF. (b) FT increased $T_{recovery}$ failure for $C_I = 164$ fF.

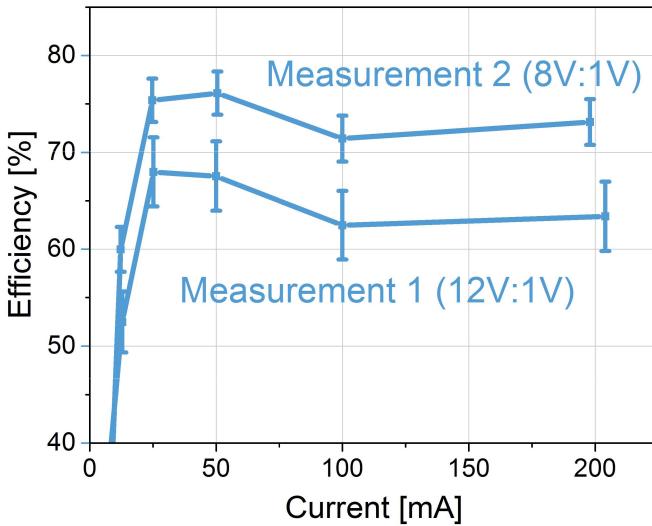


Fig. 15. Converter efficiency as a function of output load current for three-phase 40-MHz operation at the conditions noted as Measurements 1 and 2 in Table II. The error bars represent invalidity due to instruments inaccuracy and measurement noise.

8:1 V conversion and 68% for 16:1 V as shown in Fig. 15 for load currents in excess of 25 mA. Lower efficiencies are achieved for load currents below 25 mA as losses that do not scale with load current (such as dynamic switching losses) dominate. Fig. 16 shows the per-phase converter efficiency as a function of output load current per phase for all four measurements conditions noted in Table II. Efficiencies all drop off substantially for per-phase load currents less than approximately 8 mA as efficiency measurement includes all power sources provided to the converter.

The peak measured power density is 0.55 W/mm². The entire silicon and GaN front ends (dies) were included in the calculation of converter area, excluding the area consumed by

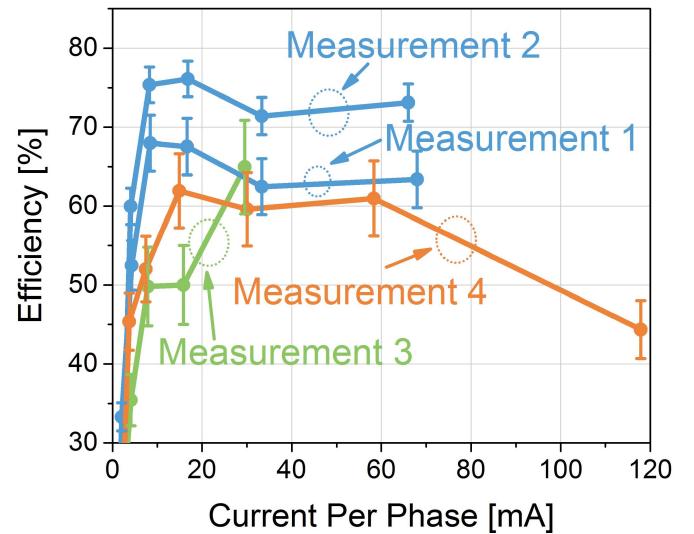


Fig. 16. Per-phase converter efficiency as a function of output load current per phase for all four measurements conditions noted in Table II. The error bars represent invalidity due to instruments inaccuracy and measurement noise.

passives. Overall CMOS propagation delay, from the PWM output to GaN gate input, including dead time, was measured to be 3.8 ns (4.8 ns) for low-to-high (high-to-low) transitions, significantly faster than a representative prior design using GaN devices and CMOS gate drivers [41] for which these delays were on the order of 8.2 ns (9.7 ns). Such low propagation delay time improves efficiency due to faster switching characteristics and allows lower $D \cdot T_S$ values to be achieved, which is necessary in order to achieve higher conversion ratios.

VI. CONCLUSION

By exploiting face-to-face bonding of GaN HEMTs and CMOS, we demonstrate the design of a prototype 40-MHz hybrid CMOS/GaN voltage converter. While input voltages of up to 20 V are supported and conversion ratio as high as 16:1 V are demonstrated, higher input voltages would certainly be supported by this circuit and technology architecture. Converters like these should allow single-step IVRs from high-voltage dc distributions, replacing significantly less efficient and more complicated multi-step conversion schemes. Switching frequencies for these converters, which can ultimately scale into the hundreds of megahertz, will also allow inductor values to be reduced to the point that integrated inductor technologies [40] could be exploited in these designs.

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