Virtuoso® Schematic Editor Tutorial

Product Version 5.1.41
July 2007

Cadence Design Systems, Inc., 555 River Oaks Parkway, San Jose, CA 95134, USA

Contents

Preface

The Virtuoso® Schematic Editor is a design entry tool that supports the work of logic and circuit design engineers. Physical layout designers and printed circuit board designers can use the information as background material to support their work.

The preface discusses the following:

Related Documents

The schematic editor is often used with other Cadence® products or requires knowledge of special languages such as the Cadence SKILL language. The following documents give you more information about these tools and languages, but in general for this tutorial, you will not need to refer to them.

- The *Cadence Design Framework II User Guide* provides information if you are not familiar with Cadence terms and starting your system.
- The *Cadence Application Infrastructure User Guide* provides additional information about the architecture.
- The *Virtuoso Schematic Editor User Guide* describes how to create and check schematics and symbols.
- The *Virtuoso Inherited Connections Flow Guide* describes how to use inherited connections and net expressions with various Cadence tools in the design flow.
- The *Virtuoso Schematic Editor SKILL Functions Reference* is for users who customize the standar
- d product.
- The *Library Manager User Guide* explains how to open or create cellviews from the Library Manager.
- The *Virtuoso Verilog-XL Environment Reference Manual* and the *Virtuoso Verilog-XL Environment User Guide* describe how to use the schematic editor with Verilog® HDL. The manual is intended for integrated circuit designers who are using the Verilog-XL logic simulator to verify the logic of their designs.
- The *Virtuoso VHDL Environment User Guide* describes how to use the schematic editor with VHDL.

Typographic and Syntax Conventions

This section describes typographic and syntax conventions used in this manual.

`text`	Indicates text you must type exactly as it is presented.
`z_argument`	Indicates text that you must replace with an appropriate argument. The prefix (in this case, *`z_`*) indicates the data type the argument can accept. Do not type the data type or underscore.
`[ ]`	Denotes optional arguments. When used with vertical bars, they enclose a list of choices from which you can choose one.
`{ }`	Used with vertical bars and encloses a list of choices from which you must choose one.
`|`	Separates a choice of options.
…	Indicates that you can repeat the previous argument.
=>	Precedes the values returned by a Cadence® SKILL language function.
/	Separates the possible values that can be returned by a Cadence SKILL language function.
text	Indicates names of manuals, menu commands, form buttons, and form fields.

The language requires many characters not included in the preceding list. You must type these characters exactly as they are shown in the syntax.

1

Installing the Tutorial Database

Getting Started with the Tutorial

Installing the tutorial database consists of the following procedures:

1. Making a Copy of the Tutorial Data on page 12
2. Starting the Cadence Software on page 13.
3. Setting the Paths to the Tutorial Libraries on page 14.

Making a Copy of the Tutorial Data

Important

Before you begin to work on this tutorial, you must take a copy of the tutorial data to ensure that the original data is not over-written and cannot be used by future users.

➤ The tutorial data should be located in:

`<your_install_dir>/tools/dfII/samples/tutorials/composer`

You should copy this to another directory, for example:

```
cp -r <your_install_dir>/tools/dfII/samples/tutorials/composer ~/comptut/
```

Once copied, the `~/comptut` should contain the following directories:

```
drwxr-xr-x   7 gblack   daemon      4096 Jun  2 10:37 .
drwxrwxr-x   3 gblack   daemon      4096 Jun  2 10:37 ..
-rwxr-xr-x   1 gblack   daemon      6470 Jun  2 10:37 .cdsinit
-rw-r--r--   1 gblack   daemon       872 Jun  2 10:37 .cshrc
-rw-r--r--   1 gblack   daemon        28 Jun  2 10:37 .datestamp
-rw-r--r--   1 gblack   daemon      1597 Jun  2 10:37 .login
-rw-r--r--   1 gblack   daemon      2303 Jun  2 10:37 .mwmrc
-rwxr-xr-x   1 gblack   daemon       339 Jun  2 10:37 .openwin-init
-rw-r--r--   1 gblack   daemon      1529 Jun  2 10:37 .openwin-menu
-rw-r--r--   1 gblack   daemon        78 Jun  2 10:37 .X11
-rw-r--r--   1 gblack   daemon     16048 Jun  2 10:37 .Xdefaults
-rwxr-xr-x   1 gblack   daemon       441 Jun  2 10:37 .xinitrc
-rwxr-xr-x   1 gblack   daemon       441 Jun  2 10:37 .xinitrcmwm
-rwxr-xr-x   1 gblack   daemon       446 Jun  2 10:37 .xinitrcolwm
-rw-r--r--   1 gblack   daemon         0 Jun  2 10:37 cds.lib
drwxr-xr-x   6 gblack   daemon      4096 Jun  2 10:37 dotfiles
drwxr-xr-x   5 gblack   daemon      4096 Jun  2 10:37 master
-rwxr-xr-x   1 gblack   daemon      7906 Jun  2 10:37 restart
-rw-r--r--   1 gblack   daemon       720 Jun  2 10:37 template.bom
drwxr-xr-x   5 gblack   daemon      4096 Jun  2 10:37 TTL_tutor
drwxr-xr-x   2 gblack   daemon      4096 Jun  2 10:37 tutorial
-rw-r--r--   1 gblack   daemon       481 Jun  2 10:37 tutorial.mech
drwxr-xr-x   3 gblack   daemon      4096 Jun  2 10:37 user_ASIC
```

Starting the Cadence Software

1. Ensure that you are in the tutorial directory, for example: `~/comptut`
2. Start the Cadence software from a terminal window by typing *one* of the following commands:

   ```
   icde &
   icds &
   icms &
   msfb &
   icfb &
   ```

   Note: In this tutorial, all examples are illustrated with the `icfb` display. The ampersand (&) puts the command in the background so you can continue to use the `xterm` window for other commands.

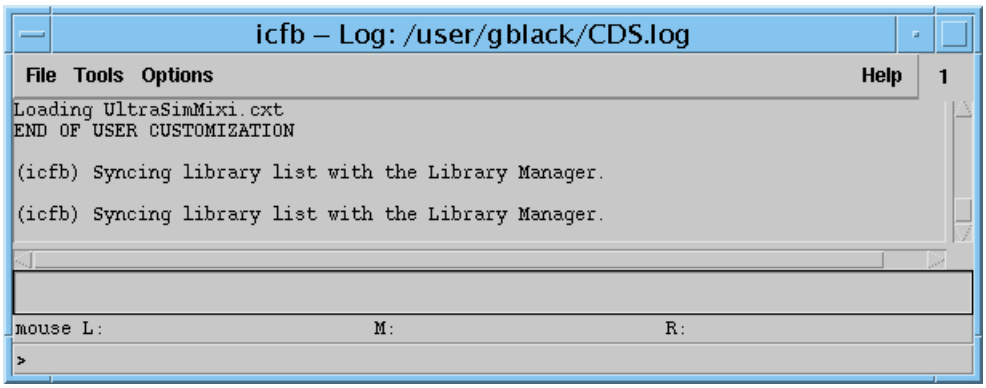


Figure 1-1 icfb Log Window

Setting the Paths to the Tutorial Libraries

To set the paths for the eight tutorial libraries, do the following:

1. From the CIW, choose *Tools – Library Path Editor*.

   The Library Path Editor form appears:

2. Enter the default paths of the eight tutorial libraries in the Library Path Editor form as follows:

```
basic /your_install_dir/tools/dfII/etc/cdslib/basic
US_8ths /your_install_dir/tools/dfII/etc/cdslib/sheets/US_8ths
analogLib /your_install_dir/tools/dfII/etc/cdslib/artist/analogLib
sample /your_install_dir/tools/dfII/samples/cdslib/sample
TTL_tutor /your_home_dir/comptut/TTL_tutor
master /your_home_dir/comptut/master
tutorial /your_home_dir/comptut/tutorial
user_ASIC /your_home_dir/comptut/user_ASIC
```

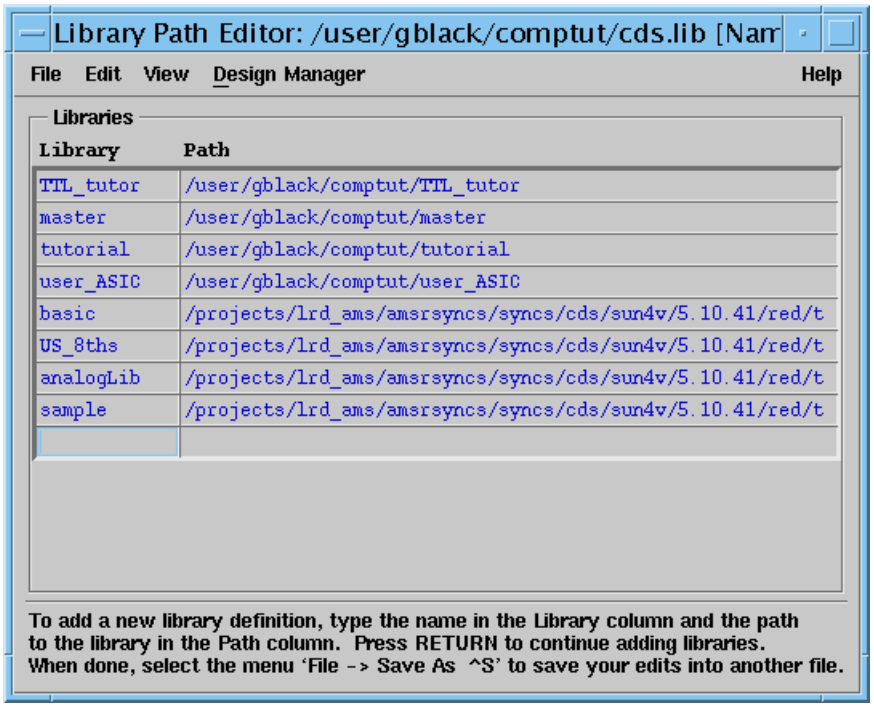


Figure 1-2 The Library Path Editor with Tutorial Libraries Added

Note: If the path displays in red in the Library Path Editor form, that indicates that the path is incorrect.

3. From the Library Path Editor form, choose *File – Save/Save As* and save the information in `~/comptut/cds.lib`.

About the Tutorial Libraries, Cells, and Cellviews

The tutorial libraries are described as follows:

`TTL_tutor`	Reference library supplied with this tutorial. Contains the standard TTL parts used in the tutorial design.
`US_8ths`	Reference library supplied with the Virtuoso® Schematic Editor software. Contains templates for page borders for schematics.
`basic`	Reference library supplied with the schematic editor software. Contains basic symbols, including ground and power.
`master`	Read-only design library. Contains copies of the designs used in this tutorial.
`sample`	Reference library supplied with the schematic editor software. Contains a sample collection of gates and other electronic circuitry.
`tutorial`	Design library in which you create your schematic.
`user_ASIC`	Reference library supplied with this tutorial. Contains the Arithmetic Logic Unit (ALU) used in the tutorial design.
`analogLib`	Reference library supplied with the schematic editor software. Contains the analog parts used in the analog design.

Cadence uses the term *library* to mean both reference libraries, which contain defined components for a specific technology, and design libraries, in which you create your own designs.

The master Cell Library

In the schematic editor software, designs are called *cells*. The `master` library contains three cells:

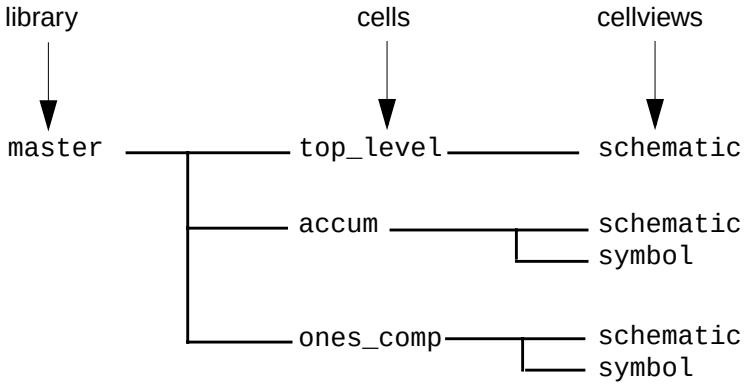
- The `accum` cell contains the accumulator used in the `top_level` schematic.
- The `ones_comp` cell contains the one's complement used in the `top_level` schematic.
- The `top_level` schematic contains the tutorial design, which is a simple processor.

Depending on its use, a cell can have multiple representations or views, such as a *symbol* or a *schematic*. For example:

- the `accum` cell appears as a symbol in the `top_level` schematic, and also has its own schematic. The `accum` symbol representation is called a *cellview.*

  Note: The `ones_comp` cell has the same cellviews (schematic and symbol) as the `accum` cell.

- The `top_level` cell has one cellview, which is the schematic view of the `top_level` schematic.



2

Getting Started with the Schematic Editor

Learning Objectives

In this chapter you will perform the following tasks:

Setting Tutorial Options

The options you set affect the schematics that you display. The options stay in effect until you exit the schematic editor software.

1. In the CIW, select *Options – User Preferences* to display the User Preferences form.

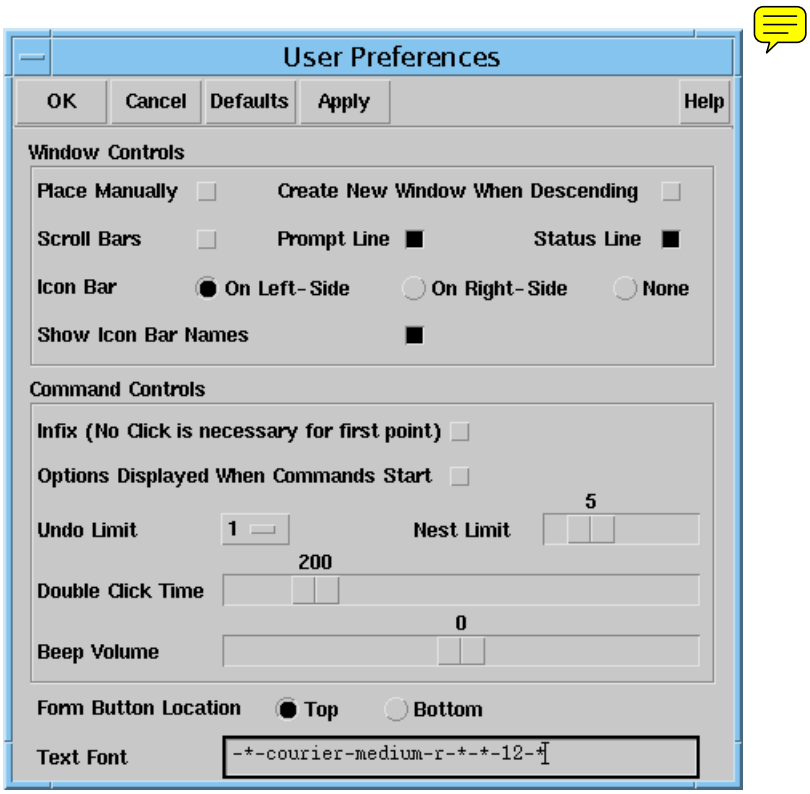


Figure 2-1 The User Preferences Form

2. Turn on the *Scroll Bars* button. The *Scroll Bars* button displays scroll bars on the schematic windows.
3. Turn on the *Infix* button. Turning on *Infix* limits the number of mouse clicks required to execute certain commands, as you will learn later in this chapter.
4. Click on the *Undo Limit* drop-down box and increase it to *10*. *Undo Limit* defines the number of previous commands that can be undone.

   Note: In OpenAccess: *Undo Limit* is a drop-down box with two values, *0* and *128*.
5. Click *OK*.

Opening the Schematic Window

To open a schematic window, do the following:

1. From the CIW, choose *File – Open.*

   The

   Open File form is displayed. From here, you can find and open any cellview, of any cell, that you have access to.

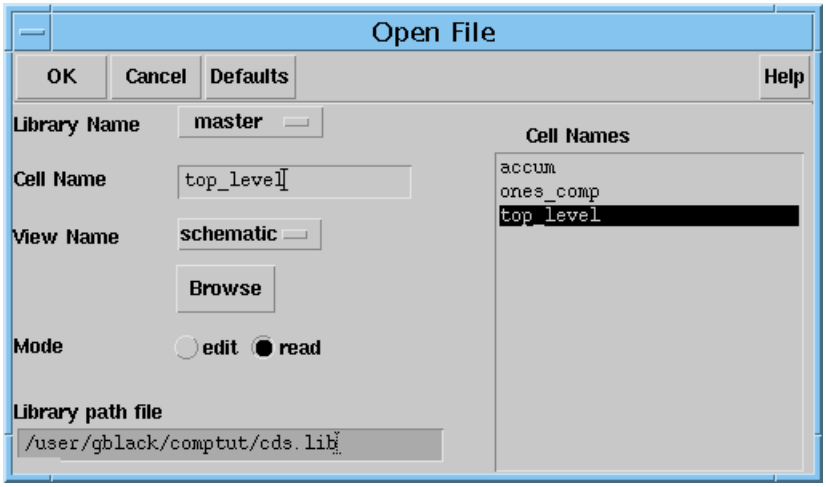


Figure 2-2 The Open File Form

2. In the *Library Name* cyclic field, choose `master`.

   The Open File form updates to display the contents of the `master` library.

3. In the *Cell Names* list box, click on `top_level`.

4. In the *View Name* cyclic field, choose `schematic`.

5. Set *Mode* to *read*.

   You must choose *read* because the `master` library is a read-only library.

6. Click *OK*.

   The Open File form closes. The `top_level` schematic appears.

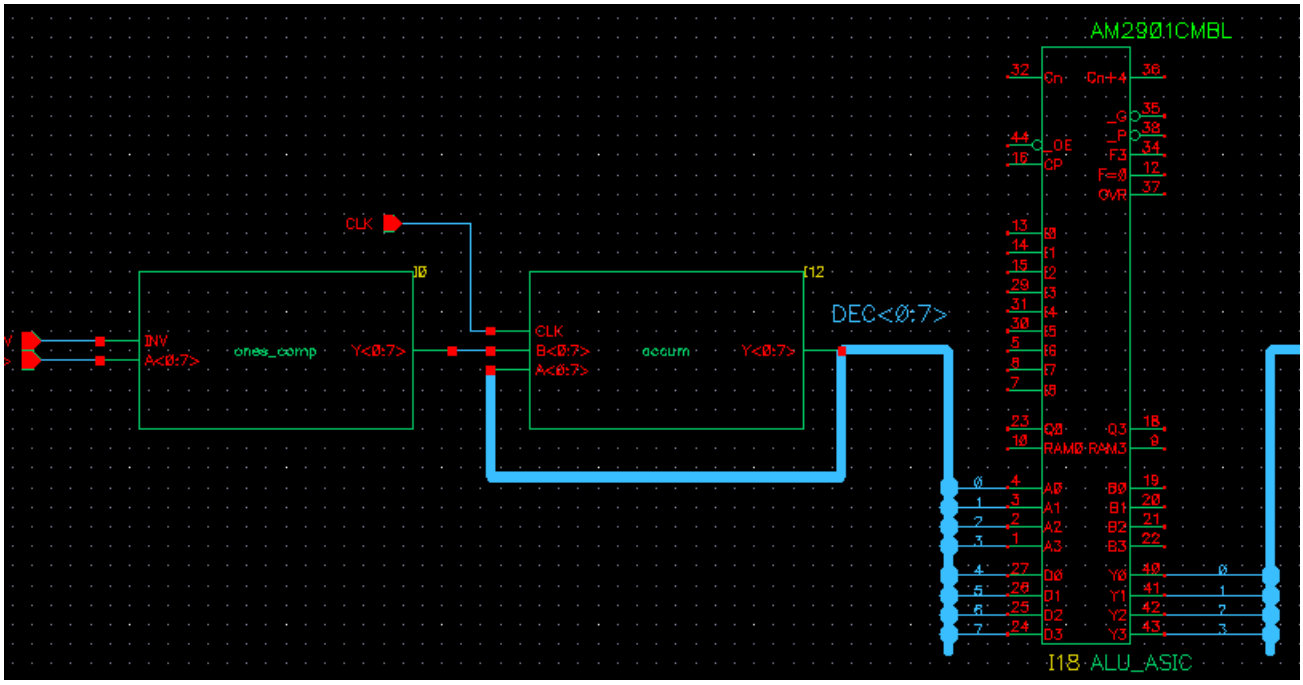


Figure 2-3 The top_level Schematic

Note: On the left-hand side of the schematic you can see the one's component instance, the centre section has the accumulator instance, and the right-hand side shows the `ALU_ASIC` instance.

Viewing the Schematic

➤ To inspect a design closer, so that you can read pin names, wire names, and so on, you can, choose *Window – Zoom – Zoom In By 2* from the schematic window.

The first instance, on the left, is named `ones_comp`.

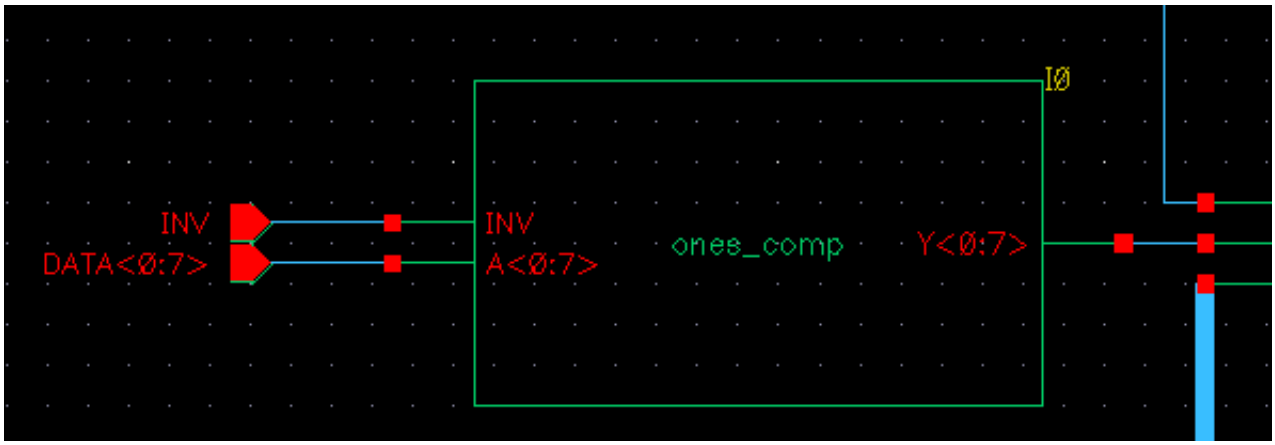


Figure 2-4 The ones_comp Instance

The second instance is named `accum`, and it has an output bus `DEC<0:7>`.

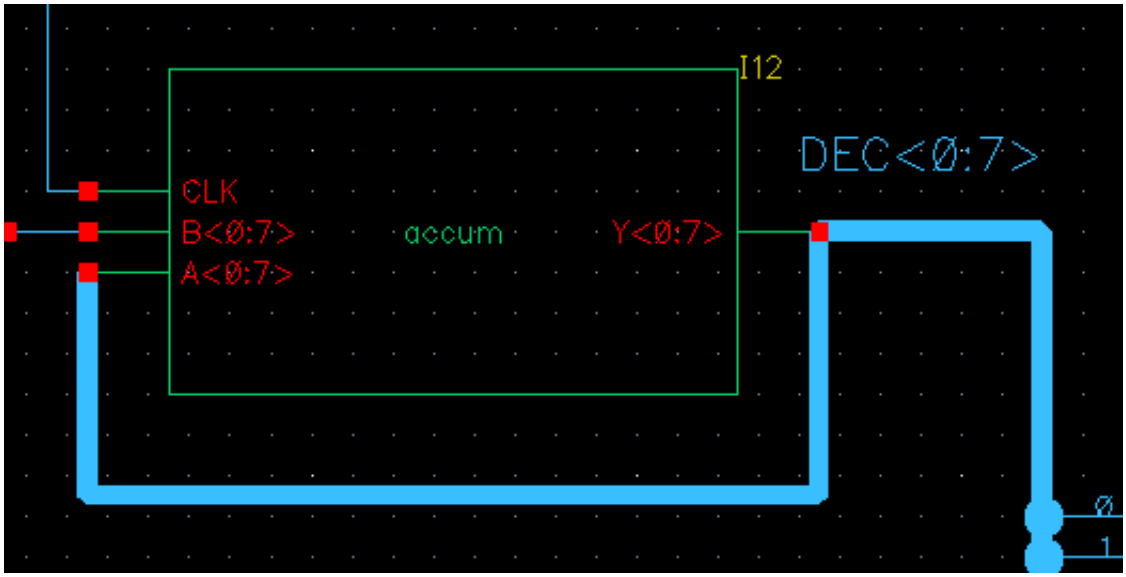


Figure 2-5 The accum Instance

The third instance is named `ALU_ASIC`, and it has an output bus `OUT<0:3>`.

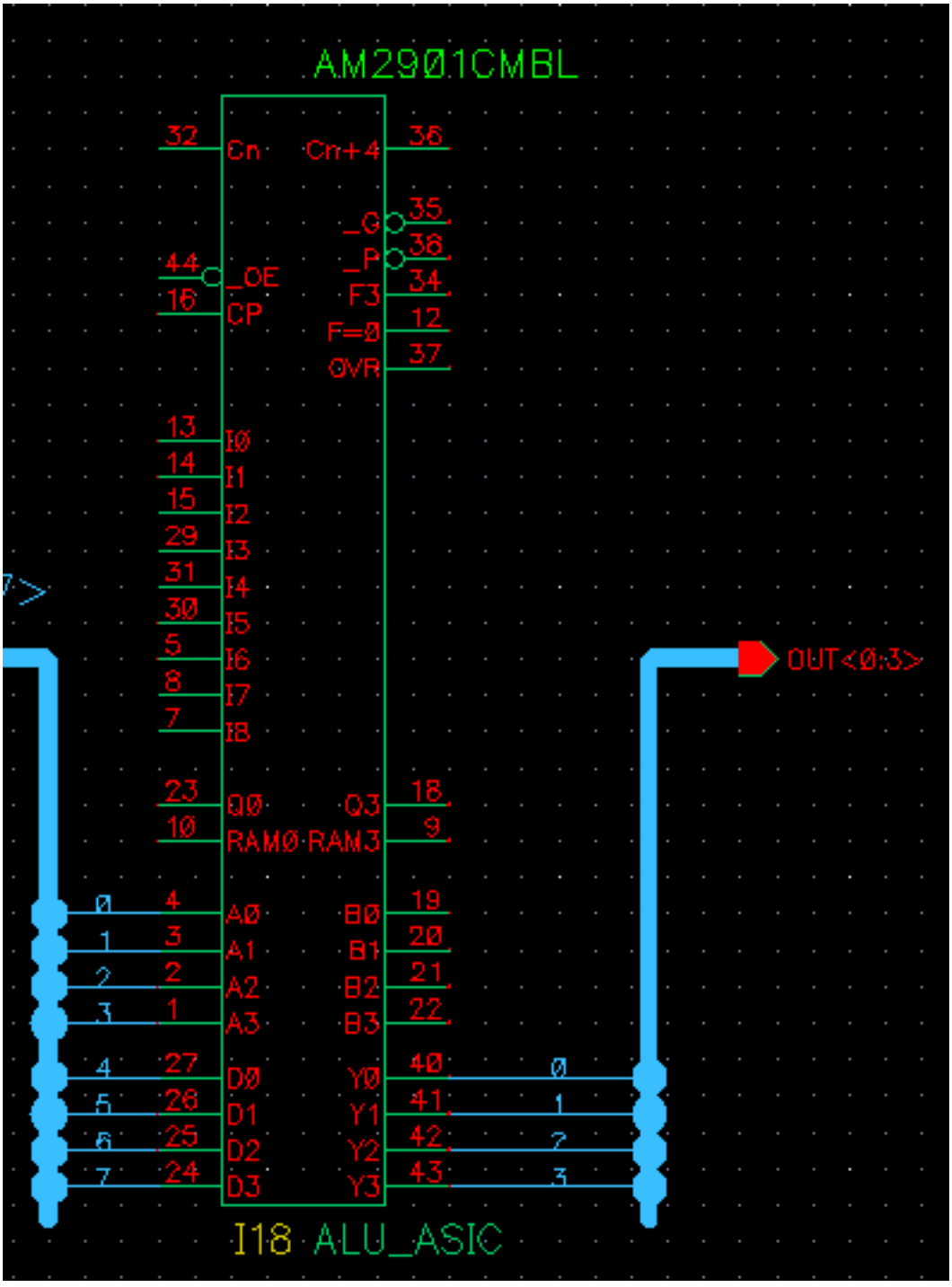


Figure 2-6 The ALU_ASIC Instance

Browsing the Schematic Hierarchy

The `top_level` cellview is the top schematic in this particular hierarchy.

In this section, you will descend one level to view another schematic in the hierarchy.

Moving Down the Schematic Hierarchy

To descend the hierarchy to view the `accum` cell, do the following:

1. Choose *Design – Hierarchy – Descend Read*.

   The status bar, at the bottom of the window, now prompts you to:

   `Point at instance to descend into.`

2. Click on the `accum` instance.

   The `accum` instance is selected when a box appears around it.

   The Descend form appears.

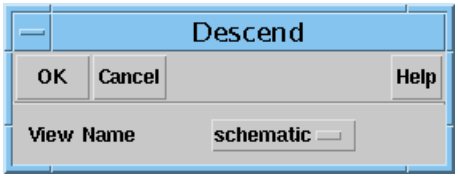
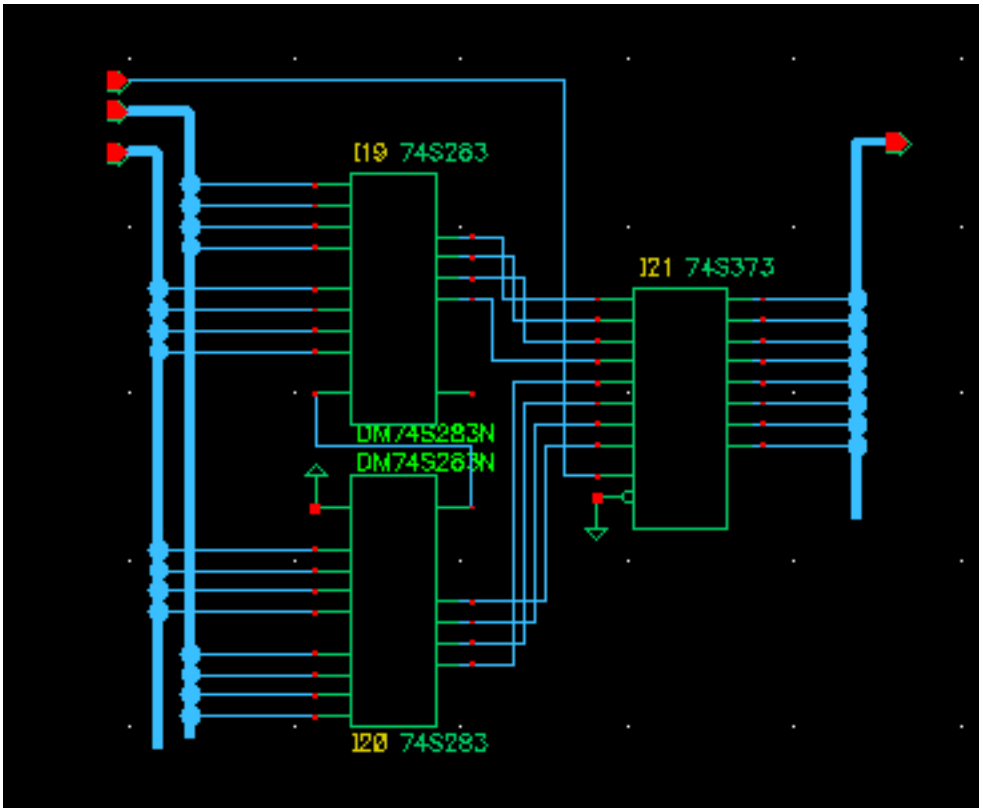


Figure 2-7 The Descend Form

3. In the *View Name* cyclic field, choose *schematic*.
4. Click *OK*.

   The schematic for the accumulator appears.



If you look at the accumulator instance, you will see that it contains:

- Two 4-bit adders (both 74S283), one below the other. The lower adder is upsidedown
- One 8-bit register (74S373)
- Nets or wires represented by thin lines
- Buses represented by the thick lines.

Moving Back Up the Schematic Hierarchy

To return to the top-level schematic:

1. Choose *Design – Hierarchy – Return To Top*. The `top_level` schematic reappears.
2. Choose *Window – Fit*. The Fit command fits the `top_level` schematic to the window, displaying the entire schematic.

Closing the Design and Quitting the Software

If you want to continue with the tutorial go to Creating Symbols and Pins on page 27.

Each time you close the schematic editor software, and quit the Cadence® software (using the CIW), the user preferences are reset to the default values.

If returning to this tutorial later, you must open the User Preferences form and restore the settings as discussed in Setting Tutorial Options on page 18.

To close the design, do the following:

➤ Choose *Window – Close*. 

To quit or edit the software, do the following:

➤ Choose *File – Exit*.

3

Creating Symbols and Pins

Learning Objectives

In this chapter, you will be performing the following tasks:

The top_level Schematic

Completing these learning objectives will lead to the creation of your own `top_level` schematic which will contain the following.

- A one's complement (`ones_comp`) module based on standard functions
- An accumulator (`accum`) based on standard functions
- An ALU (`ALU_ASIC`)
- Two buses (`DEC` and `OUT`), indicated by the thick lines, and nets

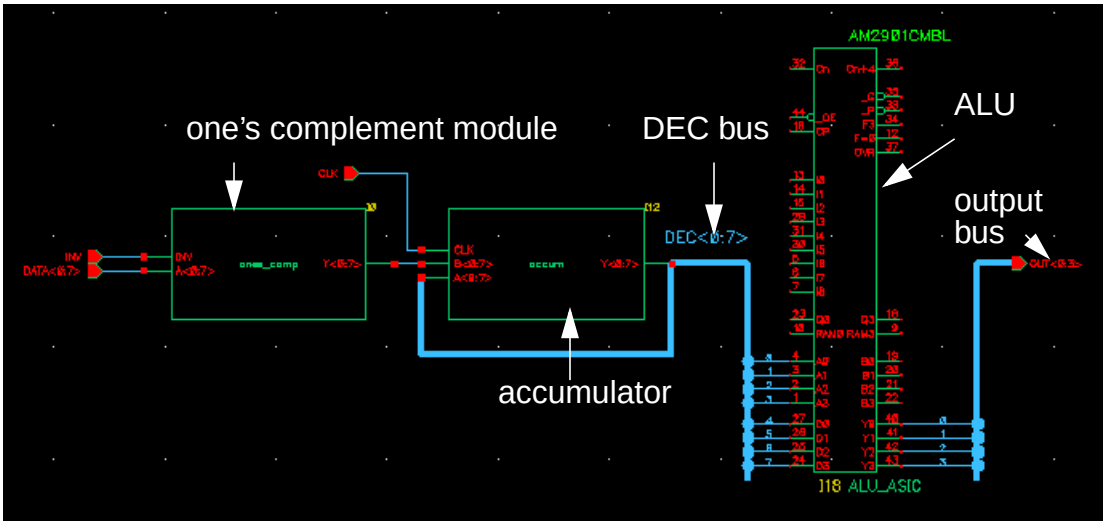


Figure 3-1 The top_level Schematic To Be Created

Creating a New Design

The first step in creating a schematic is to open a new design cell with a schematic cellview.

In the Virtuoso® Schematic Editor software, *cell* means the overall design and *cellview* means the representation of the design, such as the schematic or symbol representation.

Note: If you are continuing the tutorial from previous chapters, these options should already be set.

1. From the CIW, again choose *Options – User Preferences*.
2. Turn on the *Scroll Bars* button.
3. Turn on the *Infix* button.

   All the procedures in this tutorial assume that you have turned on *Infix.*
4. Move the *Undo Limit* slider control to 10.

   For OA Only: the *Undo Limit* option is a drop-down box with two values, 0 and 128.
5. Click *OK*.

Opening the top_level Design

In this section, you will create the new design cell and schematic cellview by opening a new design in the *tutorial* design library. The *tutorial* library already exists as part of the tutorial database.

1. From the CIW, choose *File – New – Cellview* to display the Create New File form.
2. In the *Library Name* cyclic field, choose *tutorial*.
3. In the *Cell Name* field, type `top_level`.
4. In the *View Name* field, type `schematic`.
5. In the *Tool* cyclic field, choose *Composer-Schematic*.
6. Click *OK*.

   A blank schematic window appears, ready for you to begin entering your design.

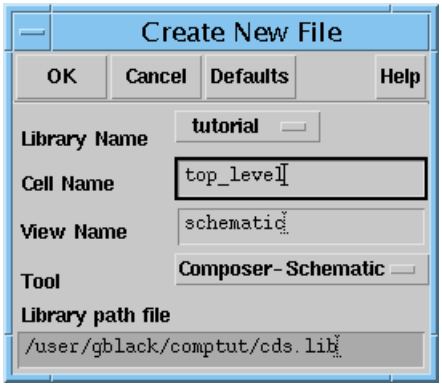


Figure 3-2 How the Create New File Form Should Be Completed

Placing the ALU Symbol

In this section, you place the symbol for the ALU in the schematic (the ALU symbol is supplied with the tutorial database).

1. From the schematic editing window, choose *Add – Instance* to display the Add Instance form.

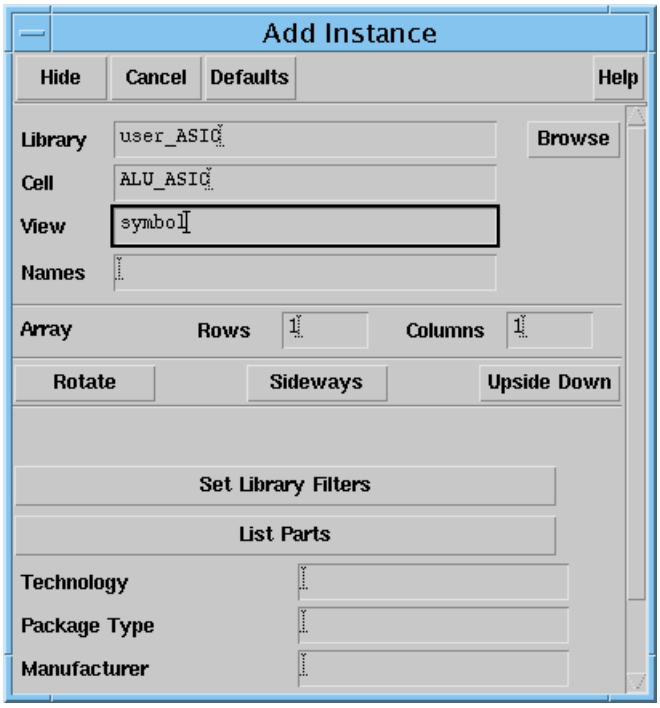


Figure 3-3 The Add Instance Form

2. In the *Library* field, type `user_ASIC`.
3. In the *Cell* field, type `ALU_ASIC`.
4. In the *View* field, type `symbol`.

   Note: You can also use the *Browse* button to assist you in entering the instance name.

5. Move the pointer onto the schematic editing window and you will notice that the ALU instance appears in the schematic window attached to the pointer.

6. Position the ALU instance on the right side of the design and click to place it.

   Note: When you place the ALU instance, it might be so large that it barely fits into the schematic window. To give yourself more room on the schematic, zoom out by choosing *Window – Zoom Out By 2*.

   Note: If necessary, refer to Figure 3-1 on page 28 for placement positioning.

7. Move the pointer again, and you will notice that the ALU instance continues to follow the pointer. This lets you continue to place copies of the same instance without having to start the command again.

8. Cancel the *Add – Instance* command by placing the pointer in the schematic window and pressing Esc.

9. Choose *Design – Save* to save your work.

Creating the One's Complement Symbol

You can create the one's complement symbol automatically, based on the symbol's primary input and output pins.

1. In the schematic window, choose *Design – Create Cellview – From Pin List.*

   The Cellview From Pin List form appears.

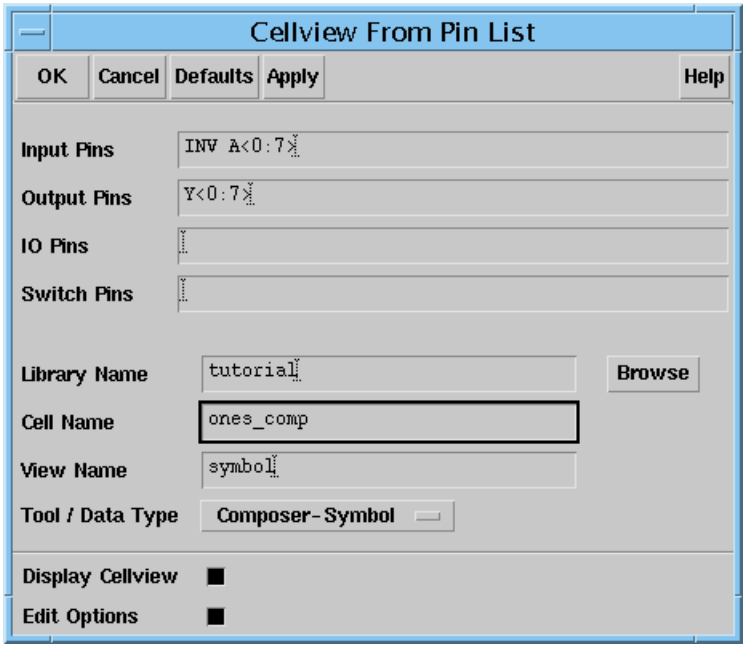


Figure 3-4 The Cellview from Pin List

2. In the *Input Pins* field, type `INV A<0:7>`.

   Note: Take care not to type a space between `A` and `<0:7>`. The name `A<0:7>` represents eight signals. Because `A<0:7>` represents multiple signals, it is called a *bus* pin.

3. In the *Output Pins* field, type `Y<0:7>`.

4. In the *Cell Name* field, type `ones_comp`.

5. Click *Apply*.

   The *Apply* button executes the command but does not cancel the form. (The *OK* button executes the command and cancels the form.) You want to keep the command active because you will be creating the accumulator symbol after you create the one's complement symbol.

The Symbol Generation Options form appears on top of the Cellview From Pin List form.

This form appears because the *Edit Options* button on the Cellview From Pin List form is *on* by default.

This form lets you specify graphic information for the symbol. Regardless of the order in which the pin names are entered into the Cellview From Pin List form, the Symbol Generation Options form presents the pin names in alphabetical order.

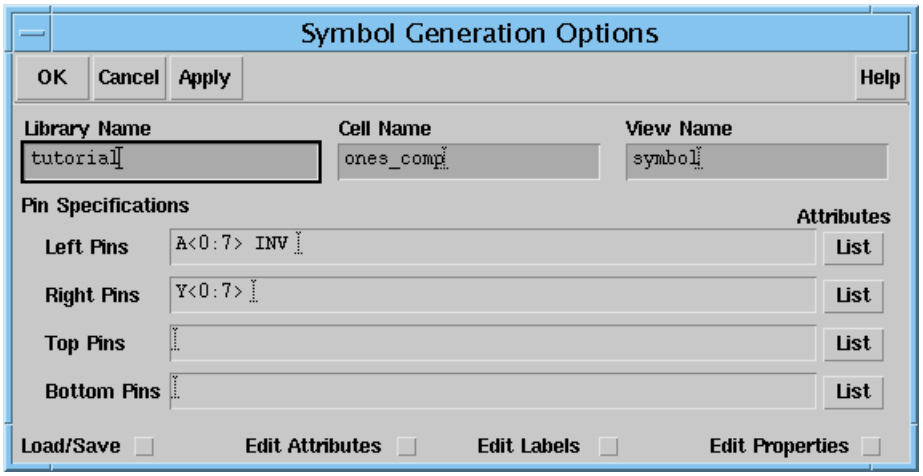


Figure 3-5 The Symbol Generation Options Form

6. Click *OK* on the Symbol Generation Options form.

   A symbol editing window opens to show you the generated symbol. In the future, you can use this window to modify the appearance and characteristics of the symbol.

Figure 3-6 The Generated Symbol in the Symbol Editing Window

Note: When you add the symbol to the top-view schematic, later in this tutorial, `[@partName]` changes to `accum` and `[@instanceName]` changes to the names of the next consecutive instance, `I1`.

7. Choose *Window* – *Close* to close the `ones_comp` symbol.

Creating the Accumulator Symbol

You will now create the accumulator symbol automatically, based on its primary input and output pins.

1. On the Cellview From Pin List form which was left open from a previous step, do the following:

   a. In the *Input Pins* field, type `CLK B<0:7> A<0:7>`

   b. In the *Output Pins* field, type `Y<0:7>`

   c. In the *Cell Name* field, type `accum`.

   d. Turn off *Display Cellview* and *Edit Options*.

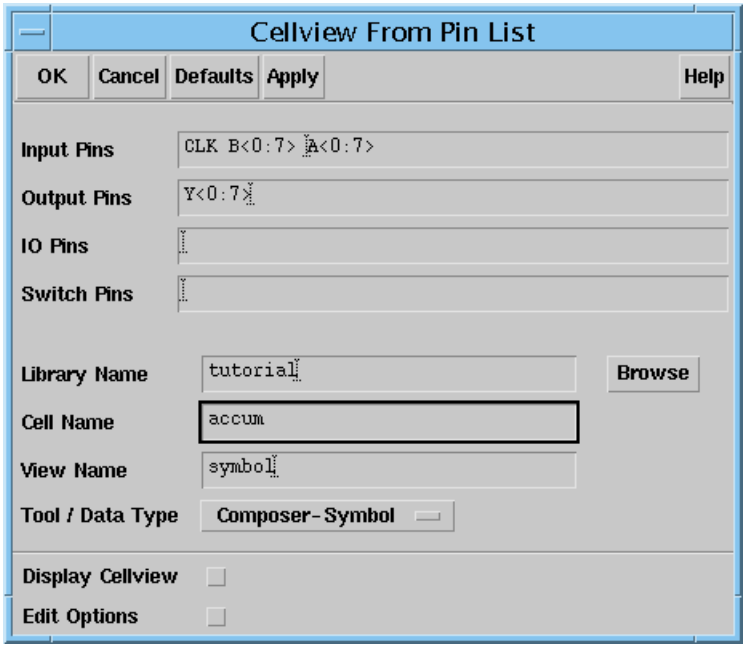


Figure 3-7 The Cellview From Pin List Form

2. Click *OK*.

Placing the Accumulator Symbol

To now place the accumulator symbol, you can use the Library Browser to fill in the form rather than typing in the fields yourself.

1. From the schematic editing window, choose *Add* – *Instance* to display the Add Instances form.
2. Click on the *Browse* button to display the Library Browser - Add Instance form.

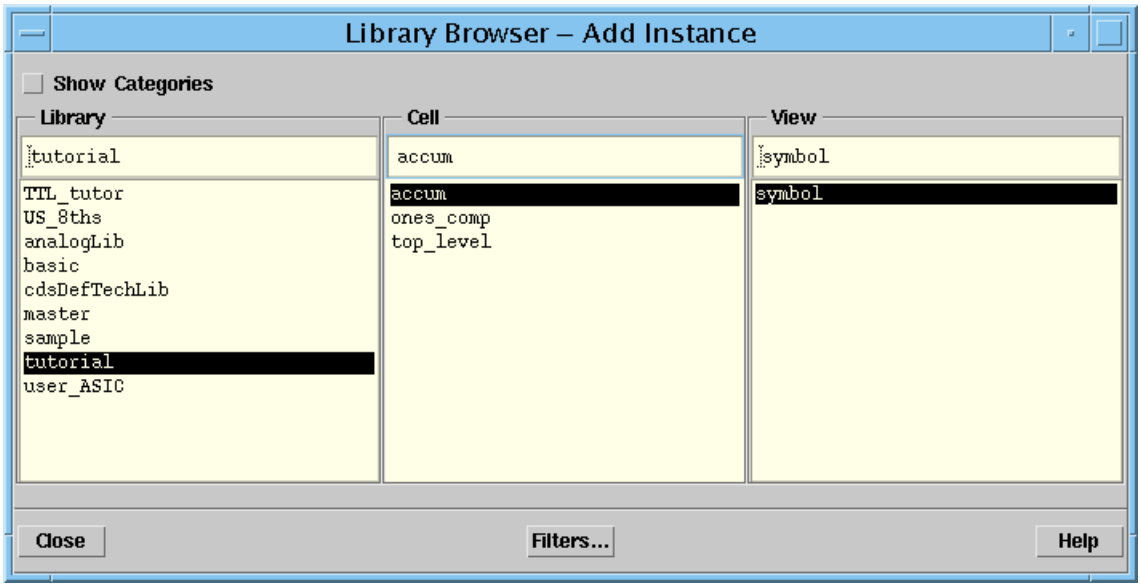


Figure 3-8 The Library Browser Add Instance Form

3. In the *Library* list box, click `tutorial`.
4. In the *Cell* list box, click `accum`.

   The Add Instance form changes as the system fills in the fields.

   The accumulator instance is now attached to the pointer.
5. Position the accumulator in the middle of your design and click to place it.

   Note: If necessary, refer to Figure 3-1 on page 28 for placement positioning.

Important

Do not press `Esc`, as you will want to keep the Add Instance form on screen, so that you can also place the one's complement symbol.

Placing the One's Complement Symbol

1. In the Library Browser, click ones_comp in the *Cell* list box to change the Add Instance form to now show that the ones_comp *Cell* has been selected.

   The shape of the one's complement instance now follows the pointer.

2. Position the one's complement to the left of the accumulator and click to place it.

3. Now you can cancel the *Add – Instance* command by pressing Esc with the pointer on the schematic.

4. Choose *Design – Save* to save your work.

Adding the Schematic Input and Output Pins

In the schematic editor software, a *schematic pin* is a primary input, output, or input/output terminal for the schematic.

1. From the schematic window, choose *Add – Pin* to display the Add Pin form.

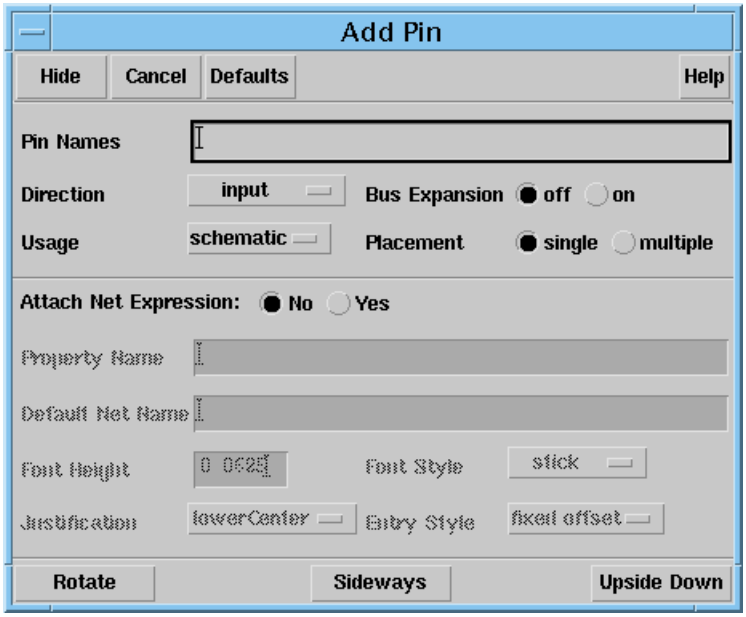


Figure 3-9 The Add Pin Form

2. In the *Pin Names* field, type `CLK INV DATA<0:7> OUT<0:3>`.

   The software places these pins one at a time, in order.

3. From the *Direction* cyclic field, choose *input*.

   Note: You will change the direction on the form to *output* just before you place the `OUT<0:3>` pin.

4. From the *Usage* cyclic field, choose *schematic*.

5. Position and click to place the `CLK` pin (see Figure 3-10 on page 39).

   Note that the `CLK` pin drops off the *Pin Names* field.

6. Position and click the `INV` and `DATA<0:7>` pins.

   Note: Before you place the `OUT<0:3>` pin, you need to change the pin direction to *output*.

7. From the *Direction* cyclic field, choose *output*.
8. Position and click the `OUT<0:3>` pin.

   Each time you place a pin, notice that the system removes the pin name from the list on the Add Pin form.

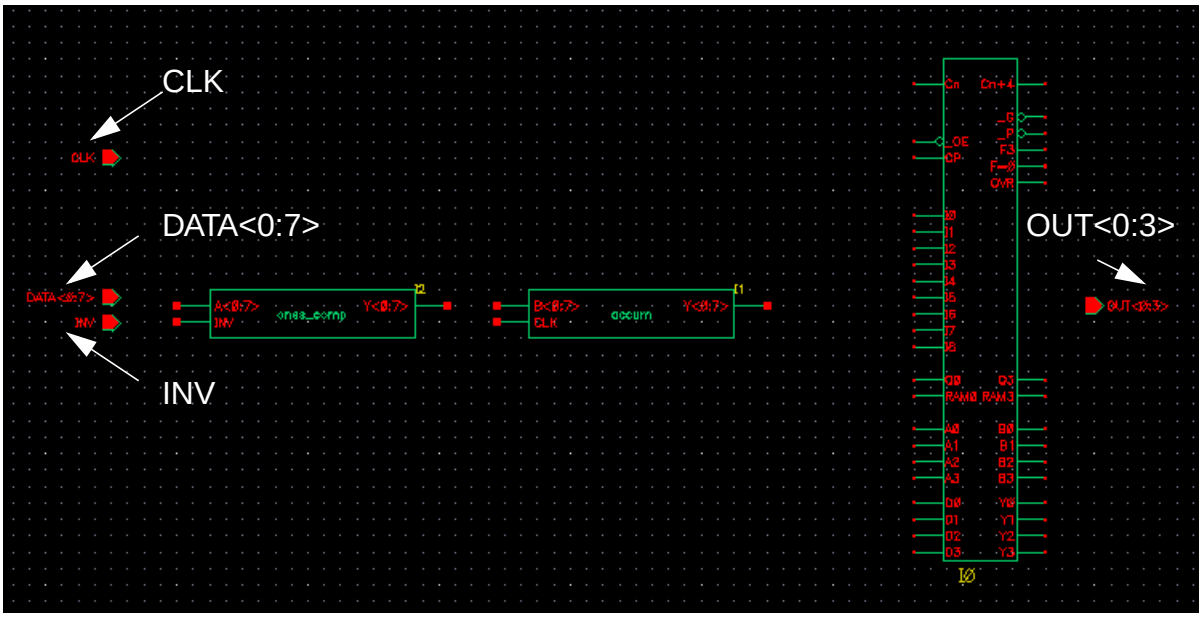


Figure 3-10 Positioning and Placing the Pins

You are now ready to add the two buses to your top-level schematic:

- The bus that connects the accumulator to the `ALU` (named the `DEC` bus)
- The output (`OUT`) bus.

Adding the DEC Bus

You can draw the buses using a thick line. The width of the line does not affect the connectivity of the buses, but it does help you identify buses on the schematic.

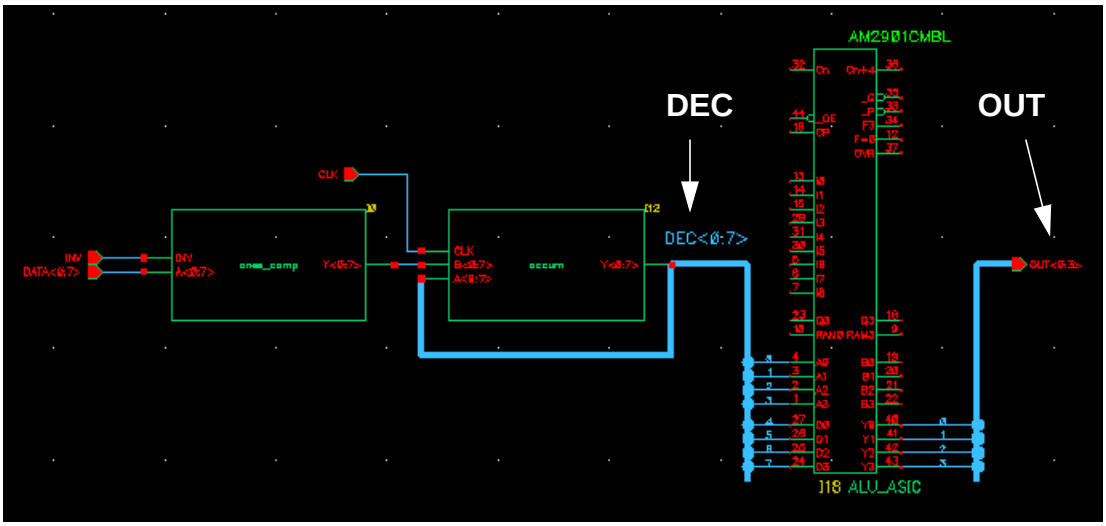


Figure 3-11 The Location of the DEC and OUT Buses

1. Zoom in so that you can see more clearly where to connect the buses. You can also do this with your mouse:

   a. At Point A, click you mouse pointer and press the Z key.

   b. Now move your pointer to point B and click again. This auto zooms into the selected area.

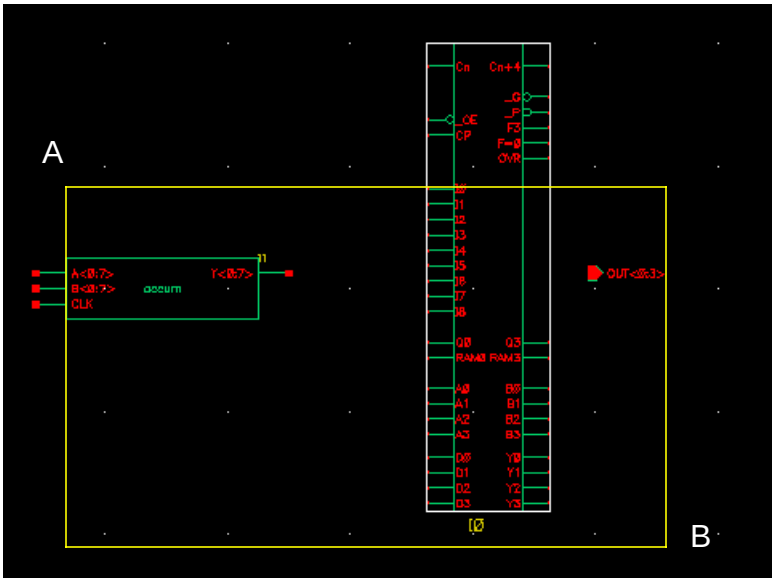


Figure 3-12 Zooming In Using the Z Key

2. From the schematic editing window, choose *Add – Wire (wide)*.

   The command line prompts you to start drawing the bus by displaying

   `Point at starting point for the router or snap to diamond using the "s" key.`

3. Click on the accumulator `A<0:7>` pin to start drawing the `DEC` bus.

Figure 3-13 Starting to Draw the Wide Wire

The first portion of the bus ends at the `Y` pin on the accumulator. If you move the pointer onto the `Y` pin, you will see that the router places the bus close to the accumulator. In the next step, you help the router by placing the first segment yourself.

Note: If you place a bus segment incorrectly, press `Esc` to cancel the command and then choose *Edit – Undo* to undo the error.

4. Move the pointer above the `accum` instance to position the first segment of the bus and click to place it.

   When you click, the segment appears as a thick line.

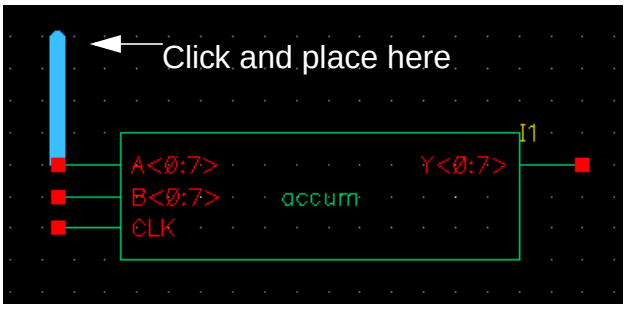


Figure 3-14 Placing the First Position Of The Wide Wire

5. Click on the Y pin to complete the first part of the DEC bus.

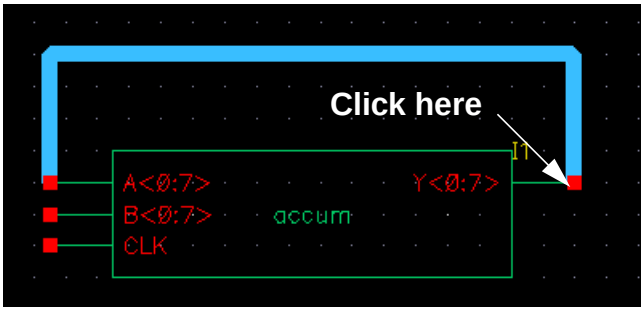


Figure 3-15 Completing the First Part of the DEC Bus

While routing a wire, notice that the pin closest to the end of the wire becomes highlighted with a diamond symbol. You can snap-connect the end of the wire to the highlighted pin by pressing s (for snap). When you press s, the wire jumps to the highlighted pin, closing the gap with straight segments joined at right angles. Snapping automatically routes the wire around other symbols. Undo the last step and try routing the bus again using snapping.

In the next steps, you change the *Draw Mode* to “X-first,” which is appropriate for drawing the remaining buses.

6. Choose *Add – Wire (wide)* again.

7. Before you select anything in the schematic window, press the F3 function key.

   The Add Wire form appears to let you change the manner in which wires are drawn.

8. Change the *Draw Mode* cyclic field to “X-first.”

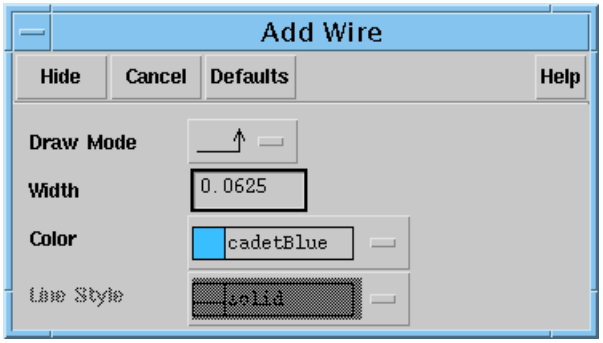
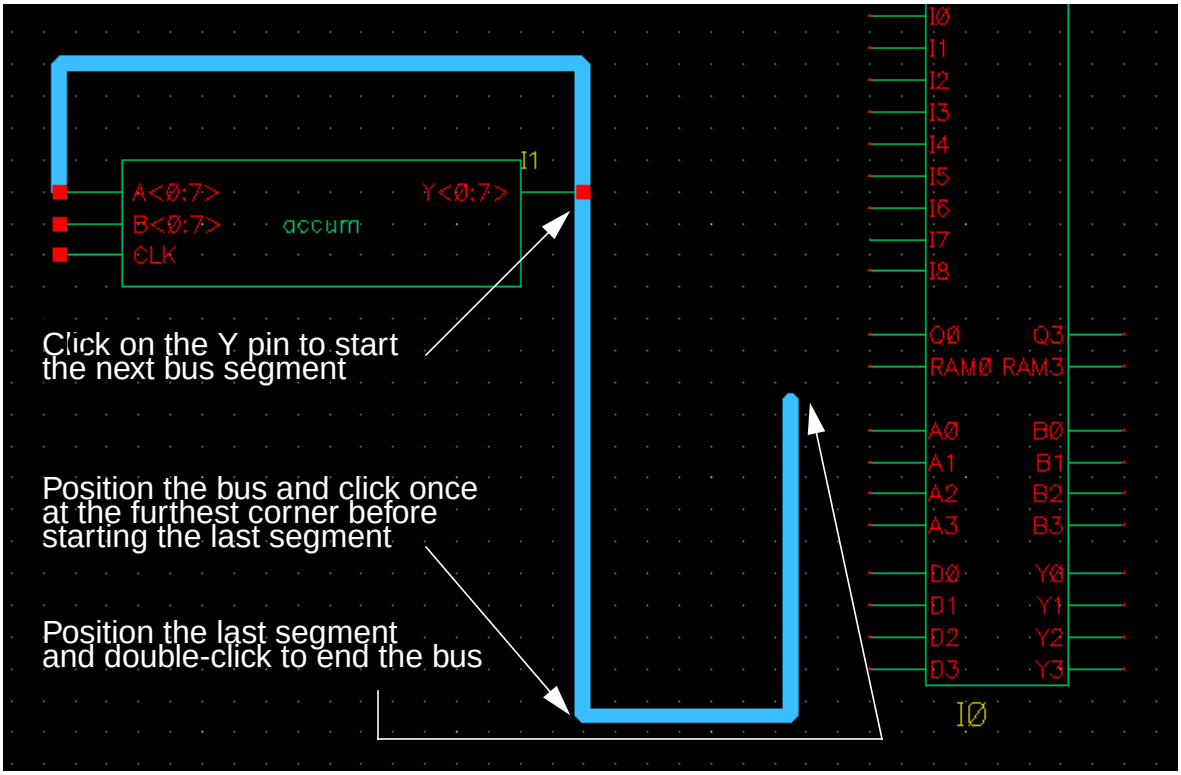


Figure 3-16 The Add Wire Form With X-first Selected As Draw Mode

9. Click on the accumulator Y pin to start the next bus segment.

10. Refer to the following diagram to position the bus, then double-click to end the DEC bus.

You must click twice to end any bus (or wire) that does not terminate on a symbol pin or a schematic pin.

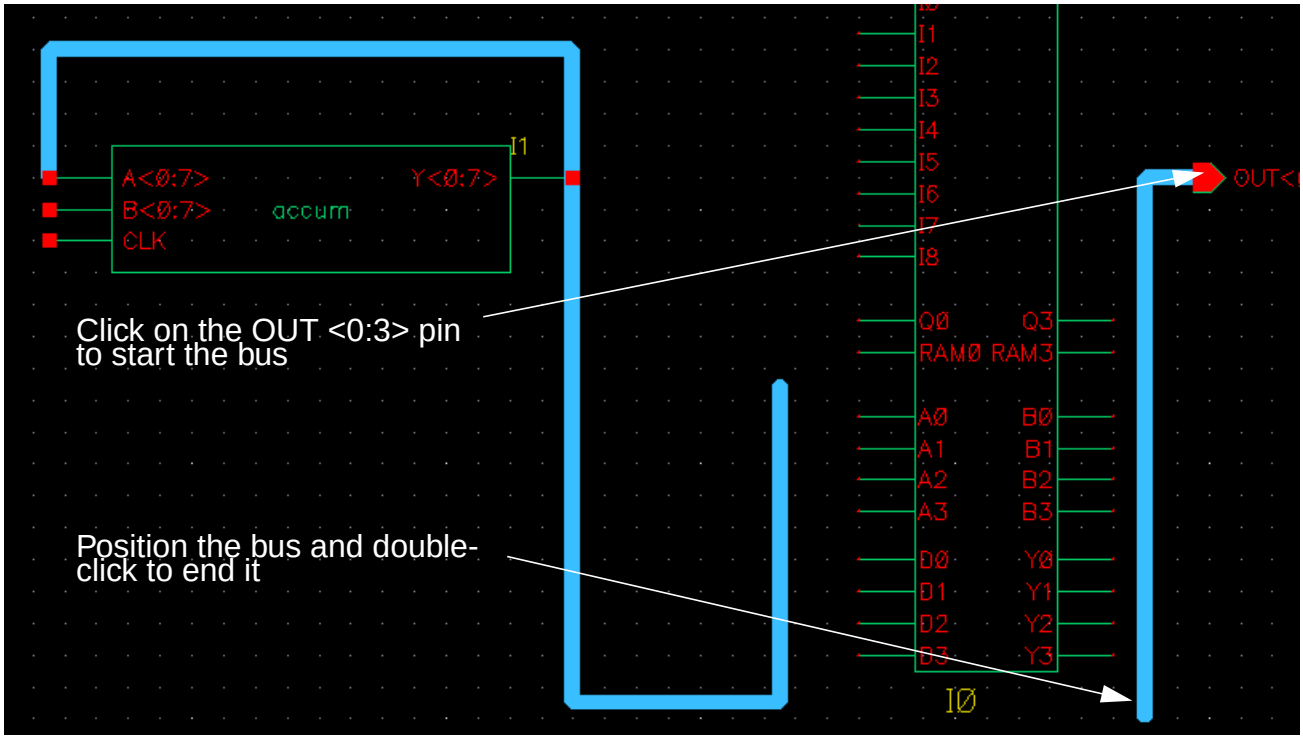


Note: If you create another segment by mistake, double-click to end the bus, press Esc to cancel the command, and choose *Edit – Undo* to undo the extra segment. You can also remove the last wire entered by pressing the Backspace key. You can press Backspace repeatedly to remove multiple wire segments.

Adding the Output Bus

You also use the “X-first” mode to place the output bus.

1. Click on the `OUT<0:3>` pin to start the output bus
2. Refer to the diagram to position the bus, then double-click to place it.



Note: You do not connect the two buses. In the next section, you will use nets to connect them to the ALU.

4

Adding Wires, Checking the Schematic, and Attaching a Border

Learning Objectives

In this chapter, you will finish the `top_level` schematic. In doing this, you will be performing the following tasks:

Wiring the Input Pins

In this section, you wire the instances, pins, and buses using the *Add – Wire (narrow)* command from the object-sensitive menu (OSM).

1. Select *Window – Zoom – Zoom In* (or use the "Z" key zoom technique described Figure 3-12 on page 41) to connect the nets easier.

   Note: Window menu commands, such as *Fit* and *Zoom In*, do not affect the current editing command, such as *Add Wire*. This means that you can zoom in and out on the schematic whenever necessary.

2. Click the pointer on the CLK pin.

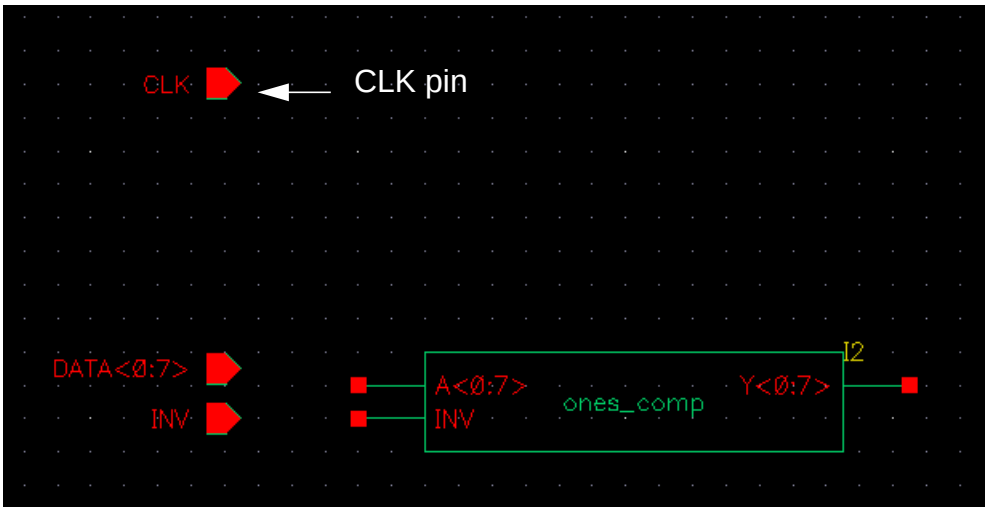


Figure 4-1 Clicking on the CLK Pin

3. Press the middle mouse button to pop up a *Pin* OSM.

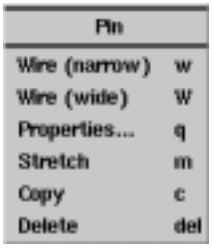


Figure 4-2 Middle Mouse Button Options for Pin

The *Pin* OSM contains commands that you might use on a pin.

4. Choose *Wire (narrow)* and release the button.

   Because you popped up the *Pin* OSM on the `CLK` pin (and *Infix* is on), the net from the `CLK` pin is already started. You see it when you move the pointer.

5. Route these nets, as shown in the figure (click at the beginning and ending points for each net).

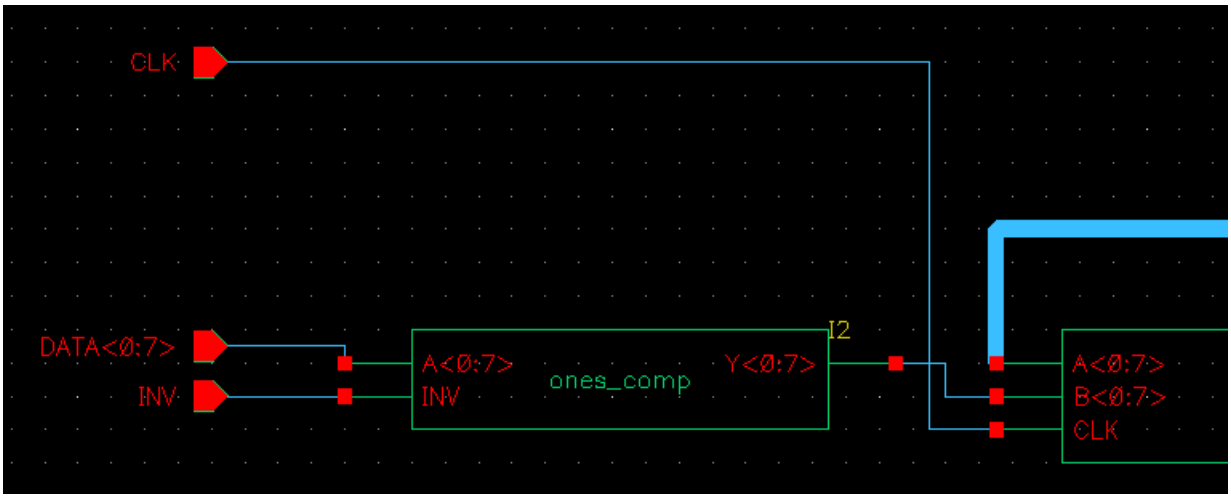


Figure 4-3 Wiring the Nets

   a. Connect the `CLK` pin to the accumulator `CLK` pin.

   b. Connect the `INV` pin to the `INV` pin on the one's complement module.

   c. Connect the `DATA<0:7>` pin to the `A<0:7>` pin on the one's complement module.

   d. Connect the `Y<0:7>` pin on the one's complement module to the `B<0:7>` pin on the accumulator.

Wiring the ALU

Now, you will wire the ALU. As always, it is easier to perform your work when you are zoomed in on the area where you are working.

1. Press `f` (Fit) to display the entire schematic.
2. Zoom on the area shown in the figure.

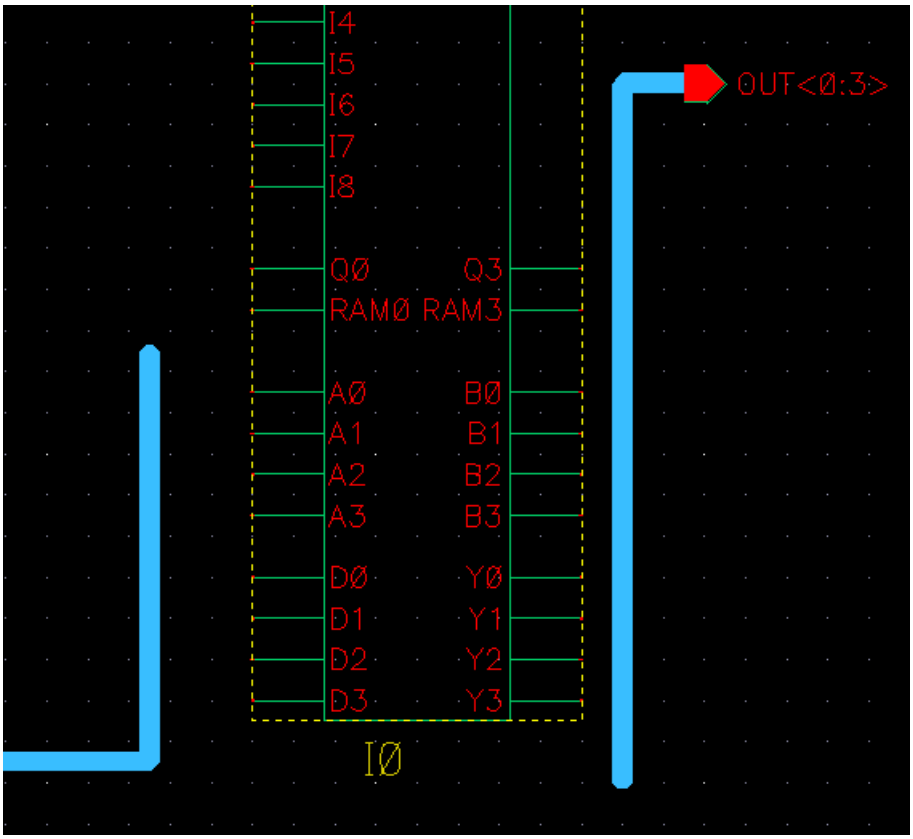


Figure 4-4 Zooming in to the ALU Area

3. To wire the ALU, click on the beginning and ending points for each net as shown below:

   A solder dot appears when you successfully tap one of the buses.

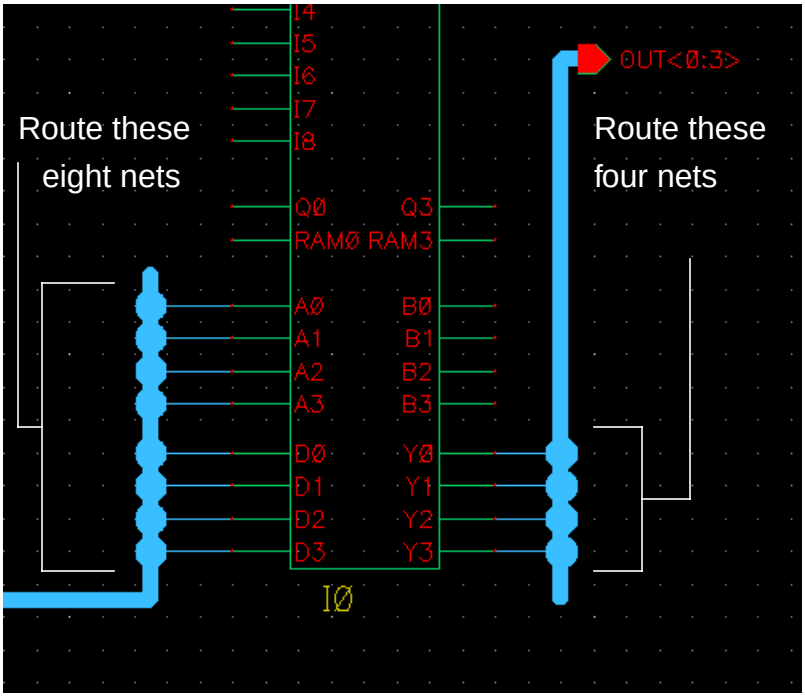


Figure 4-5 Routing the Nets

Note: The nets you have just placed are not tapped into a specific signal in either bus until you assign names to the nets. You will assign those names in the next section.

Naming the Nets

In this section, you name the nets tapping the buses. The nets that connect to the pins inherit the pin names and do not need names. You will use the name array feature, which lets you attach multiple names at one time.

If you zoomed in to fit the entire schematic into the window at the end of the previous section, you need to zoom in again on the nets tapping the buses.

1. Place the pointer over one of the nets tapping the buses.
2. Press the middle mouse button over the wire and the *Wire* OSM pops up.

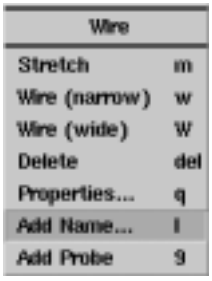


Figure 4-6 The Wire OSM

3. Choose *Add Name* from the Wire OSM to display the Add Wire Name Form.

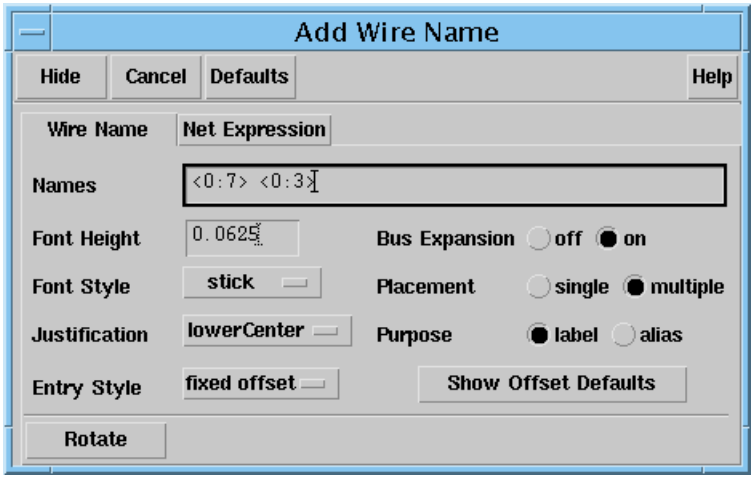


Figure 4-7 The Add Wire Name Form

4. In the *Names* field, type names for all these nets by specifying two name arrays, `<0:7>` and `<0:3>`.

   These arrays identify the bit ranges you are naming.

   The `ALU` pins tap the `DEC` bus and the `OUT` bus as follows:

   - Pins `A0` through `A3` tap bits `0` through `3` from the `DEC` bus.
   - Pins `D0` through `D3` tap bits `4` through `7` from the `DEC` bus.
   - Pins `Y0` through `Y3` tap bits `0` through `3` to the out bus.

5. Set *Bus Expansion* to *on*.

   The *Bus Expansion* button tells the system to extract individual bit names from the array names. The first name will be `<0>`, the second name will be `<1>`, and so on.

6. Set *Placement* to *multiple*.

   Setting the *Placement* button to *multiple* tells the system that you want to place an array of names, rather than one name at a time.

   You are now ready to place the input wire names.

Placing the Input Wire Names

1. Position the pointer on the first net to be named.

   The <0> name follows the pointer (see the figure).

Important

Follow the instructions in this section carefully. Check the figure before you do a step. Placing multiple names is easy once you know how, but it can be tricky the first time.

2. Click on the net to assign the name to it.

   Once the name is assigned, it remains with the net when you stretch or move the net.

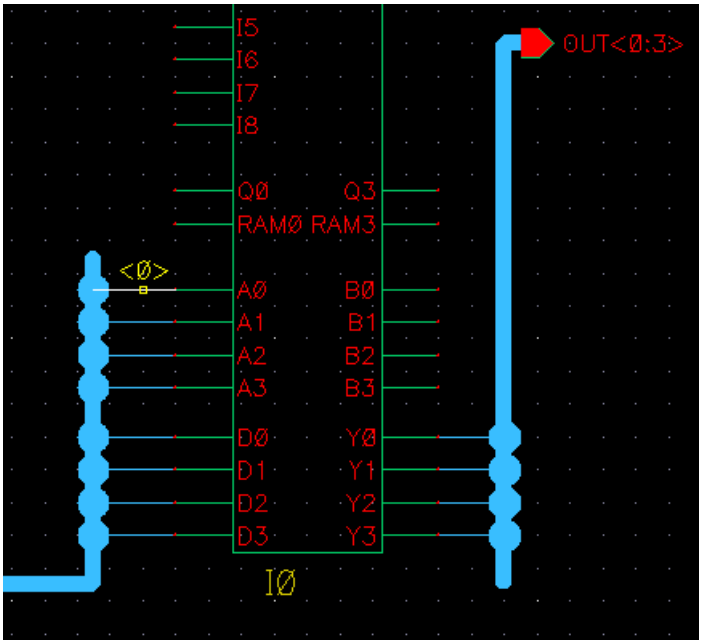


Figure 4-8 About to Place The Input Wire Names

A “rubberband” line, connected to the first wire, appears when you move the pointer. You will use the rubberband line to assign names to the remaining nets, as described in the next step.

3. Move the pointer to the bottom net to display and position the remaining names.

4. Click on the bottom net to assign the remaining names.

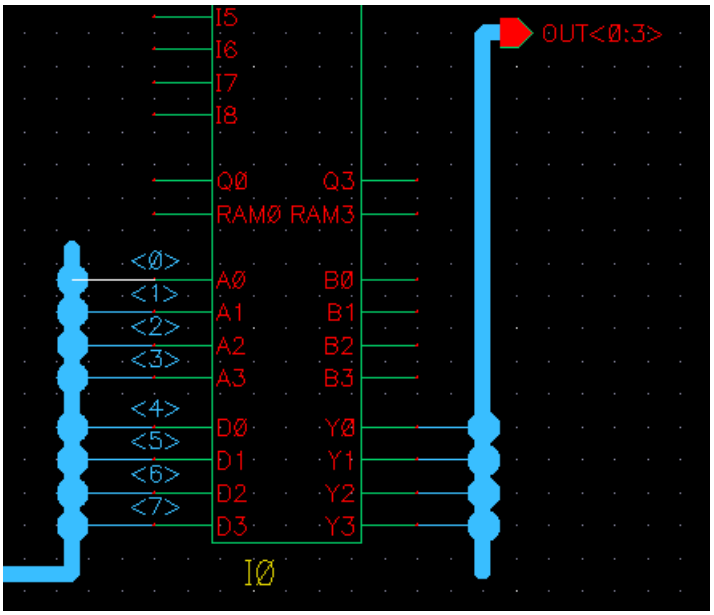


Figure 4-9 Net Names <0:7> Assigned

Dropped a bit? If you accidentally click on a net other than the last one, the system saves the remaining wire names and allows you to continue placing them until all eight names for the bus wires have been assigned. If you have any other problems with automatic name placement, undo your last steps and try again. If you do not name all the nets, the system issues an error message when you check the design.

Placing the Output Wire Names

Assign the output names just as you placed the input names.

1. Click to place the <0> name on the net connecting the Y0 pin.
2. Move the pointer to the bottom net (connecting the Y3 pin) to include the remaining nets.
3. Click on the bottom net to assign the remaining names.

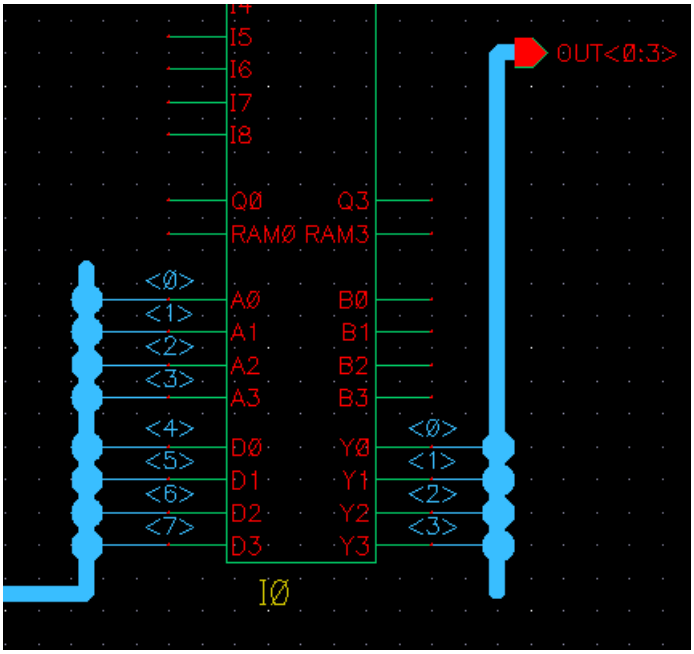


Figure 4-10 Net Names <0:3> Assigned

4. Press Esc to cancel the *Add – Wire Name* command.

   You have now completed naming the nets.
5. Zoom out to fit the entire schematic.

Checking the Schematic

Up to this point, you have created a drawing of the schematic. In this section, you use the *Check and Save* command to do the following:

- Check your design for errors
- Establish electrical connectivity
- Save the design and connectivity information in the system database

You might have noticed that you have not yet named the DEC bus. As a result, *Check* will find an error in your schematic.

Once you have established electrical connectivity with the *Check and Save* command, you can use the design as input to other tools, such as a simulator.

Setting Up the Check Rules

In this section, you set the rules for checking the schematic to ignore floating inputs and outputs. Your design is incomplete, with floating inputs and outputs, and you do not want to be presented with a long list of error messages.

1. Choose *Check – Rules Setup* to display the Setup Schematic Rules Checks form. This form identifies the conditions to be flagged with warning or error messages.

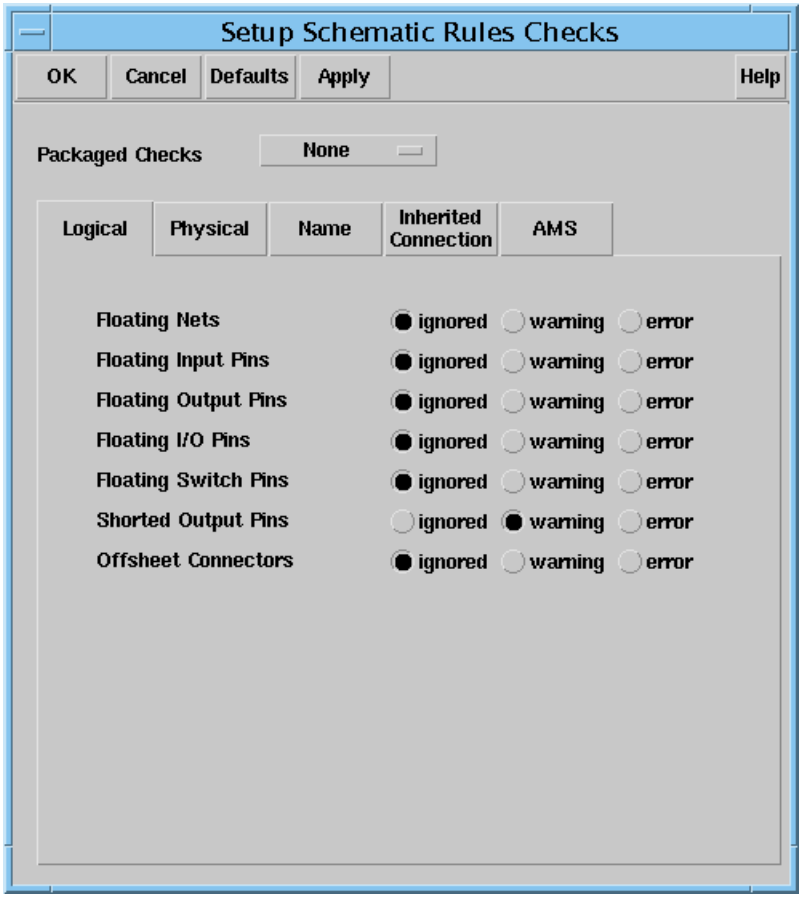


Figure 4-11 The Setup Schematic Rules Check Form

2. Turn on the *ignored* buttons for floating nets and pins.
3. Click *OK*.

Running Check and Save

1. Choose the *Check and Save* icon (the tick box) on the left side of the schematic window.

   The Check program checks the schematic. Because you have omitted the DEC bus name, *Check* finds errors in your design. As a result, the following occurs:

   - The errors on the schematic start blinking with *error markers*.
   - The (CIW) shows the error messages.
   - A dialog box appears, giving the number of errors.

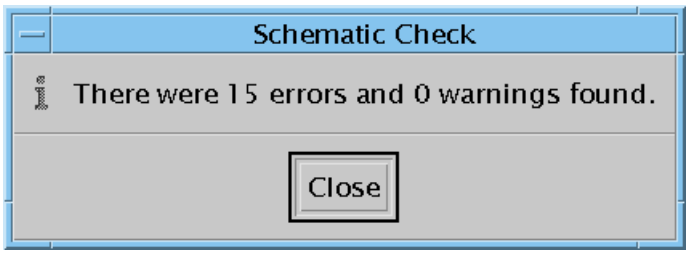


Figure 4-12 The Schematic Check Error Results

2. Click *Close*.

   A second dialog box appears, questioning your decision to save a design with errors.

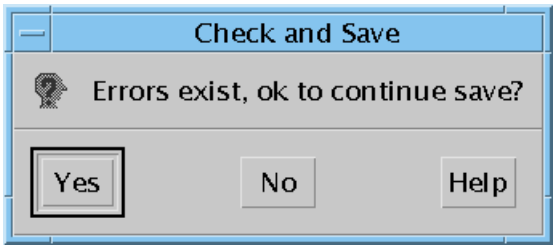


Figure 4-13 Saving The Design With Errors

3. Click *Yes*.

   The Virtuoso® Schematic Editor software saves the design and displays a confirmation message in the CIW:

   ```
   "tutorial top_level schematic" saved.
   ```

The following output is an example of the errors that might exist:

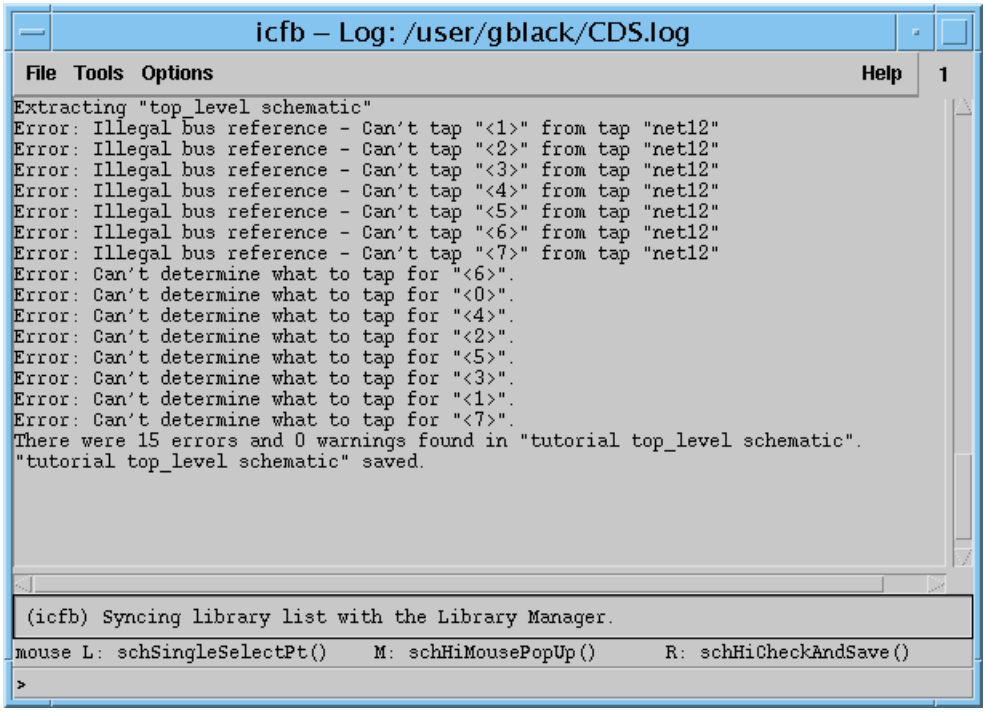


Figure 4-14 The CIW Displaying The Schematic Errors

In the next section, you display the error message for each error marker.

Identifying the Errors

1. Choose *Check – Find Marker* to display the Find Marker form.

   The Find Marker form appears, displaying the error messages. The first message on the Find Marker form is selected.

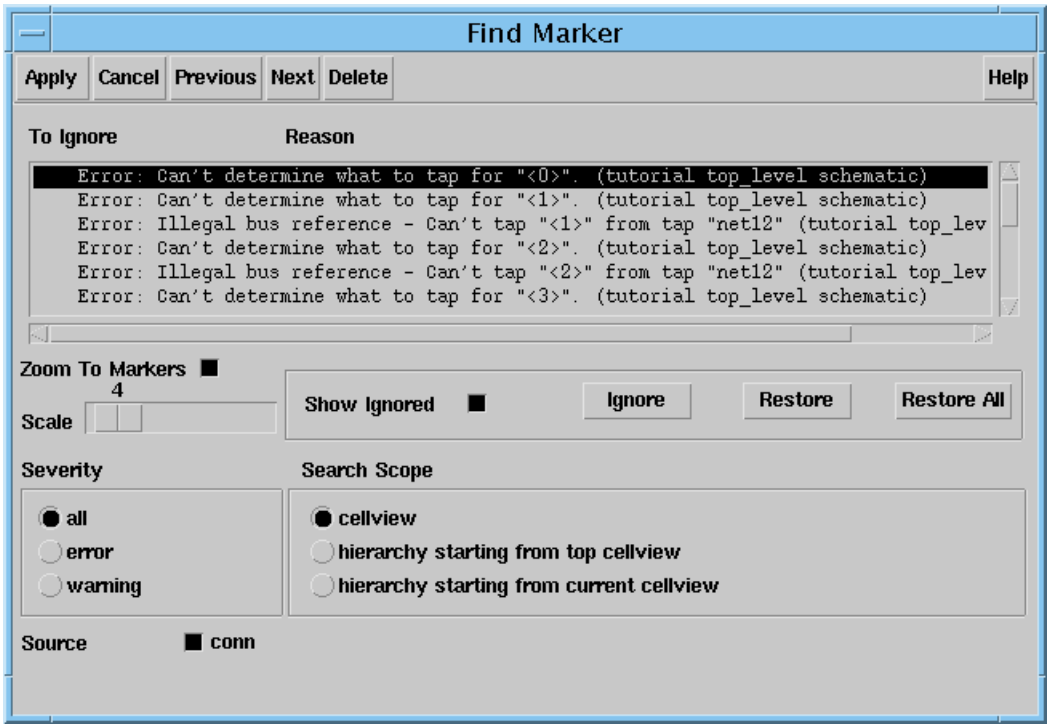


Figure 4-15 The Find Marker Form

2. To magnify the location of specific error markers, turn on *Zoom To Markers*.

3. Position the schematic editing window and the Find Marker form side by side.

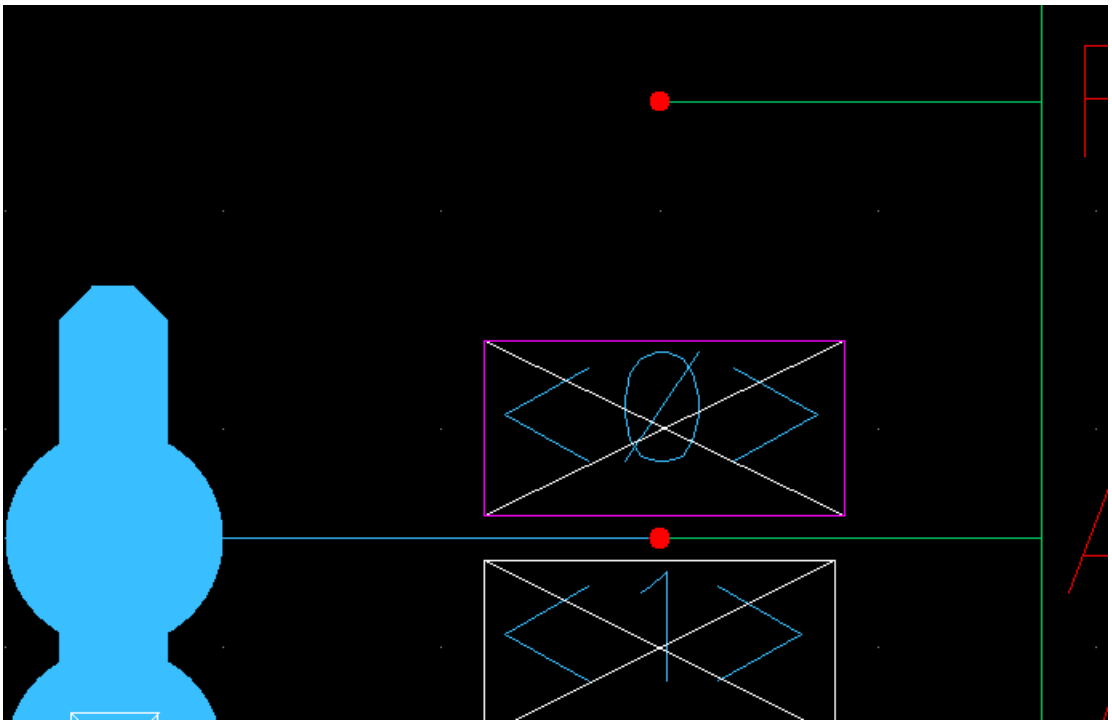


Figure 4-16 Zooming In To The Error Markers

The error is caused by the missing name for the DEC bus. The system cannot determine which signal is being tapped. Because any signal is a possible candidate, the system shows the whole design and does not zoom in on one section.

4. Click *Next* to see the next error.

   You can continue clicking on *Next* or *Previous* to cycle through the messages. When you get to an `illegal bus reference` message, the schematic window will zoom in on the area with the flashing markers.

   The one marker in a different color corresponds to the selected error message. All other markers remain white.

   All the errors are caused by the missing bus name. In the next section, you create the missing name.

5. Click *Cancel* on the Find Marker form to cancel the command.

   The forms disappear. The markers remain. They will be automatically deleted later when you run *Check and Save* after naming the bus.

Naming the DEC Bus

1. Choose *Add – Wire Name* to display the Add Wire Name form.

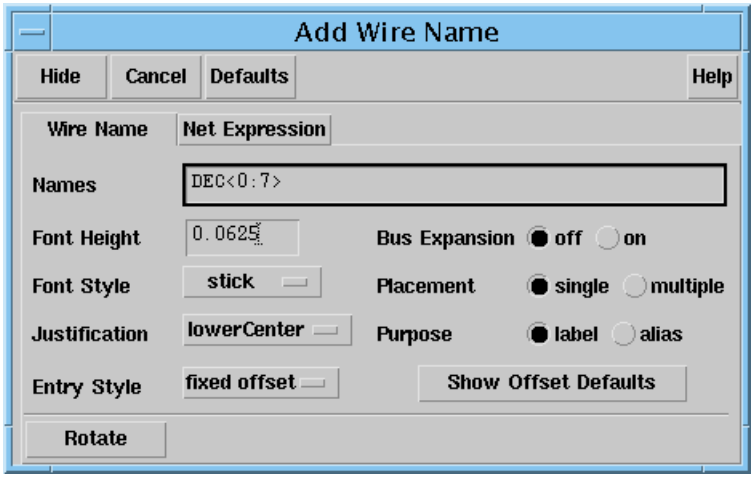


Figure 4-17 The Add Wire Form

2. In the *Names* field, type `DEC<0:7>`.
3. Position the name *above* the bus and click to place it.

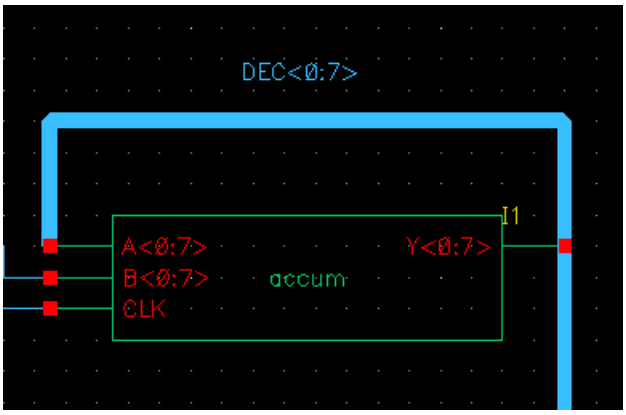


Figure 4-18 Placing The DEC<0:7> Name

4. Press Esc to cancel the *Add – Wire Name* command.

5. Choose the *Check and Save* icon to rerun the Check program. This time, no errors occur on the `DEC<0:7>` bus.

   The system saves the design with its connectivity information. Confirmation messages appear in the CIW.

You have completed the design. In the next section, you attach a border to the schematic.

Creating a Sheet Border and Title

You can create a border to your schematic and a title block to identify it. Attaching a border consists of the following three steps:

1. Creating the border
2. Centering the design within the border
3. Naming the schematic.

Creating a Border

1. Choose *Sheet – Edit Size* to display the Change Sheet Border Size form.

Figure 4-19 The Change Sheet Border Size Form

2. Change *Border Size* from *A* to *B*.
3. Click *OK*.

   Depending on where you placed the instances, a dialog box might appear.

   The B-sized border appears on the schematic. The border might cut through part of the design, as illustrated in the following figure.

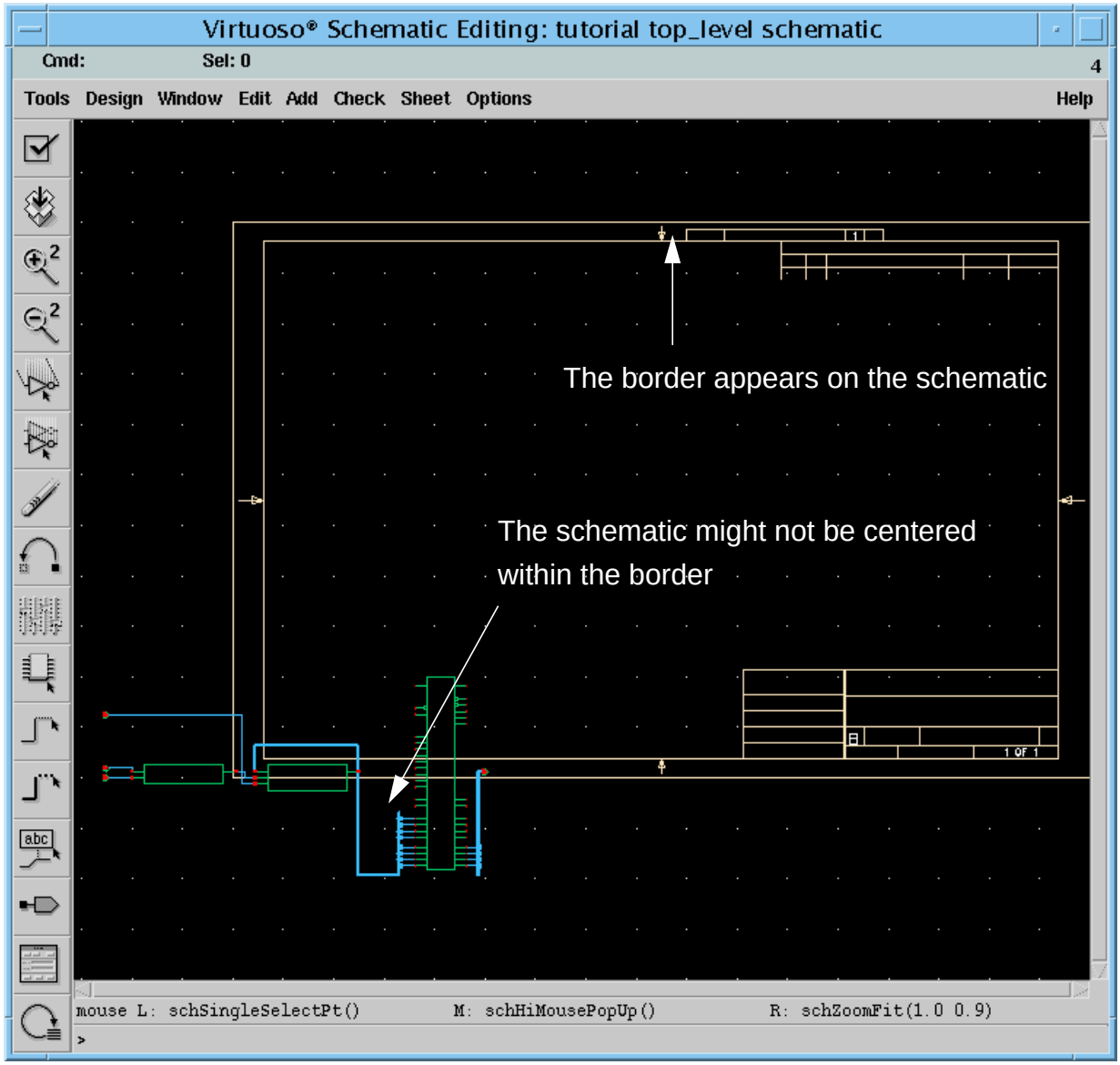


Figure 4-20 The Original Placement Of The Sheet Border

Centering the Schematic within the Border

If the border cuts through part of your schematic, you must move the design to center it. If your design is already centered within the border, you can skip this section.

1. Select the entire schematic by moving the pointer above the design, click, and drag to form a box around the design.

   The entire schematic is selected.

2. Press `M`.

   A bright box appears around the schematic.

3. Move the pointer to position the design inside the border.

   The shape of the design follows the pointer.

4. Click to place the design.

   The design appears within the border, and the Move box disappears.

5. Click on the schematic window, outside the schematic, to deselect it.

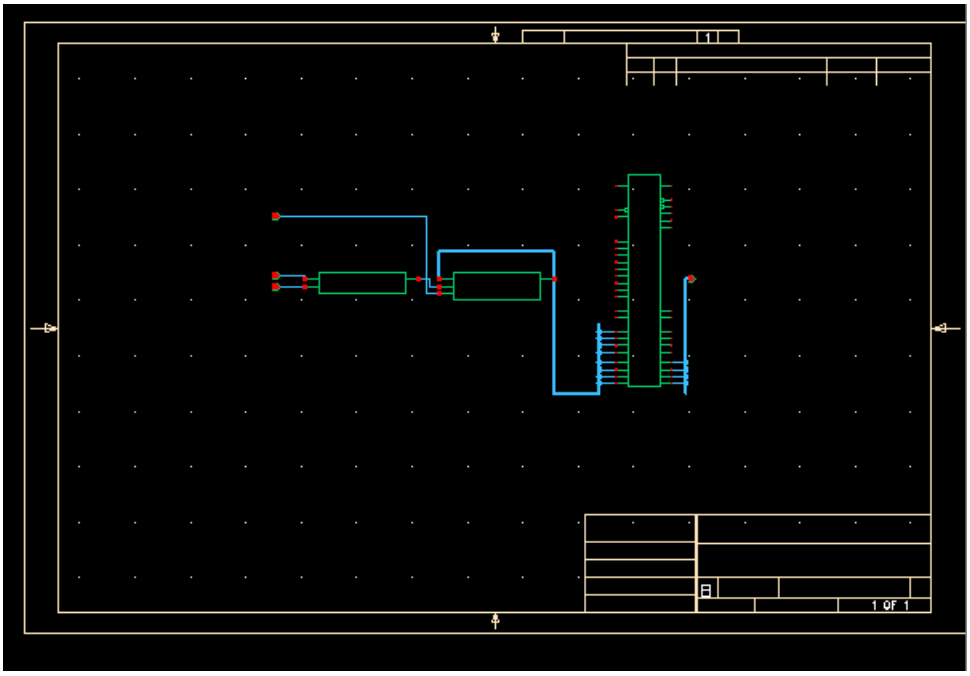


Figure 4-21 The Re-Positioned Schematic Within The Sheet Border

Adding a Name to the Title Block

1. Choose *Sheet – Edit Title* to display the Schematic Title Block Properties form

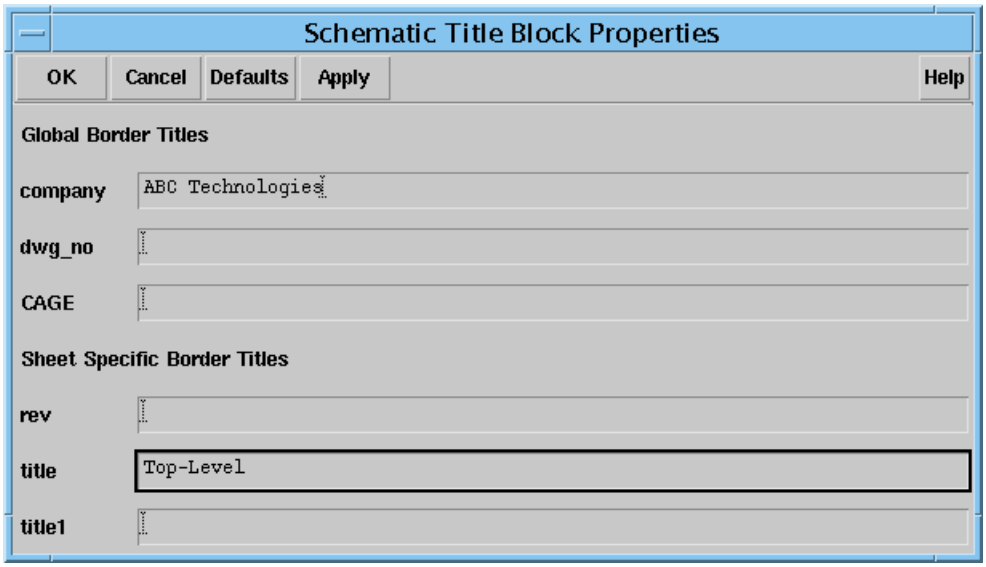


Figure 4-22 The Schematic Title Block Properties Form

2. Type your company name and the schematic title.
3. Click *OK*.

   The company name and schematic title appear in the title block of the schematic design.
4. Save your design.
5. Choose *Window – Close* to close the schematic window.

You have now completed and checked in the top-level schematic for the tutorial design.

In Chapter 5, “Creating the Accumulator Schematic” you will create the accumulator schematic.

5

Creating the Accumulator Schematic

Learning Objectives

In this chapter you will learn how to:

- Automatically create a schematic cellview
  - You will automatically create the schematic cellview for the accumulator, based on the accumulator symbol on the top-level schematic.
  - The new schematic cellview will contain schematic pins based on the pins defined for the accumulator symbol.
- Add instances for standard functions to the schematic.
- Create pin-to-pin connections between two parts
- Wire multiple pins with one command by creating wire copies
- If you have problems executing a command, remember to look at the prompt in the CIW.

About the Accumulator

The accumulator schematic contains the following:

- Two 4-bit adders
- One clocked 8-bit register
- Three schematic input pins and one schematic output pin
- Three 8-bit buses, represented by the thick lines

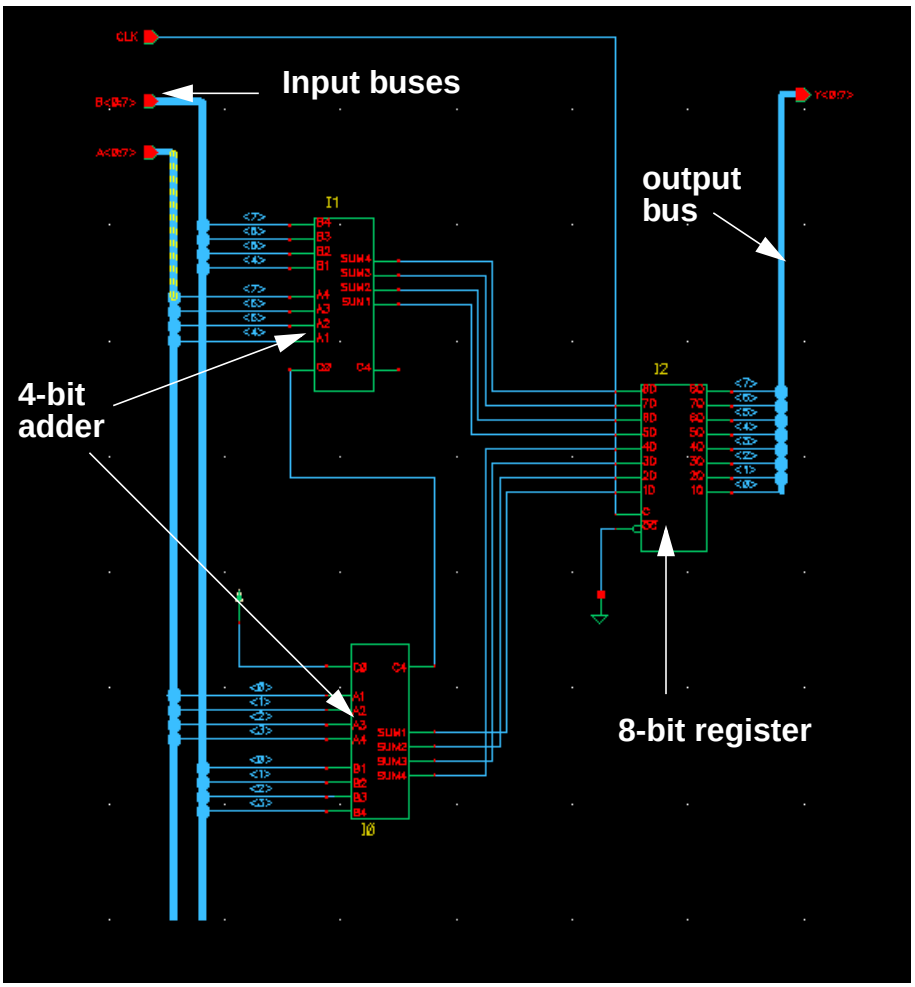


Figure 5-1 The Accumulator Schematic

Note:

Adding Instances

In this section, you automatically create the *accum* schematic cellview.

You will base the schematic on the accumulator symbol in the top-level schematic. The new schematic contains the pins defined for the accumulator symbol.

Follow these steps to create the *accum* schematic cellview.

1. Start the Virtuoso® Schematic Editor software (unless it is already running) and set your environment options with *Options – User Preferences*.

   Set *Infix* and scroll bars to *on* and change the undo limit to 10.

2. In the *tutorial* library, choose *Design – Open* and open the top-level schematic for editing.

3. Choose *Design – Create Cellview – From Instance*.

   The prompt line in the status bar at the bottom of the schematic editing window is

   ```
   Point at instance to generate view
   ```

4. Click on the *accum* instance to create the *accum* schematic cellview.

   The Cellview From Instance form appears.

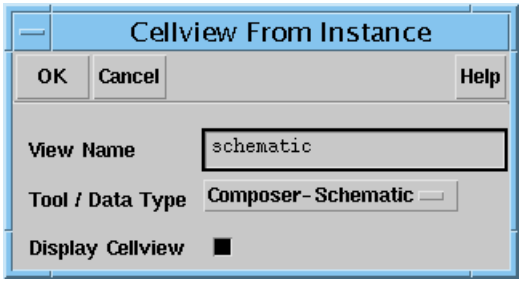


Figure 5-2 The Cellview From Instance Form

5. Make sure the *Display Cellview* option is selected.

6. Check that *View Name* is set to `schematic` and click *OK* to now display the Create Schematic form appears.

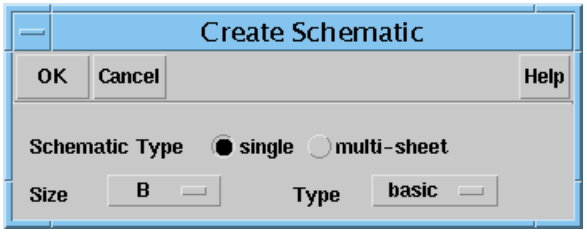


Figure 5-3 The Create Schematic Form

7. Set *Size* to *B* and click *OK.*

8. Open the *accum* cellview.

   The *accum* cellview is displayed automatically in another schematic window. It contains the schematic input and output pins created by the *Create Cellview* command, set inside a B-sized schematic border.

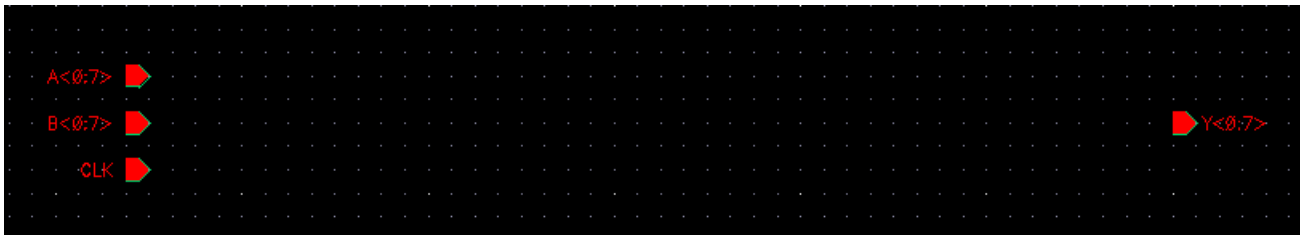


Figure 5-4 The accum Cellview

You are now ready to start creating the schematic.

Adding Two 4-Bit Adder Symbols

1. Choose *Add – Instance* to display the Add Instance form.

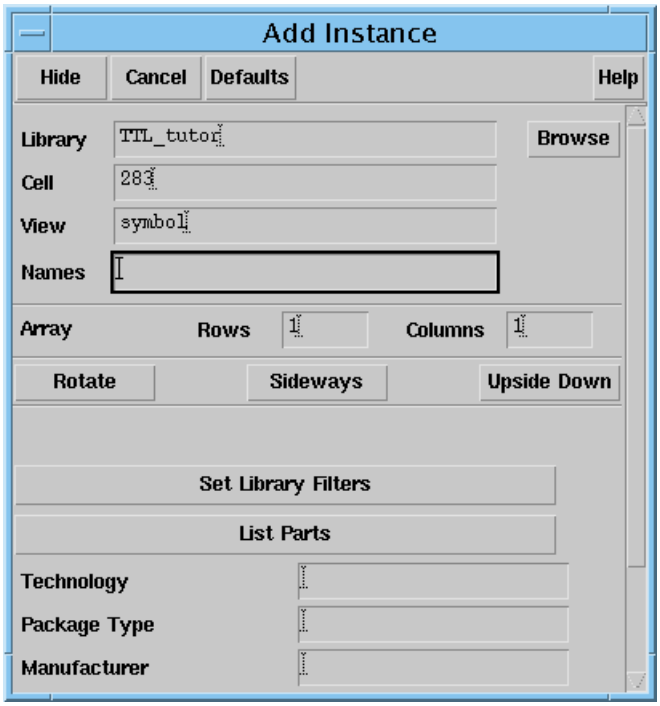


Figure 5-5 The Add Instance Form

2. In the *Library* field, type `TTL_tutor`.

   The *TTL_tutor* library contains symbols for the functions used in the tutorial design. The generic function numbers for these symbols appear in the Instance window.

3. In the *Cell* field, type `283`.

   The *adder* instance appears in the schematic window.

4. Position the first *adder* (`I0`) instance at the bottom of the screen and click to place it.

   You will place the second adder instance upside down. The instance shape continues to follow the pointer.

5. Click on *Upside Down* on the Add Instance form.

6. Position the second instance (`I1`) above the first instance and click to place it.

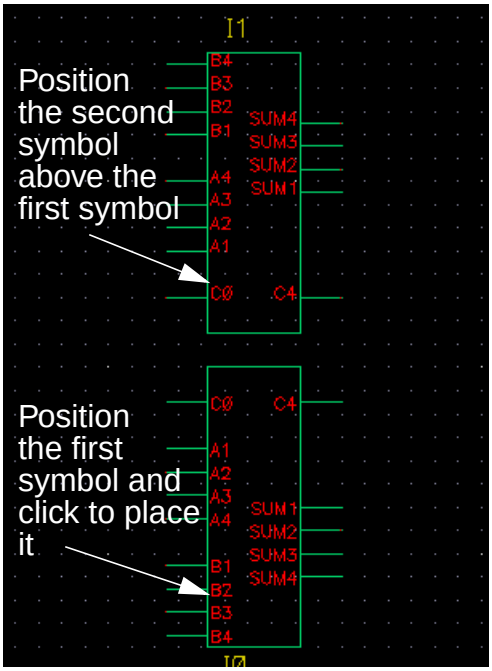


Figure 5-6 The Two 4-Bit Adder Symbols Added

Adding the 8-Bit Register Symbol

1. In the *Cell* field, type `373` for instance `I2` and click on *Upside Down* to turn off the feature from the last step.
2. Zoom in and place the *register* instance so that you create a pin-to-pin connection with the top adder instance.

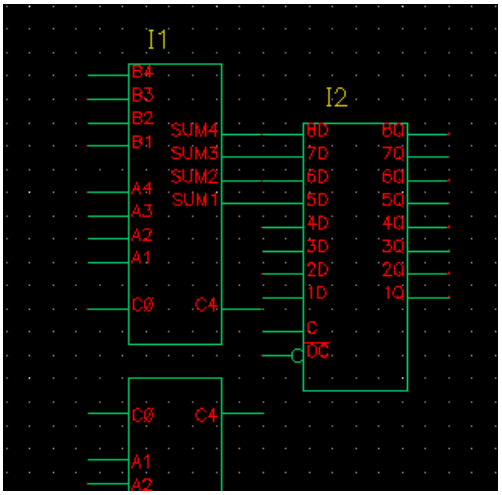


Figure 5-7 Placing the `I2` Instance

3. Position the register instance so that the top four input pins are touching the four SUM output pins of the top adder instance.
4. Check that the register instance is positioned properly (not upside down).
5. Press `f` to fit the entire schematic in the window.

   In the next section, you will add the power and ground symbol.

Adding Power and Ground Symbols

To add power and ground symbols, do the following:

1. In the *Library* field of the Add Instance form, type `basic`.

   The power and the ground symbols are in the *basic* library. This library is supplied with the schematic editor software.

2. In the *Cell* field, type `PWR`.

3. Position the power symbol close to the `C0` pin on the bottom adder instance and click to place it.

   The shape of the `PWR` symbol continues to follow the pointer.

4. In the *Cell* field, type `GND`.

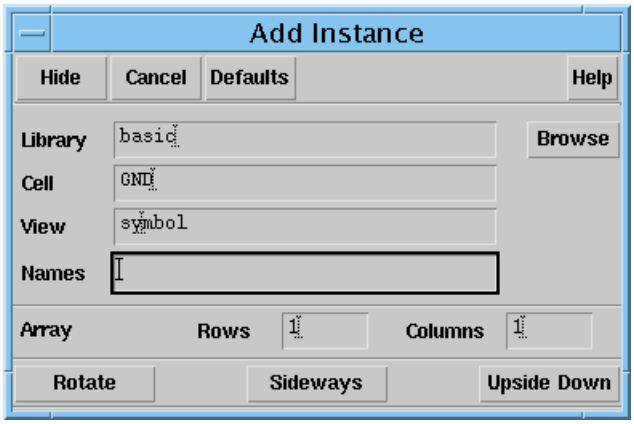


Figure 5-8 Adding the GND Symbol

5. Rotate the `GND` symbol *Upside Down*.

6. Position the ground (GND) symbol on the other side of the bottom adder instance.

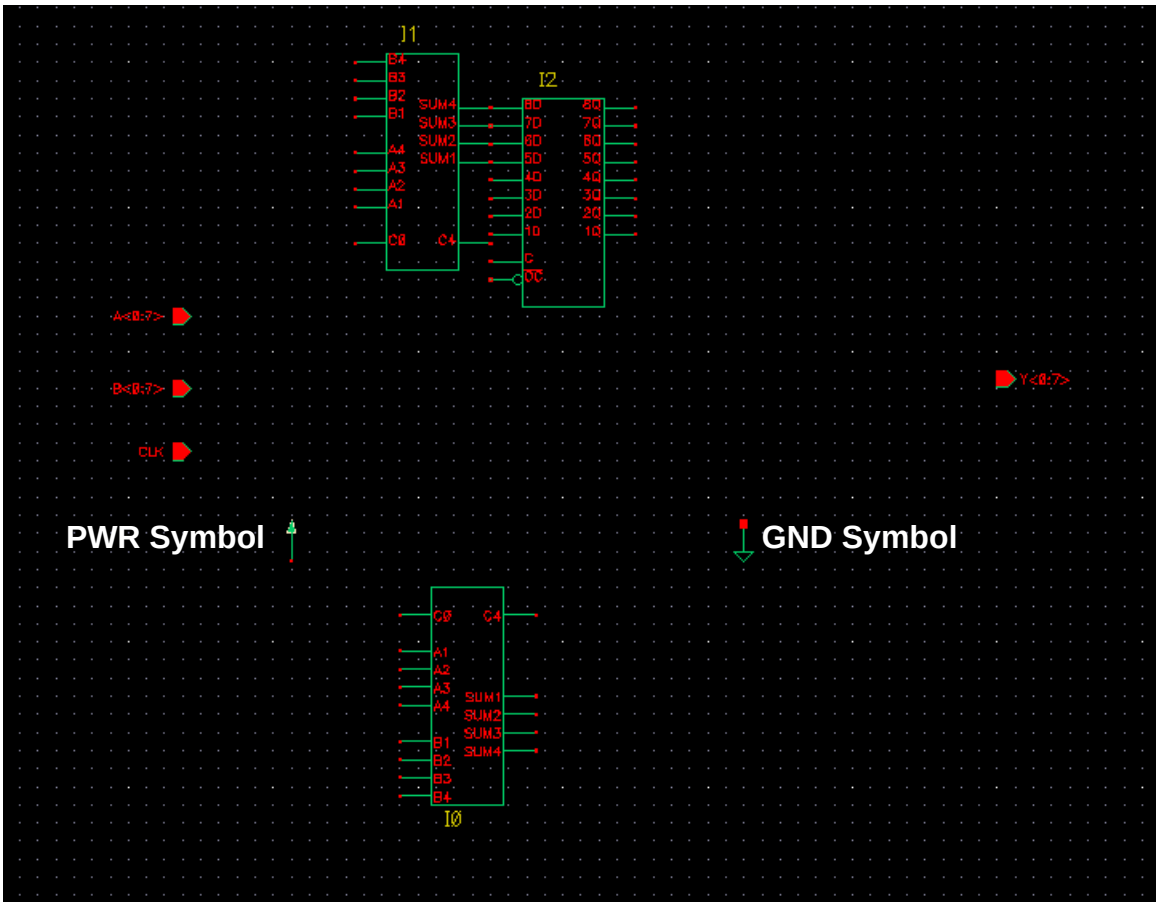


Figure 5-9 The PWR and GND Symbols Placed

7. Press Esc to cancel the *Add – Instance* command.

   In the next section, you will start wiring the schematic.

Adding Wires and Buses

In this section you “stretch” the register symbol and wire the adders, power supply, and ground symbols.

Stretching the Register Symbol

You will now stretch the register symbol to create the wires between the adder and the register symbols. Stretching an object is similar to moving an object, except that the object retains its connections to other objects.

1. Choose *Edit – Stretch*.

   The status bar at the bottom of the window displays

   `Point at object to stretch.`

2. Click on the register symbol to select it for the stretch.

   The CIW displays

   `Point at destination point for stretch.`

3. Reposition the register symbol as shown below. Dotted flight lines show the connections between the two symbols.

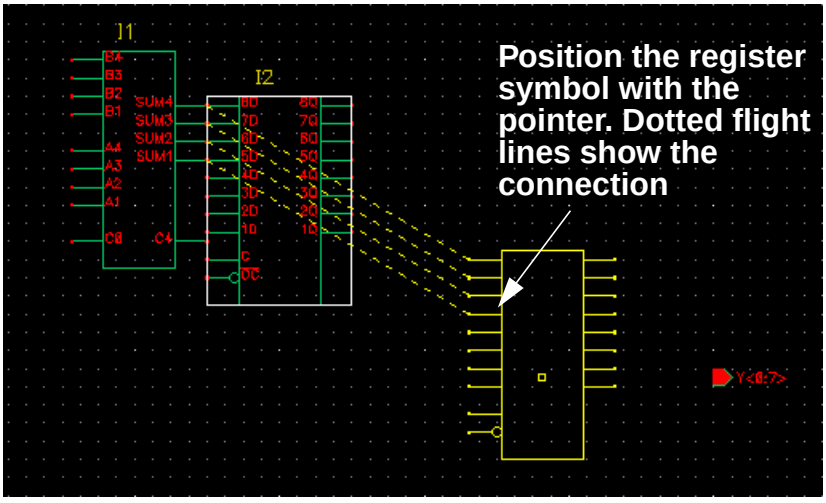


Figure 5-10 Repositioning The Register Symbol

4. Click to place the register symbol.

   The system automatically routes the nets.

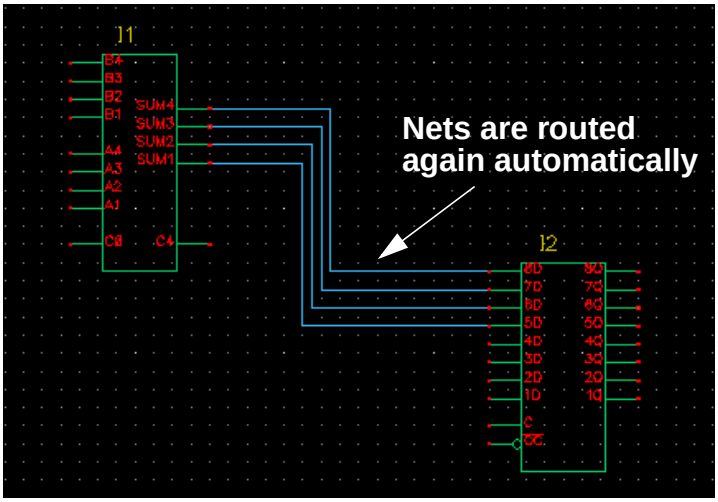


Figure 5-11 Re-routed Nets After Stretching

Wiring the Adders, Power Supply, and Ground Symbols

1. Zoom in on the area shown in the figure.

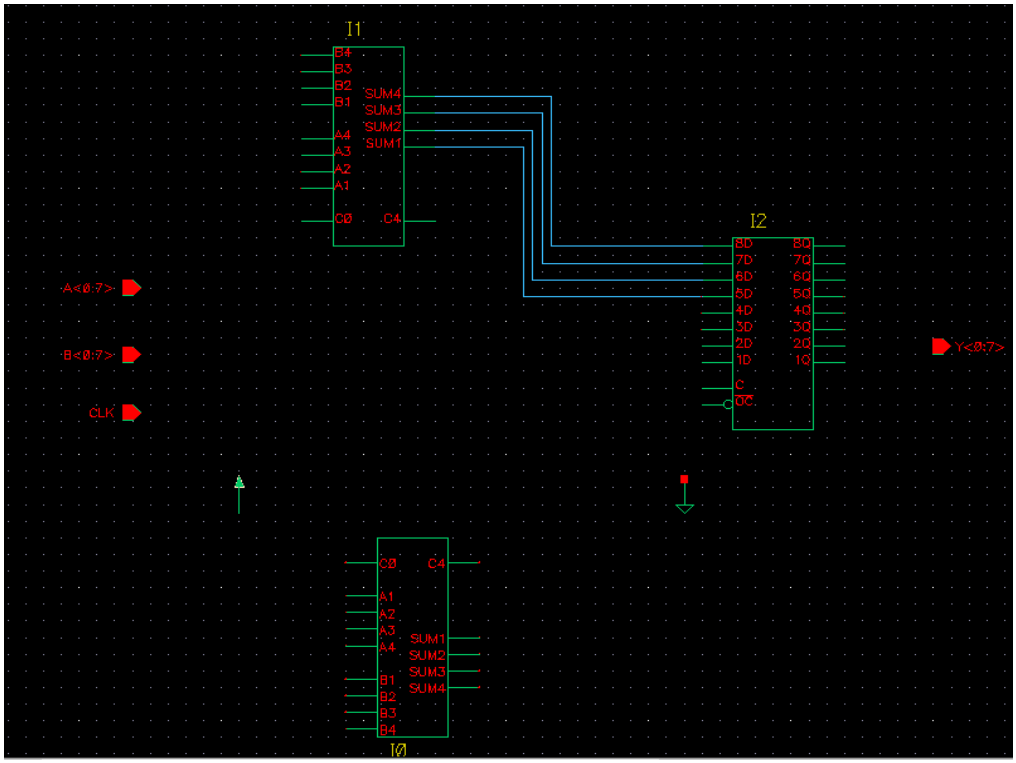


Figure 5-12 Zoomed In Area

2. Choose *Add – Wire (narrow)*. You may need to press the F3 function key to bring up the Add Wire form.
3. Set *Draw Mode* to *route*.

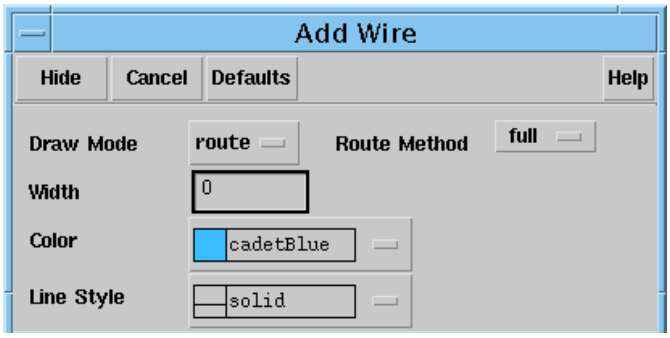


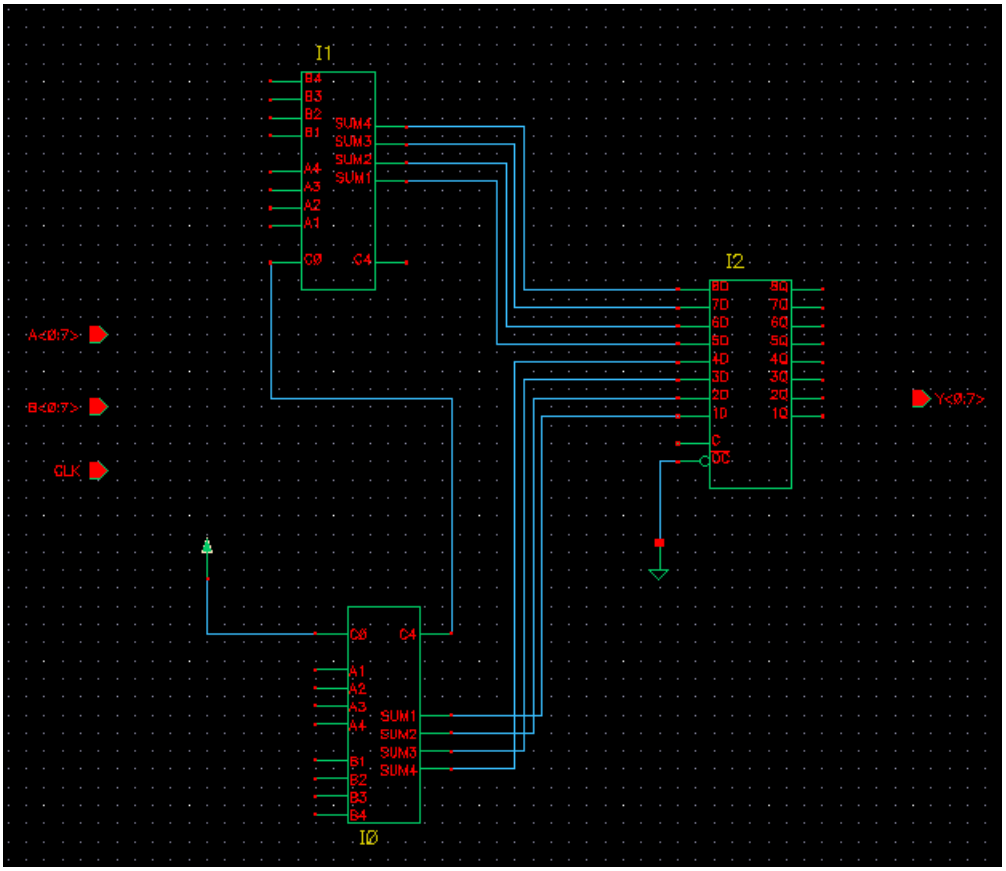
Figure 5-13 The Add Wire Form

In the next steps, you wire the four lower input pins on the register symbol to the four SUM output pins on the lower adder symbol.

4. Route the `SUM4` pin on the lower adder symbol to the register `4D` pin. Click at the beginning and the ending points for the wire.

5. Similarly, route the following nets:

   `SUM3` to `3D`
   `SUM2` to `2D`
   `SUM1` to `1D`
   `C0` (on the top adder) to `C4` (on the bottom adder)
   `PWR` to `C0` (on the bottom adder)
   `GND` to `0C` (on the register)

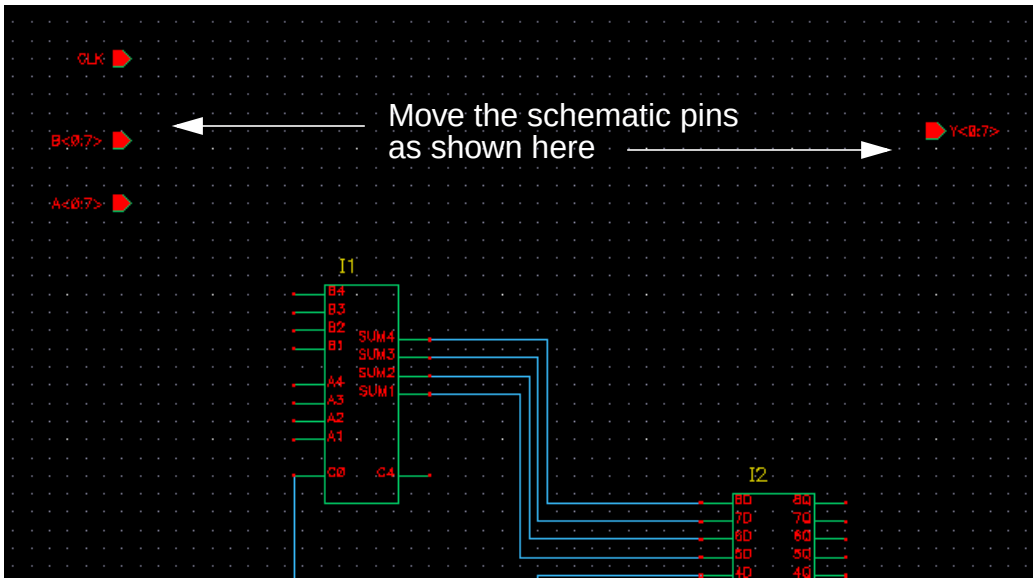


In the next section, you add three buses for the schematic input and output pins. Before you add the buses, you move the schematic pins to the locations shown in the figure.

Then, you will draw the buses using the “X-first” drawing mode, just as you did when you added buses to the top-level schematic.

Moving the Schematic Pins for Space

1. Choose *Edit – Move*.
2. Select the `CLK`, `B<0:7>`, and `A<0:7>` input pins (drag a box around them with the mouse).
3. Click on the pins you selected to verify that you want to move them.
4. Position the pins in the top left corner of the schematic (see the figure) and click to place them.
5. Select the `Y<0:7>` output pin by clicking on it.
6. Position the output pin in the top right corner and click to place it.



Note: Take care over the order of the pins on the left: `CLK`, `B<0:7>`, `A<0:7>`

Editing commands, such as *Move*, work differently depending on whether you select the command first or select the objects first. When you select the command first, the objects are automatically deselected after the command executes, but the command remains active. When you select the objects first, the objects are not deselected, but the command is automatically canceled.

Drawing the Buses

You will now use the same procedure that you used to create the top-level buses) see Adding the DEC Bus on page 40).

1. Choose *Add – Wire (wide)*.
2. Press the F3 function key to open the Add Wire form.
3. Set the *Draw Mode* cyclic field to the “X-first” drawing mode.

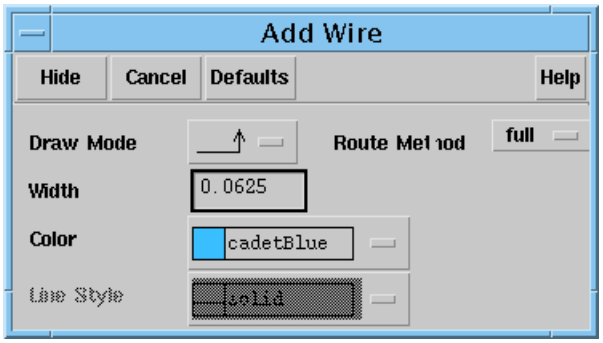


Figure 5-14 The Add Wire Form

4. Draw the buses, clicking twice to end each bus.

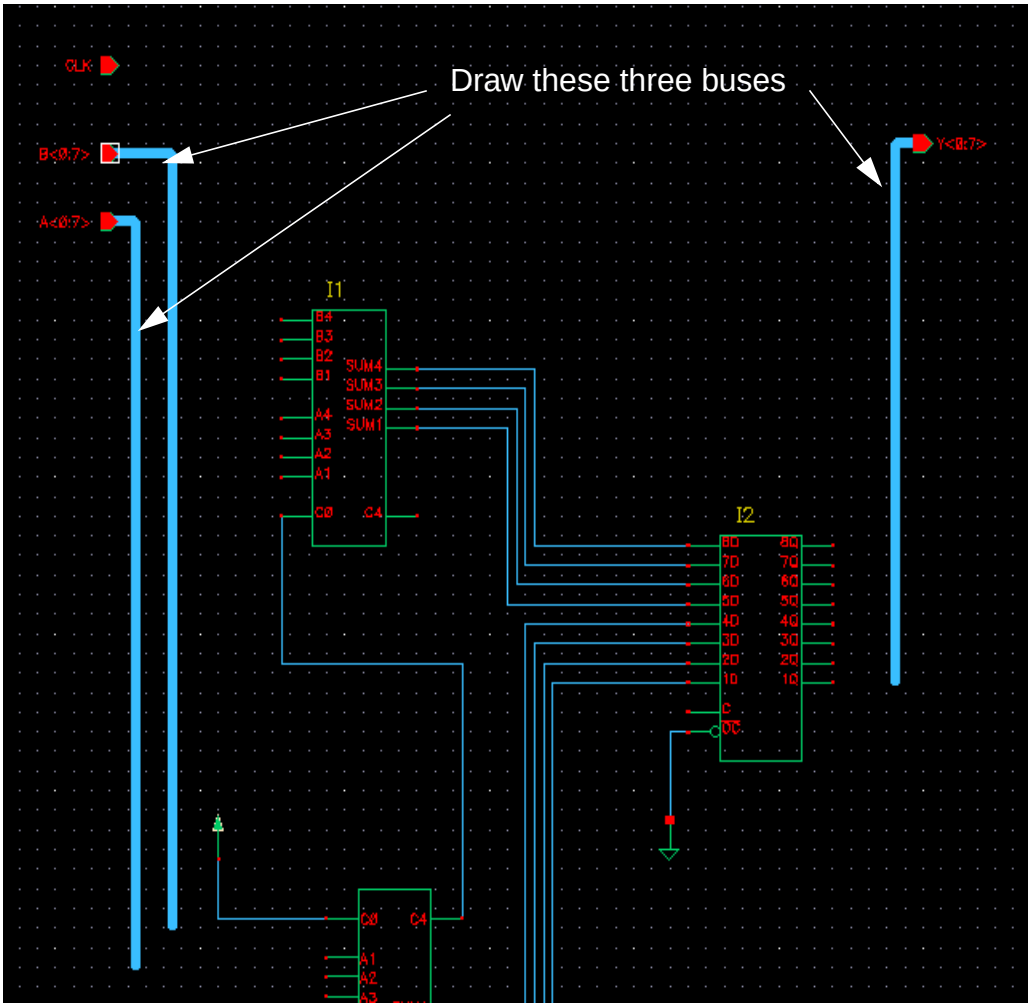


Figure 5-15 The Three Wire Buses Added

In the next section, you will wire the CLK pin and tap the buses to connect the symbol pins. To speed up the process, you use the *Copy* command to copy wire arrays.

Wiring the CLK Pin

1. Choose *Add – Wire (narrow)*.
2. Press the F3 function key to open the Add Wire form.
3. Click the *Defaults* button to set *Draw Mode* to full routing.
4. Click the *Hide* button.
5. Route the CLK pin to the C input pin on the register symbol.

   You must place the first segment yourself (to help the router place it appropriately).

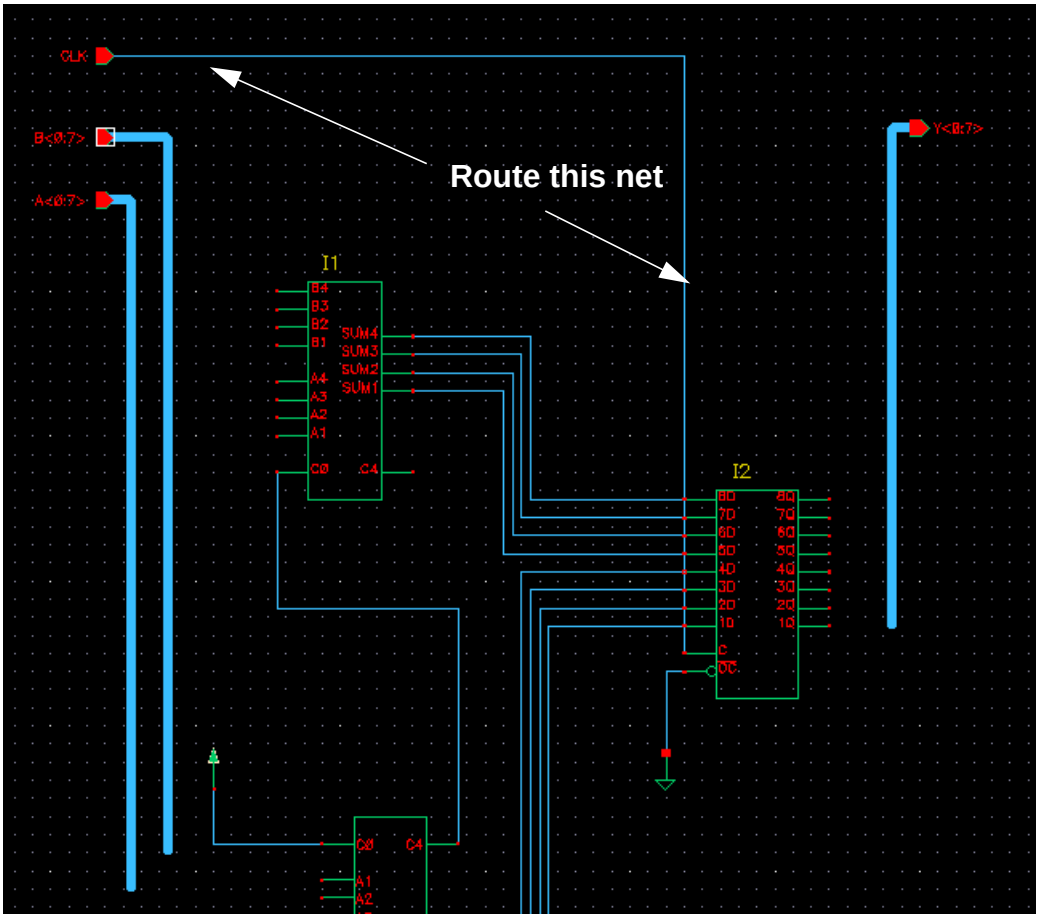


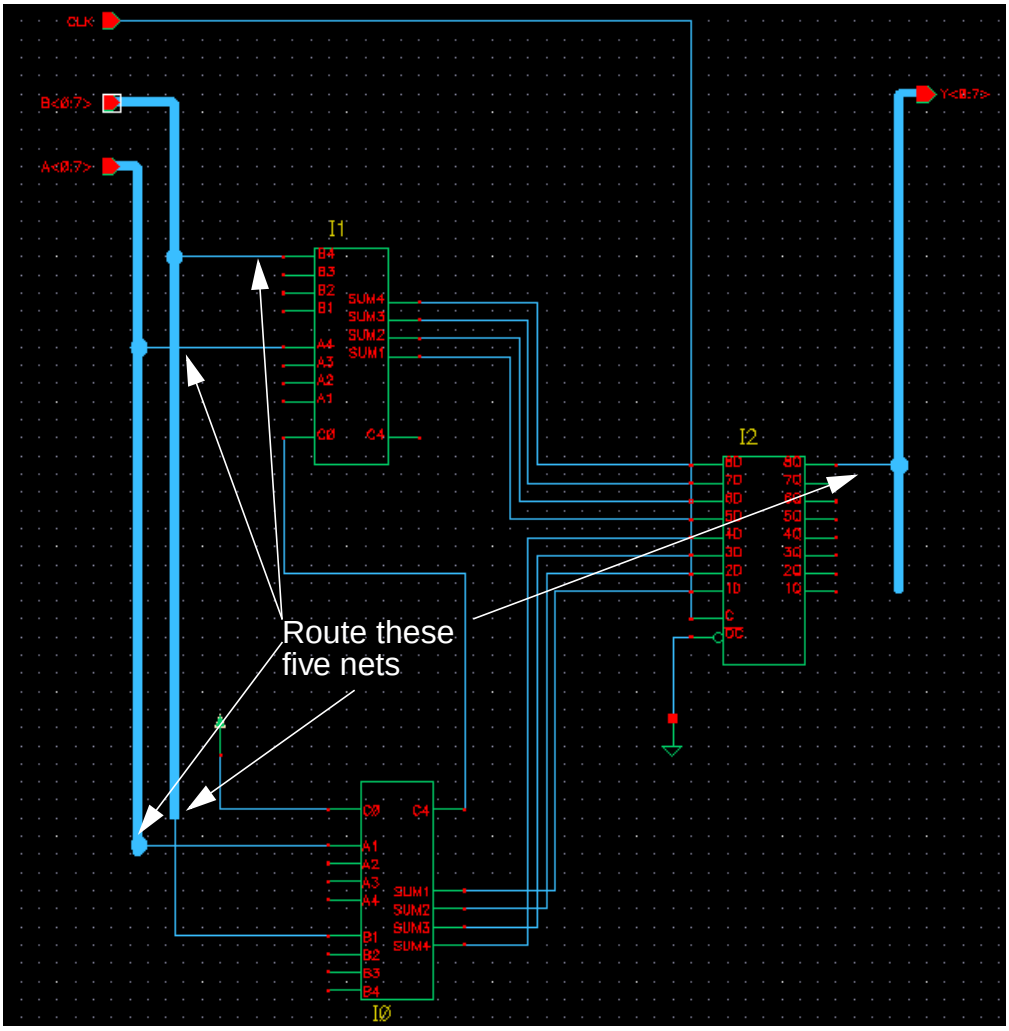
Figure 5-16 Wiring The CLK Pin

Wiring the Adders

1. Route these nets:

   Note: Check your work carefully to be sure that you connect each pin to the correct bus.

   - ❑ Pin B4 on the top adder symbol to the B bus
   - ❑ Pin A4 on the top adder symbol to the A bus
   - ❑ Pin A1 on the bottom adder symbol to the A bus
   - ❑ Pin B1 on the bottom adder symbol to the B bus
   - ❑ Pin 8Q on the register symbol to the Y bus



Next, you copy each of these nets to complete the wiring for the functions.

2. Choose *Edit – Copy*.

   The status bar displays

   `Point at reference point to copy`

3. With the pointer in the schematic window, press the F3 function key to display the Copy form.

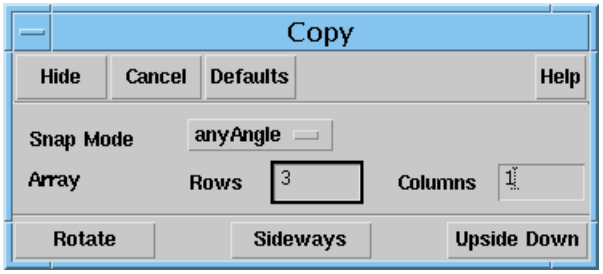
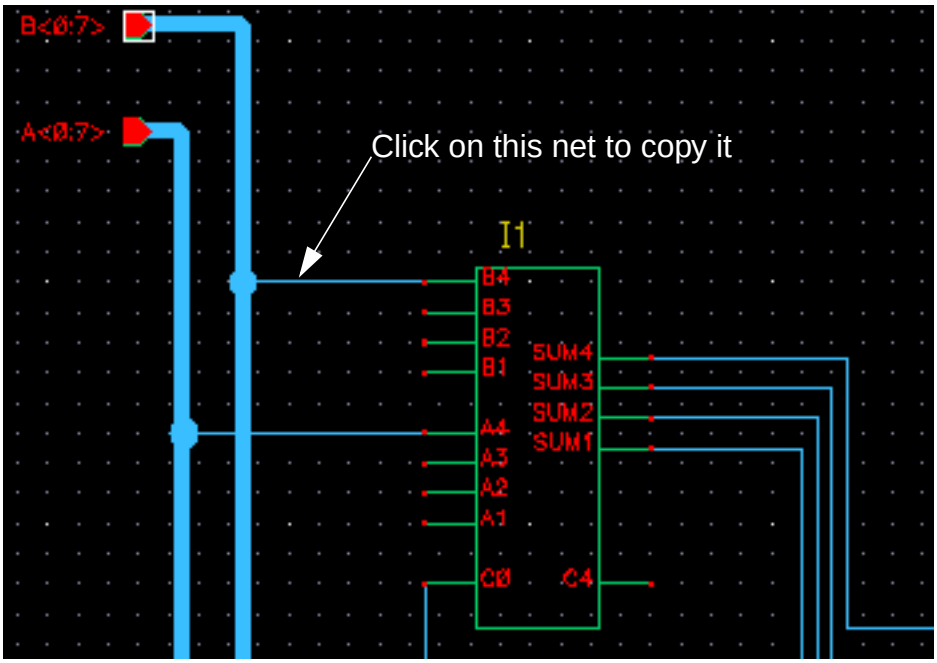


Figure 5-17 The Copy Form

4. In the *Rows* field, type 3 to indicate that you want to make three copies of the first net.
5. Click on the top input net on the top adder symbol to indicate that you want to copy it.



   A second net appears, highlighted in yellow.

6. Position the second net and click to place it.

The system anticipates the next two copies, giving you two more nets to place simultaneously.

7. Position the remaining nets with the pointer.
8. Click to place them.

   Solder dots appear, indicating that the nets are connected to the bus.
9. Copy and place the remaining input nets.

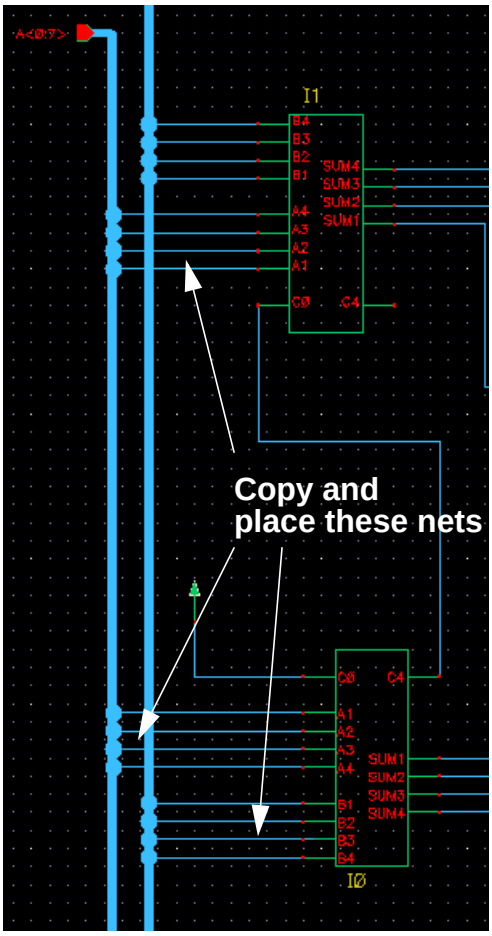


Figure 5-18 Copying And Placing Nets

a. Start by clicking on the first net of each set as you did before.

b. Then, position and click to place each net copy. Watch the prompt line to keep track of your next step.

In the next section, you create a seven-wire array for wiring the register.

Wiring the Register

1. On the Copy form, type 7 in the *Rows* field to indicate that you want to create an array of seven nets.
2. Click on the net that connects the 8Q pin on the register symbol to copy it.

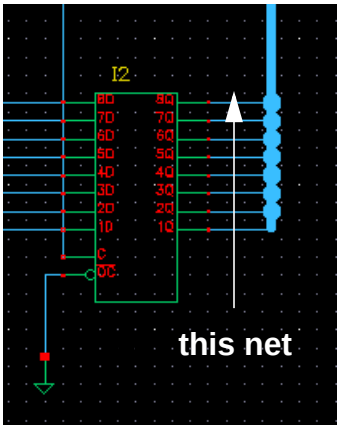


Figure 5-19 Copying the Nets on the 8Q Pin

3. Position the second net with the pointer and click to place it.
4. Position the remaining nets with the pointer and click to place them.

Naming the Nets

In this section, you will name the single-bit input and output nets using the array feature to create the names. You will use the same process that you used to name nets on the top-level schematic.

Naming the Nets That Tap the B Bus

To name the nets that tap the B bus, do the following:

1. Choose *Add – Wire Name* to display the Add Wire Name form.

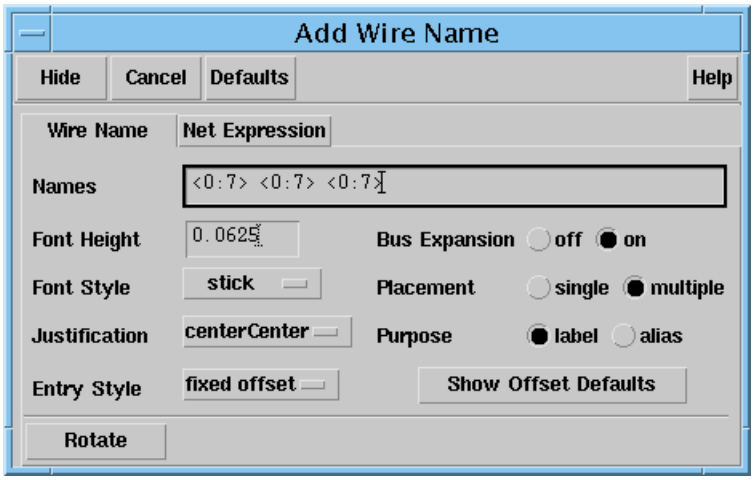


Figure 5-20 The Add Wire Name Form

You need to create three sets of seven names:

- One set for the A pins on the adder
- One set for the B pins on the adder
- One set for the Q pins on the register

2. In the *Names* field, type `<0:7> <0:7> <0:7>`.
3. Turn on *Bus Expansion*.
4. Set *Justification* to *centerCenter*.
5. Set *Placement* to *multiple*.

The buses inherit the schematic pin names. The nets tapping the buses inherit the bus name, which is why you name them with the bit number only.

6. Zoom in on the bottom nets of the B bus.

   It is much easier to place the names when you zoom in.

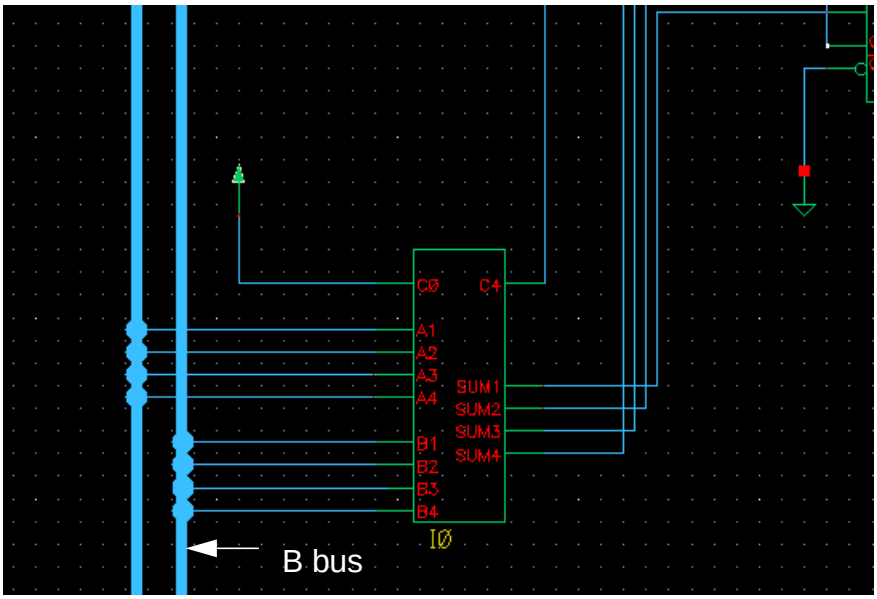


Figure 5-21 Zooming In On The B Bus

7. Click and place the names for bits 0–3 tapped from the B bus.

   Bits 0–3 from the B bus are input into pins B1 through B4, respectively, on the bottom adder symbol.

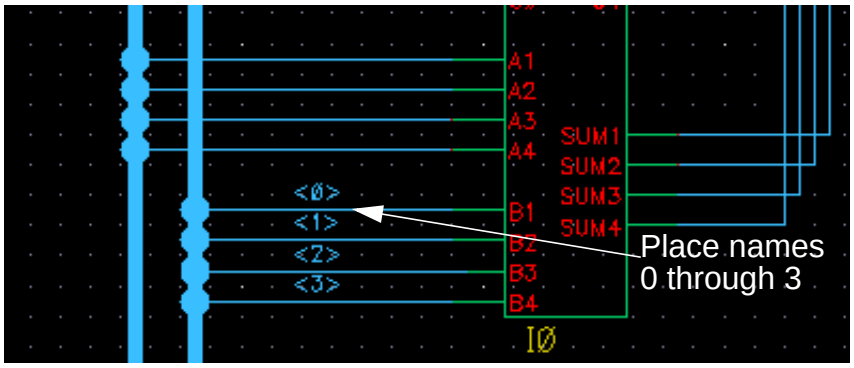


Figure 5-22 Placing The Pin Names On The B Bus

8. Press f to fit the entire schematic in the window.
9. Zoom in on the top nets for the B bus.

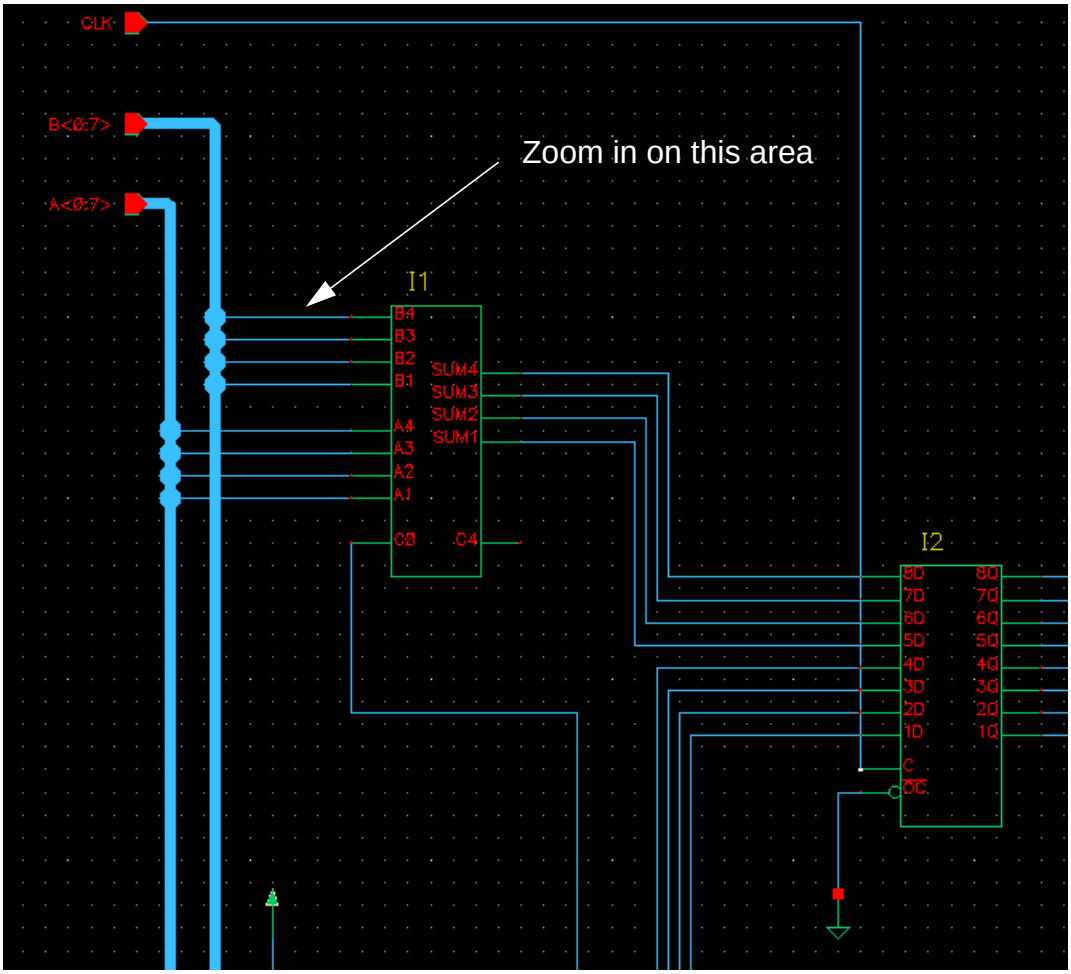


Figure 5-23 Zooming In To The Top Of The B Bus

10. Place the names for bits 4–7 tapped from the B bus, starting with the bottom net.

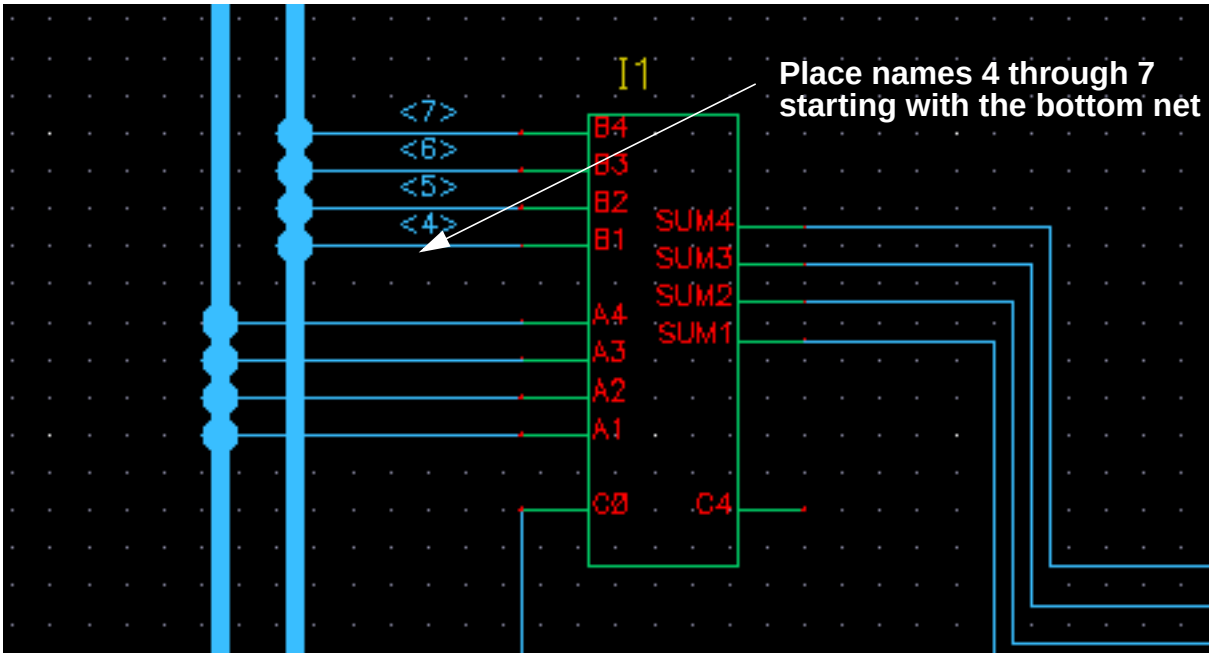


Figure 5-24 Placing Bits 4-7 On The B Bus

Bits 4–7 from the B bus are input into pins B1 through B4, respectively, on the top adder.

11. Press f to fit the entire schematic in the window.

12. Zoom in on the bottom nets for the A bus.

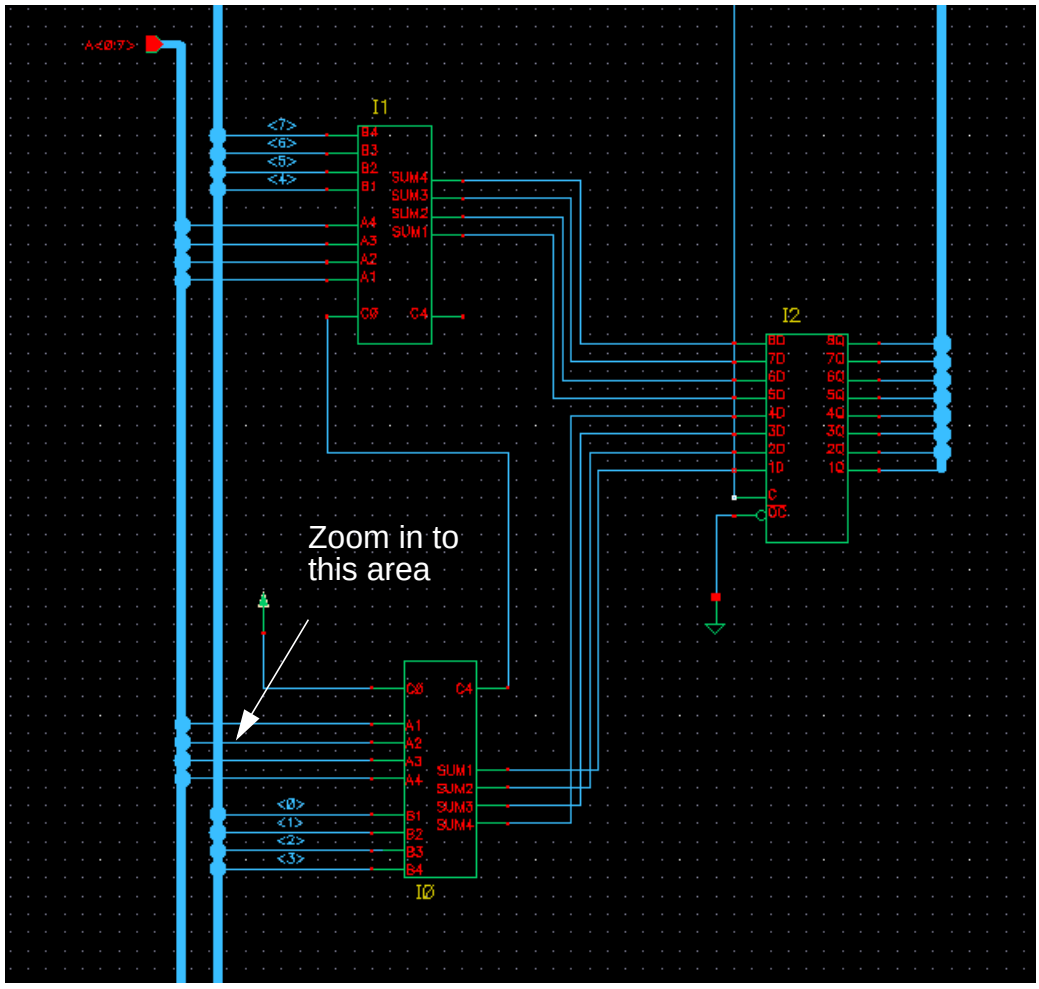


Figure 5-25 Zooming In On The A Bus

13. Place names 0–3.

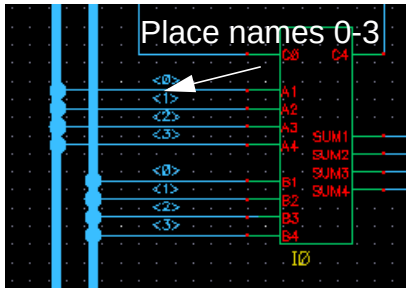


Figure 5-26 Placing Names 0-3 On The A Bus

14. Press f to fit the entire schematic in the window.

15. Zoom in on the top nets for the A bus.

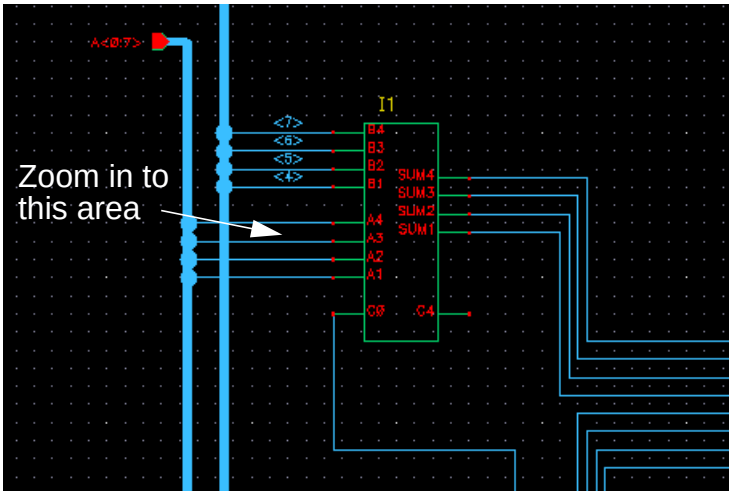


Figure 5-27 Zooming In On The Top Nets Of The A Bus

16. Place the names for bits 4–7 tapped from the A bus, starting with the bottom net.

Bits 4–7 from the A bus are input into pins A1 through A4, respectively, on the top adder.

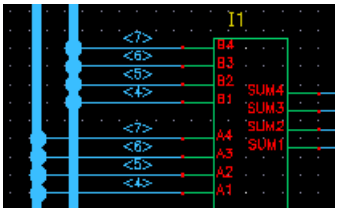


Figure 5-28 Placing The 4-7 Bits On The A Bus

17. Press f to fit the entire schematic in the window.

Naming the Nets That Tap the Y Bus

1. Zoom in on the nets tapping the `Y` bus.
2. Place the names for the nets to the `Y` bus.

   Bits `<0>` through `<7>` are output from pins `1Q` through `8Q`, respectively.

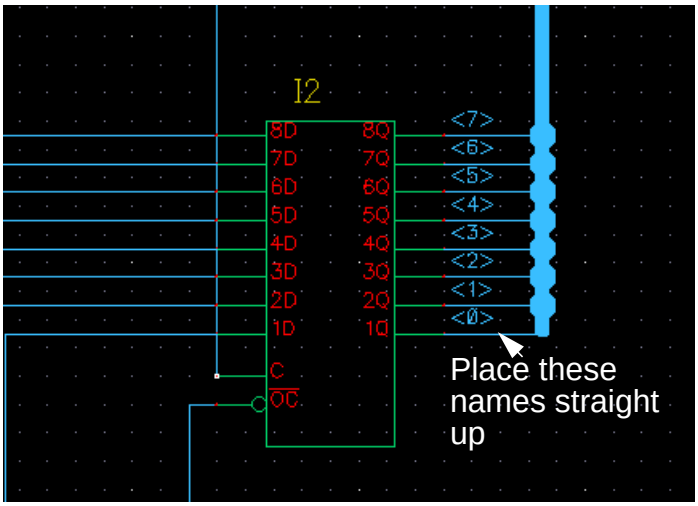


Figure 5-29 Placing Nets On The Y Bus

3. Press `f` to fit the entire schematic in the window.
4. Press `Esc` to cancel the command.
5. Save your schematic.

6

Creating the Analog Amplifier Schematic

Learning Objectives

In this chapter, you will create the schematic for a single transistor amplifier with analog components using the following procedures:

- Use a bottom-up design approach in the Virtuoso® schematic editor software
- Use a standard Cadence® parts library
- Create an analog design from discrete instances
- Use the Add Instance and Edit Object Properties forms to change the values of instance parameters
- Use the Component Description Format (CDF) editor to create a new instance parameter
- Create a new symbol cellview automatically, based on an existing schematic cellview
- Add symbols from a standard Cadence library
- Select and move objects and wired pins with dynamic editing

About the Analog Amplifier Schematic

The amplifier schematic that you will create contains:

- Four resistors
- One npn transistor
- One output capacitor
- One output pin and one input pin

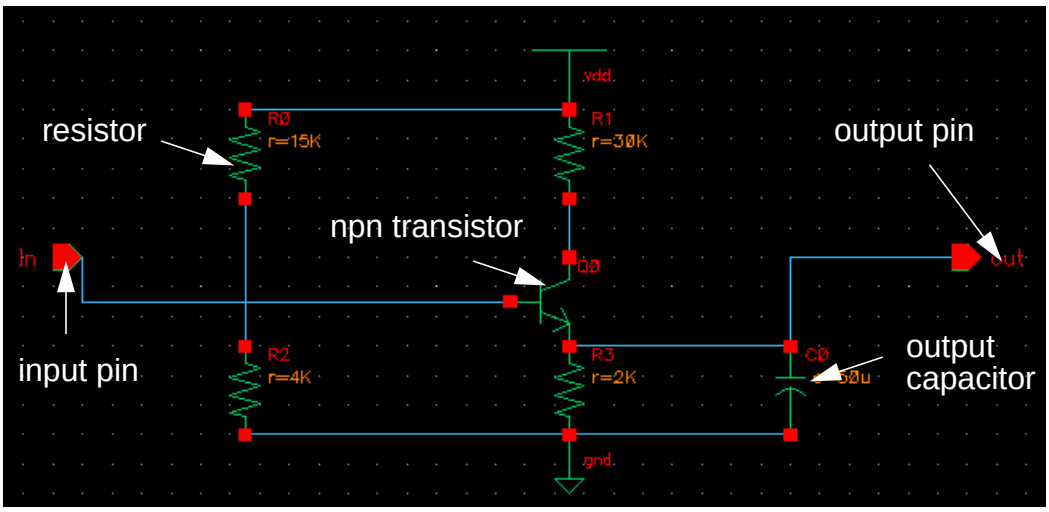


Figure 6-1 The Analog Amplifier Schematic

Creating the amp Schematic Cellview

In this section, you create the *amp* schematic cellview from discrete parts in a bottom-up design.

1. Start the Virtuoso schematic editor software (unless it is already running).
2. From the CIW, choose *Options – User Preferences* to set the environment options.
   a. Set *Infix* and *Scroll Bars* to *on*
   b. Change the *Undo Limit* to 10.

   Because no *amp* schematic cellview exists, you must create it.
3. Choose *File – New – Cellview* to display the Create New File form.

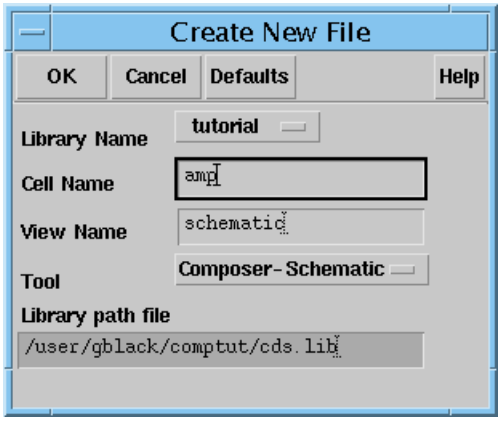


Figure 6-2 The Create New File Form

4. Set the *Library Name* cyclic field to `tutorial`.
5. In the *Cell Name* field, type `amp`.
6. In the *View Name* field, type `schematic`.
7. Set the *Tool* cyclic field to *Composer – Schematic*.
8. Click *OK*.

   The schematic editor opens, displaying an empty design window.

You are now ready to create the *amp* schematic.

Adding Symbols for the Four Resistors

1. Choose *Add – Instance*.

   The Add Instance form appears.

2. In the *Library* field, type `analogLib`.

   The *analogLib* library contains cells for analog functions.

3. In the *Cell* field, type `res`.

   The Add Instance form expands to reveal an instance parameters section.

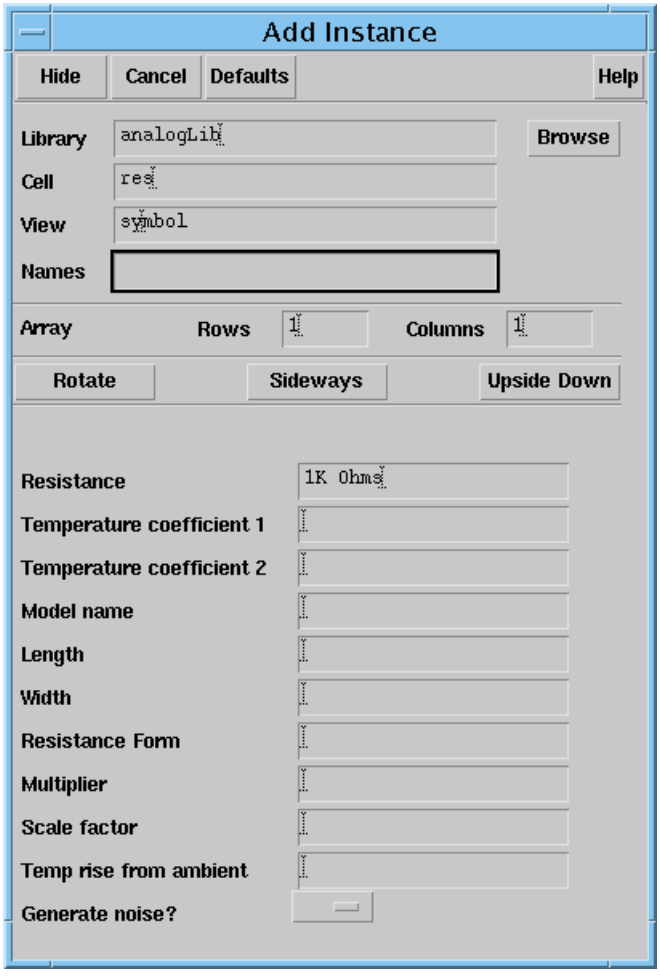


Figure 6-3 The Add Instance Form

4. Position the first resistor symbol, `R0`, at the bottom of the schematic window and click to place it.

5. Place the remaining three resistors (R1, R2, R3) in the pattern shown.

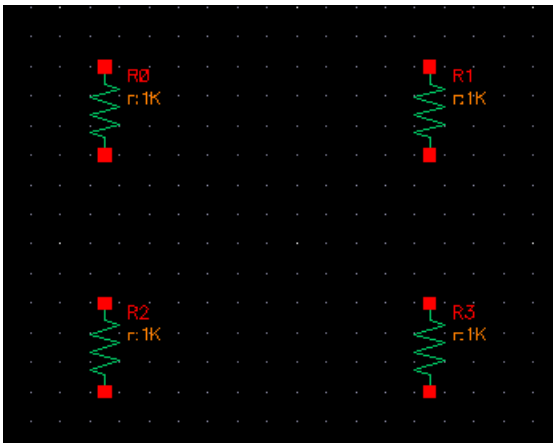


Figure 6-4 Placing The Resistors

6. With the pointer in the schematic window, press Esc to cancel the *Add – Instance* command.

Changing Resistor Parameter Values

The analog instances in the amplifier design are generic devices with a few basic default values for their parameters. Each resistor that you add from the *analogLib* library has a default resistance value of 1 Kohms (ohms is implied). The resistance is defined as the parameter `r`. You must change the resistance of each resistor from its default value to the value needed in the design.

1. From the schematic editing window choose *Edit – Properties – Objects*.
2. Move the pointer over the resistor R1 and click to display the Edit Object Properties form.

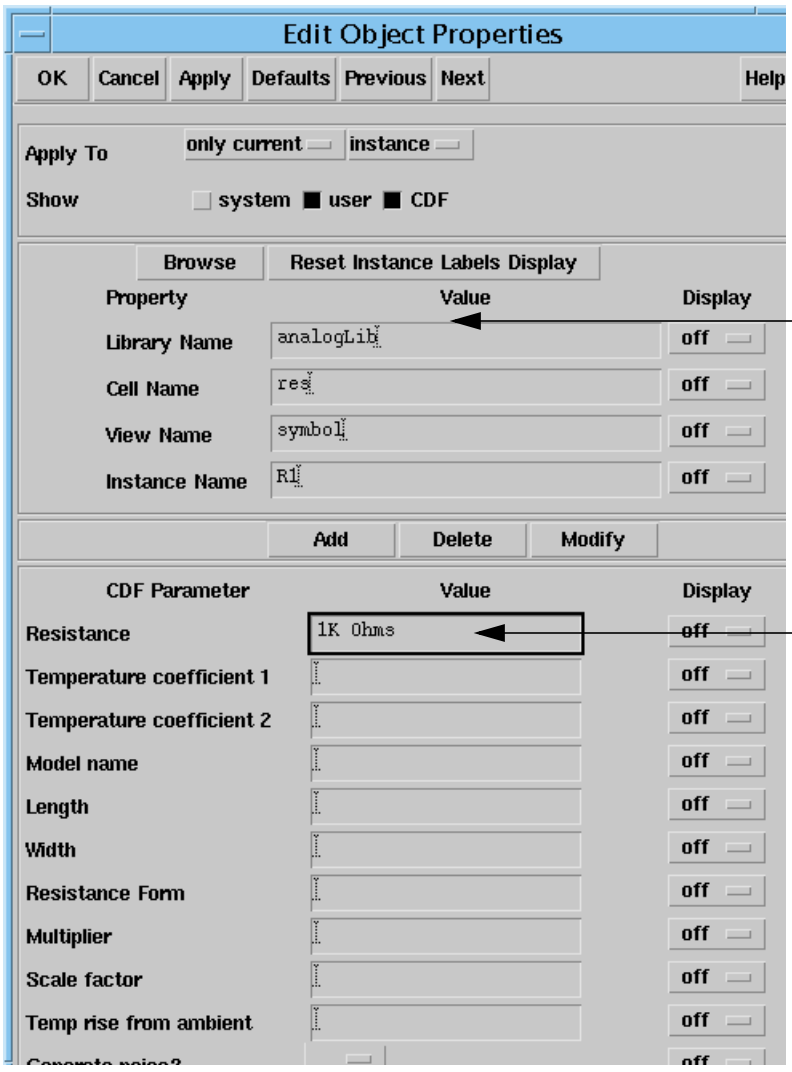


Figure 6-5 The Edit Object Properties Form

The message in the CIW changes to

```
Edit the properties on the form or select another object.
```

3. In the *Resistance* field, type `30K`.
4. Click *Apply*.

   The schematic display changes, showing the new `r` value of `30K` for `R1`.

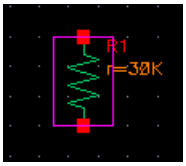


Figure 6-6 R1 With New Resistance Value Of 30K

5. Move the pointer back in the design window and click on `R2`.
6. In the *Resistance* field, type `4K`.
7. Click *Apply*.
8. Repeat the process for `R3` and `R0`. Set `R3` to `2K` and `R0` to `15K`.

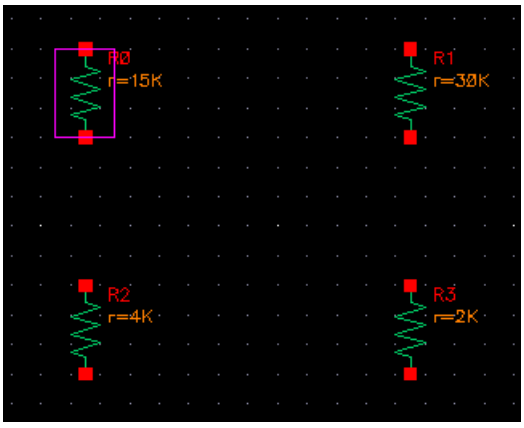


Figure 6-7 All Resistance Values Added

Note: You can use `K` and other standard notation when entering instance parameter values. If you type a long number such as 30,000, the system puts 30,000 on the schematic. If you erase the word `ohms`, don't worry. Ohms is automatically assumed for resistance. If you cancel the Edit Object Properties form and open it again, the word `ohms` has returned to the *Resistance* field.

9. Click *Cancel* to close the Edit Object Properties form.

The Edit Object Properties form displayed many other parameters associated with the resistor cell. These parameters are titled *CDF Parameters* because CDF, Component Description Format, is the format used in Cadence software to describe the features and behavior of each type of device. The CDF description for a cell can include information for simulation, layout, and label display. You will use the CDF editor later in this chapter.

Note: For more information about CDF, see the *Component Description Format User Guide*.

Adding a Capacitor and Changing Its Parameter Values

You can change instance parameter values (properties) as you place instances.

Change the capacitance value of the capacitor as you add it.

1. Choose *Add – Instance*.

   The Add Instance form appears. Unless you have used it for something else, *Library* should still say `analogLib`.

2. In the *Cell* field, type `cap`.

3. In the *Capacitance* field, type `50u`.

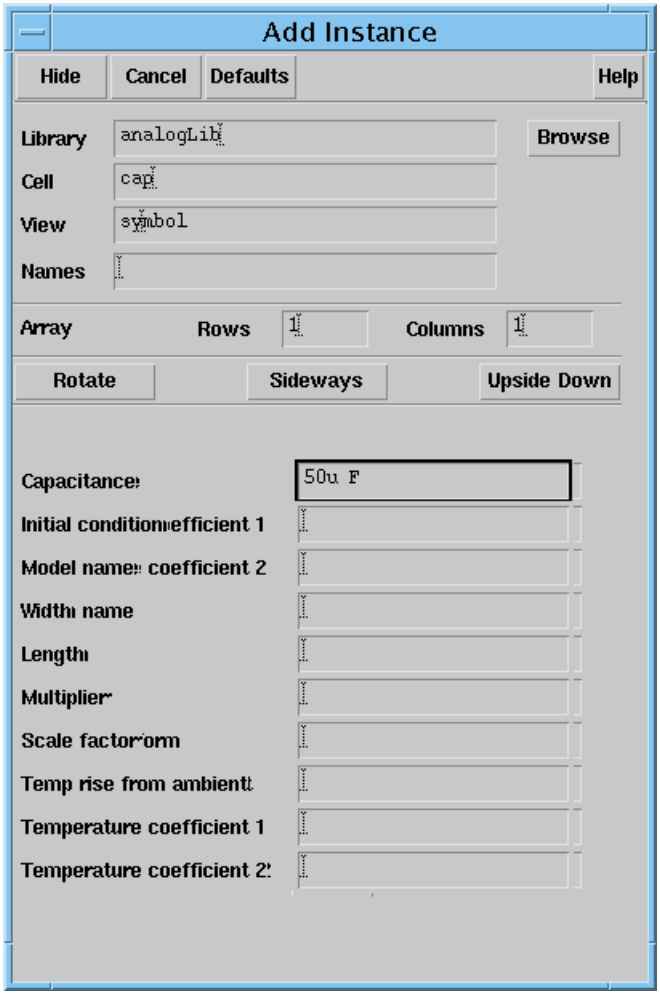


Figure 6-8 The Add Instance Form

4. Position the capacitor symbol to the right of `R3` and click.

Notice that the capacitor symbol already has a capacitance (c) equal to `50uF`, the new value you entered. If you do not include the `F`, farads is assumed.

In the next section, you add the power and ground symbols, the transistor, the I/O pins, and the wiring.

Adding Symbols for the Power and Ground

Add the remaining instances and wire them together. You can use the CDF editor after you finish the *amp* schematic.

To add symbols for the power and ground, do the following:

1. Choose *Add – Instance*.

   The *Library* field should still say `analogLib`.

2. In the *Cell* field, type `vdd`.

   The form reconfigures itself again for the new instance.

3. Position the `vdd` symbol on top of the top pin on the `R1` symbol and click to place it.

   The shape of the `vdd` symbol continues to follow the pointer.

4. On the Add Instance form, change the *Cell* field from `vdd` to `gnd`.

5. Position the `gnd` symbol at the bottom of the `R3` symbol.

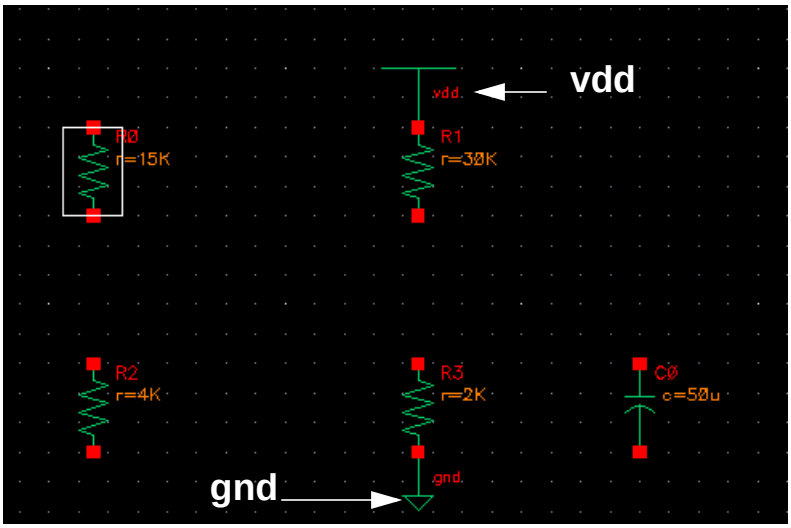


Figure 6-9 Adding vdd and gnd

Adding the Transistor Symbol

1. On the Add Instance form, change the *Cell* field from gnd to npn.

   The form updates to show the instance parameters for the transistor.

2. Position the transistor with the emitter pin on the top pin of R3. Click to place the transistor.

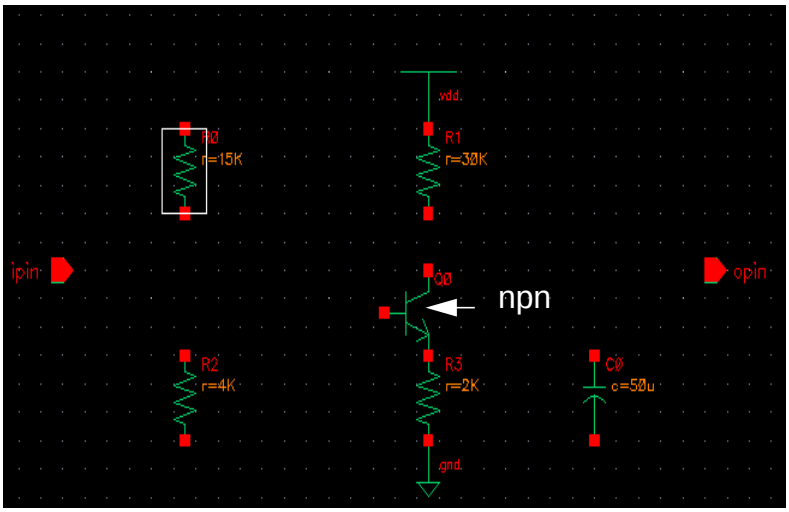


Figure 6-10 The Transistor Symbol Added

Adding the I/O Pins

1. On the Add Instance form, change the *Library* field from `analogLib` to `basic`.
2. In the *Cell* field, replace `gnd` with `ipin`.
3. Position the input pin on the left side of the schematic.
4. In the *Cell* field, replace `ipin` with `opin`.
5. Position the output pin on the right side of the schematic.

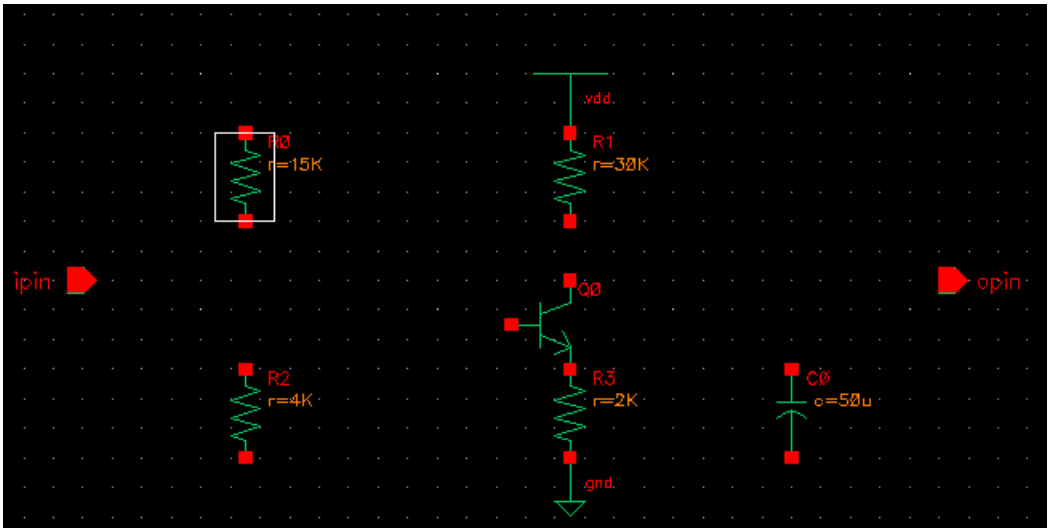


Figure 6-11 The ipin and opin Added

6. Press `Esc` to cancel the *Add – Instance* command.

Aligning the Symbols

Using dynamic editing, you can use the mouse to select and move objects in a schematic without selecting a command first.

1. Put the pointer on the `vdd` symbol of `R1` and click.
2. Simultaneously, press the `Shift` key and click over the `power` symbol of `R1`.

   A single highlight box appears around both symbols of `R1`.

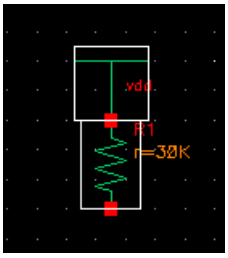


Figure 6-12 Highlighting Multiple Symbols

3. Click and drag the pointer down and to the R3 transistor until the bottom pin of `R1` is over the transistor collector pin of `R3`, then release.

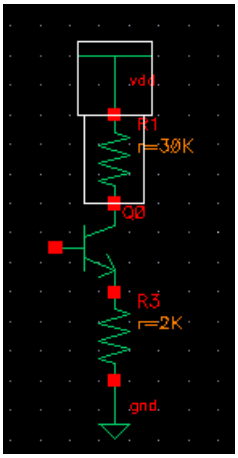


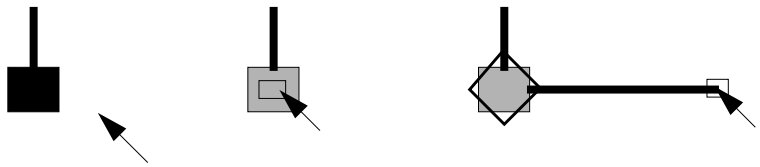
Figure 6-13 Aligning The R1 and R3 Symbols

Wiring the Schematic

You can wire without using the *Wire (thin)* command. Dynamic editing allows you to use the mouse to wire the schematic from pin to pin.

1. To route a thin wire with the mouse, position the pointer exactly on top of the starting pin.

   The pin becomes highlighted and a small square appears on the pin. Be careful not to select a label or an instance. If you accidently tear off a label or move an instance, choose *Edit – Undo*.



2. Click and drag the pointer to all destination pins as shown in the figure below. A wire-routing line appears. A diamond appears on the starting pin, while the small square follows the pointer.
3. Wire the instances together until your schematic looks as follows:

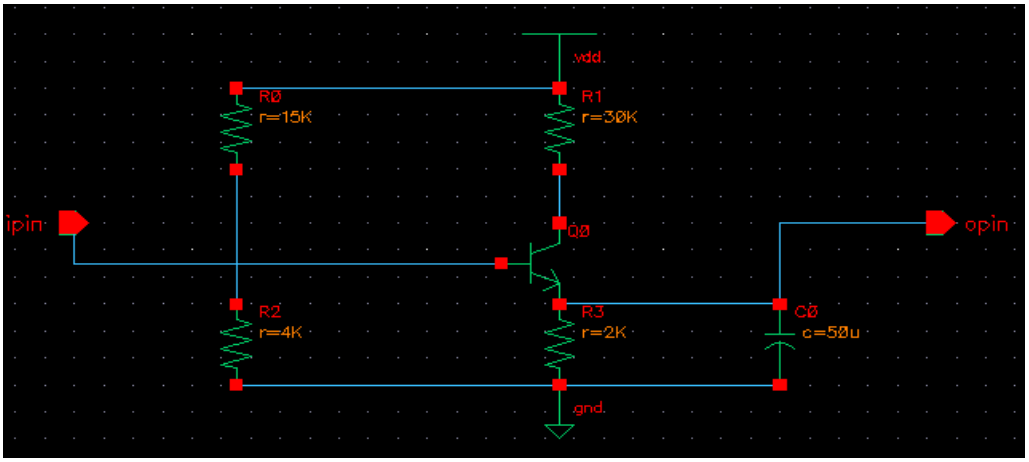


Figure 6-14 Fully Wired Schematic

Note: If you try to draw a line to a point where a resistor and the power or ground symbol are connected pin to pin, you might get a dashed line in a different color rather than a normal, solid wire. This line is a flightline. Flightlines instead of wires appear in designs because the wire router would have to violate a routing rule to make a connection.

4. If you get any flight lines while wiring the schematic, delete the flight lines, pull the instances apart so that wires appear between them, and complete the wiring.

Cleaning Up the Schematic

1. Choose *Check – Rules Setup.*
2. Click *Defaults*.
3. Click on the *Check and Save* icon.

   The CIW reports no errors.
4. Change the generic I/O pin labels.

   a. To label the I/O pins *in* and *out*, click on the *Property* icon to display the Edit Object Properties form.

   b. Select the output pin label *opin*. There are no fields on the form that you can change.

Do not use generic I/O pins. You do not want to finish your design with the generic pin labels ipin and opin. Always use Add – Pin to add pins to a schematic.

   c. Delete both I/O pins.

   d. Choose *Add – Pin* and place a new input pin *in* and a new output pin *out* from the *basic* library. Remember to change *Direction* to *output* before placing the *out* pin.

   e. Press the F3 function key to bring back the Edit Object Properties form.

   f. Select the *out* pin.

   g. The Edit Object Properties form fields for the *out* pin are different from the fields for the *opin* pin. You can edit the name and you have choices regarding direction, display, and usage.

   h. Click *Cancel*.
5. Choose *Check and Save* to save the schematic with the new I/O pins.

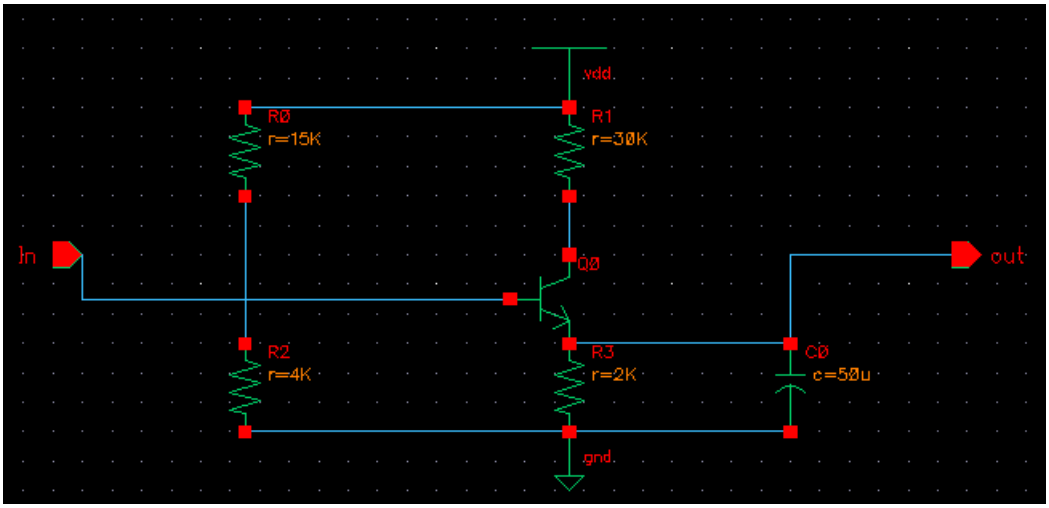


Figure 6-15 The In and Out Pins Renamed

In the next section, you will enter CDF data for the transistor.

Adding CDF Data

Every device in the *amp* schematic has a unique value that you gave it except for the transistor.

You used the Add Instance and Edit Properties commands to change the properties of the capacitor and resistors. In this section, you use the CDF editor to add properties to the transistor `Q0`.

1. Click on the *Property* icon to display the Edit Object Properties form.
2. Click on the transistor in the *amp* schematic.

   The Edit Object Properties form has a *CDF Parameter* field for the *Collector-emitter voltage*, but there is no entry for the `Beta forward` CDF parameter. You must use the CDF editor to create the `Beta forward` parameter and add it to this form.
3. In the CIW, start the CDF editor by choosing *Tools – CDF – Edit* to display the Edit Component CDF form.
4. In the *Library Name* field, type `analogLib`.
5. In the *Cell Name* field, type `npn`.

   Leave *CDF Selection* set to *Cell* and *CDF Type* set to *Effective*.

   The Edit Component CDF form expands to display information for the *npn* cell.

6. In the *Component Parameters* section, click *Add* to display the Add CDF Parameters form.

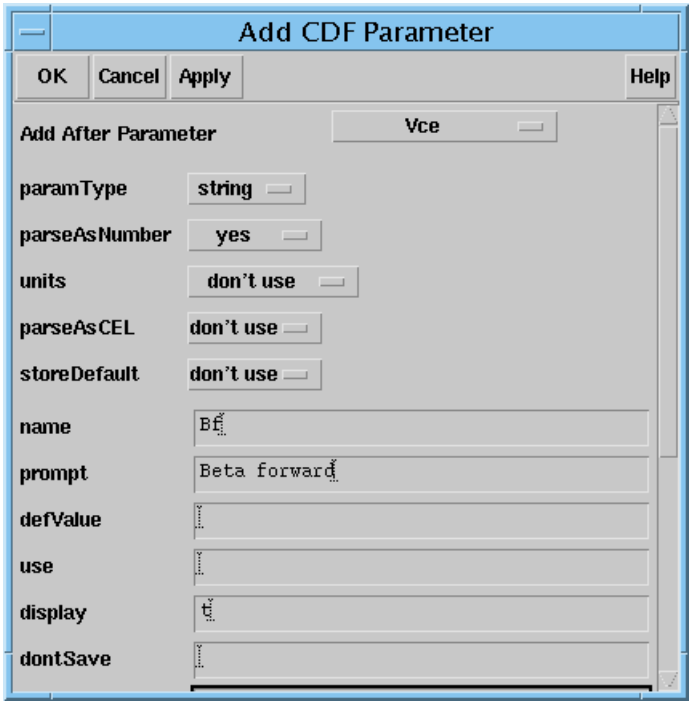


Figure 6-16 The Add CDF Parameter Form

7. Set *Add After Parameter* to *Vce*.
8. Set *parseAsNumber* to *yes*.
9. In the *name* field, type `Bf`.
10. In the *prompt* field, type `Beta forward`.
11. In the *display* field, type `t`.
12. In the *editable* field, type `t`.
13. Click *OK*.

    The `Bf` parameter is added to the list of CDF parameters on the Edit Component CDF form.
14. Click *OK* on the Edit Component CDF form.
15. On the *amp* schematic, select the transistor and edit its properties.

The *Beta forward* field should now appear on the Edit Object Properties form as a user property.

16. In the *Beta forward* field, type `40`.

17. Click *OK*.

18. Choose *Check and Save* to save the schematic one last time.

In the next section, you will create a symbol for the *amp* schematic.

Creating a Symbol from a Schematic

You now have a complete, checked and saved schematic cellview for the cell *amp*. To use *amp* as an element in other designs, you now create a symbol cellview for *amp*.

1. Choose *Design – Create Cellview – From Cellview to* display the Cellview From Cellview form.

   The form shows entries for the active design. *Library Name* should be `tutorial`, *Cell Name* should be `amp`, and *From View Name* should be *schematic*. Make sure that *To View Name* is `symbol`.

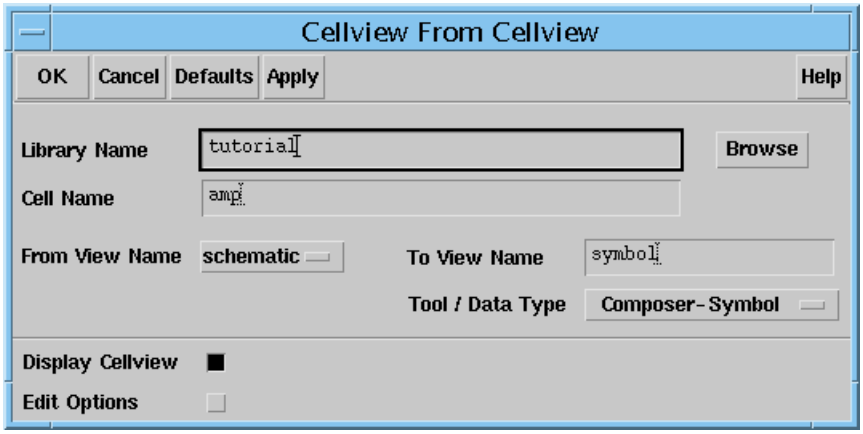


Figure 6-17 The Cellview From Cellview Form

2. Click *OK*.

   The symbol editor window appears, displaying the *amp* symbol generated by the schematic editor software.

Figure 6-18 The Generated amp Symbol

The automatically generated symbol is functional, with an input pin and an output pin, but it is a simple rectangle. The standard symbol for an amplifier is a triangle, with the output at its apex.

Use the symbol editor to replace the rectangle with a triangle pointing towards the output pin.

3. In the symbol editor window, choose *Add – Shape – Polygon*.

   The CIW displays

   ```
   Point at first point of polygon
   ```

4. Click the pointer just outside of the output pin.

   The CIW displays

   ```
   Point at next point of polygon
   ```

5. Click below the base of the input pin. Then, move straight up and click above the input pin. Finally, click on your original starting point.

   You should have formed a triangle around the component:

6. With the pointer in the schematic window, press `Esc` to cancel the *Add – Shape – Polygon* command.

7. Carefully select the inner box and delete it. Do not delete the outside box that runs through the pin squares.

8. Select the top and bottom sides of the outside (selection) box and move them out to the points on the triangle, so that the whole triangle is inside the box.

   This step becomes important later, when you route wires past the symbol.

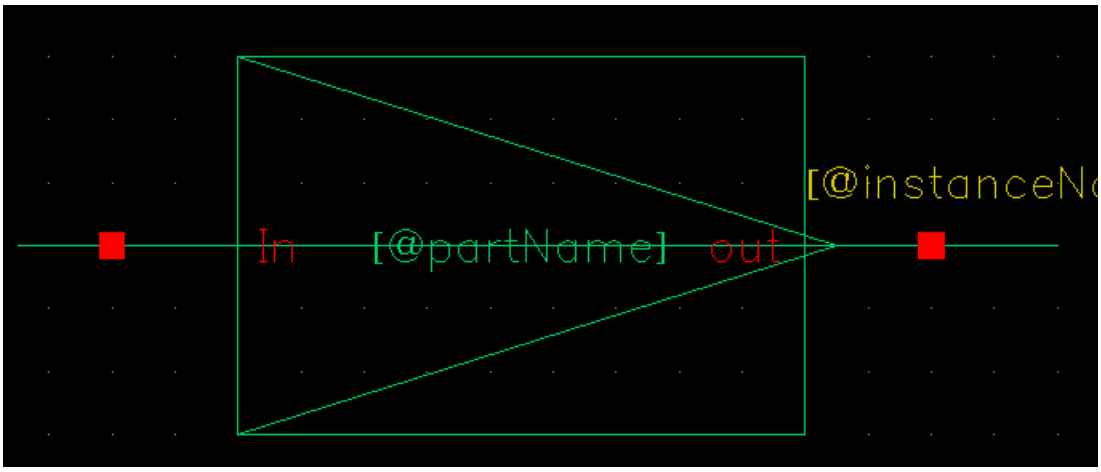


Figure 6-19 The Final Version Of The Symbol

9. Check and save the symbol using *Design – Check and Save*.

   If you look at the *amp* cell in the tutorial library, you can see that it has a schematic cellview and a symbol cellview.

10. Close the symbol editor using *Window – Close*.

11. If you have not already done so, choose *Window – Close* to close the schematic editor with the *amp* schematic.

You have completed a discrete analog amplifier design, with its own symbol, and with the instance parameters that you specified.

A

A

Solving Problems

This appendix describes how to solve problems that you might encounter as you use this tutorial.

Problem	Solution
You need to undo a command.	Press u on the keyboard, choose the *Edit – Undo* command, or click on the *Undo* icon. *Undo* does not undo window commands such as *Zoom In* or *Fit*.
You need to cancel a command.	Press Esc with the pointer on the schematic window or click the *Cancel* button on the command form.
You zoomed in on the wrong part of the schematic.	Press f on the keyboard to redisplay the entire schematic and then zoom in again.
The software performs an unexpected command.	Undo the command. Then, check the prompt line for a command prompt. You might need to cancel the previous command form.
No form opens when you choose *Add – Instance*.	Click on the *Command Options* icon.

Problem	Solution
You have trouble selecting an object.	Zoom in on the area around the object. After you zoom in, you might be able to select the object more easily. If you still cannot select the object, **1.** Choose *Edit – Select – Filter* to display the Selection Options form. This form defines the types of objects you can select. **2.** Turn on the button for the object you are selecting if it is set to off. (When the button is set to off, you cannot select the object.) **3.** Click *OK* on the form and select the object. If you cannot select the object without also selecting other objects around it, **1.** Choose *Edit – Select – Filter* to display the Selection Options form. **2.** Turn off the buttons for all types of objects other than the type you are selecting. **3.** Click *Apply*. **4.** Choose the object. (Now you will not be able to select any other type of object.) **5.** When you finish, turn all the buttons on the form back on and click *OK*.
You need to deselect one or more objects.	To deselect all selected objects, click on the schematic outside the objects. To deselect one object at a time, `Control`-click each object in turn. (Hold down the `Control` key and click.)

Problem	Solution
You need to delete one or more objects.	To delete one object, **1.** Click on the object to select it. **2.** Press the `Delete` key. To delete multiple objects, **1.** Choose the objects by either ❑ Dragging a box around the objects ❑ Clicking on the first object to select it and then `Shift`-click on additional objects to select them **2.** Press the `Delete` key. You can also activate the *Delete* command by pressing `Delete` or clicking on the *Delete* icon. While *Delete* is active, you will delete each object you click on. Cancel *Delete* by pressing `Esc` (or the *Cancel* button on the Delete form).
You cannot select a command from a pop-up menu.	You must click the middle mouse button—not the left mouse button—to select a command from a pop-up menu.
You cannot close a pop-up menu.	Move the pointer off the menu (move it anywhere on the schematic other than on the menu) and click the middle mouse button.
You pick up and move an object when you are trying to select an area or group of objects.	Release the mouse button and click on the *Undo* icon.
You cannot move an object.	Press `M` to activate the *Move* command. Then follow the prompts in the prompt line.
You need to stretch an object.	Press `m` to activate the *Stretch* command. Then follow the prompts in the prompt line.
You need to move multiple objects.	Select the objects, press `M` to activate the *Move* command, and follow the prompts in the prompt line.
You need to redisplay a form that you hid with the *Hide* button.	With the pointer on the schematic window, press `F3`, or double-click the middle mouse button, or click on the *Command Options* icon.

Problem	Solution
One of your nets is not connected.	You can delete the net and create it again, or you can stretch the net. Press `m` to activate the *Stretch* command. Then follow the prompts in the prompt line.
You cannot undo a selected object; that is, an object outlined in white.	*Undo* does not undo a selection. To deselect an object, click on the object.