Titre

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1 Questions to chapter 3

1.1 Flow diagram for the `delay` subroutine

1.2 Calculating `delaycount` in order to achieve `1 ms` in `delay`'s inner-loop

We have $\frac{50\ [MHz\ op]}{4\ [\frac{op}{loop}]\ 1000\ [\frac{ms}{s}]} = 12'500[\frac{loops}{ms}]$, so we would set `delaycount` to 12'500.

Experimentally, we figured out that it should be set to 860 approx (why?)

1.3 What is BSP and what does it contain?

BSP means Board Support Package. It is the layer of software containing hardware-specific drivers and other routines that allow a particular operating system to function. It initialises the processor, bus, interrupts, clock, RAM, amongst others, and runs the boot loader.

The BSP project in Eclipse contains amongst others all the files necessary to access the LEDs, switches, buttons, etc.

1.4 What is a soft-core processor? What type of processor is present? Features?

We talk about soft-core processors when we configure a reprogrammable logic, such as a FPGA, to function as a processor. For these laboratories, we use the NIOS II soft processor, which is a soft microprocessor core for Intel FPGAs.
Clock frequency: 50 MHz; neither data nor instruction caches for NIOS II/e; No pipeline nor branch prediction for NIOS II/e.

1.5 How does the processor access peripherals? What is the main mechanism and what main piece of hardware stands between the processor and a peripheral?

Peripherals are accessed through the Avalon Switch Fabric, which lets several masters from the core to operate at the same time. In other words, in handles the requests from the masters to the slaves (peripherals).

1.6 What peripherals/IP cores are present in the provided architecture? Identify their symbolic names and base addresses.

Buttons, switches, green and red LEDs, seven segment displays, ... For the symbolic names and base addresses, see `system.h`.