UCLA Computer Science Department: CS M51A / EE M16
Logic Design of Digital Systems
Winter 2017, TR 8:00 - 9:50am, Boelter 3400
Office hours: TR 1:00 - 3:00pm or by appointment

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Course material: Lecture viewgraphs and class notes; readings; solutions; sample exams will be posted on the **CourseWeb.**
Textbook: M.D. Ercegovac, T. Lang and J. Moreno, *Introduction to Digital Systems*, John Wiley & Sons, New York, 1999. Digital version available at the **CourseSmart site.**

Grading: Homeworks 10%, quizzes 20%, midterm 30% (February 9, in class), final 40%.
TAs: Discussion 1A: Farahpour Nazanin; Discussion 1B: Hyun Kim; Discussion 1C: Brendon Faleiro
• To get most out of lectures, please read in advance (a) the textbook and (b) class examples.
• Problems solved and discussed in class.
• Solutions to odd-numbered exercises posted on the CourseWeb.

OUTLINE

Lectures 1 - 2: About digital systems. Specification and implementation of combinational systems. High-level specification. Data representation. Binary specification. Switching functions. Boolean Algebra. [Ch. 1, Ch. 2, Appendix A]

Lecture 3: Switching expressions. Examples of specifications. [Ch. 2]

Lecture 4: CMOS switches and gates. Characteristics. Buses and three-state drivers. [Ch. 3]

Lecture 5: Description and analysis of gate networks. [Ch. 4]

Lectures 6 - 7: Design of combinational systems: two-level networks. Karnaugh maps. Two-level networks. Minimal networks. NAND and NOR gates and networks. PLAs and PALs [Ch. 5]

Lectures 8 - 9: Specification of sequential systems. State description. Time behavior. Reduction of the state set. [Sec. 7.1 - 7.7]

Lectures 10 - 11: Implementation of sequential systems. Canonical networks. Analysis and synthesis. Sequential networks with flip-flops.[Sec. 8.1-8.10]

Lectures 12 - 13: Standard combinational modules and networks: decoders, encoders, multiplexers, demultiplexers, and shifters. Uses of modules. [Ch. 9]

Lectures 14 - 15: Arithmetic combinational modules and basic operations. Addition of positive integers and adder modules. Representation of signed integers. Two's complement addition/subtraction, change of sign, sign and overflow detection. [Ch. 10]

Lectures 16 - 17: Standard MSI/LSI sequential modules and networks: registers, shift registers and counters. [Ch.11]

Lecture 18: *If there is time:* Programmable sequential arrays (PSAs), read-only memories (ROMs), and field-programmable gate arrays (FPGAs). [Ch. 12]