Ch 2 (24, 26.1, 26.3, 46.1)

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CSM151B

CSM151B Homework #2

(24)(a) Jump Instruction

- The jump instruction is a j-type instruction and consists of a 26-bit immediate
- Thus, initially the immediate consists of all 1's (and due to data alignment, the 1's are prefixed by two 0's): 0x3FFFFFF or

0011 1111 1111 1111 1111 1111 1111 1111

- Now, the hardware moves the PC to the next instruction (via a left shift by 2) => 0xFFFFFFC or

1111 1111 1111 1111 1111 1111 1100

- As the PC is fixed at 0x02 or 0010 for its most significant 4 bits, the concatenation of the PC's MS 4-bits and the immediate results in => 0x2FFFFFFC or

0010 1111 1111 1111 1111 1111 1100

- As the question is asking if the PC can reach a final address of 0x40000000 with only a single jump instruction, it is not possible as 0x2FFFFFFC < 0x40000000

(b) Branch-on-equal Instruction

- The beq instruction is an I-type instruction and consists of a 16-bit immediate
- Therefore, it is not possible as well, as it can't jump as far as with a 26-bit immediate

(26.1) • This loop will run for 10 iterations, and will result in $s2 = 20
• Roughly, the MIPS loop can be converted to the following C++ code:

```
while ($0 < $t1) {
    $t2 = 1
    $t1 -= $t1
    $s2 += 2
}
```

- Thus, after 10 iterations $t1 will finally be equal to $0, and $s2 will have been incremented by 2 ten times

(26.3) • The MIPS loop consists of 5 statements
• If $t1 is initialized to N, then the loop will consist of N iterations (or 5N instructions)
• Once the beq instruction is finally satisfied, only the first 2 instructions will be executed (and not the rest of the loop) and thus, the total number of instructions executed is $5N + 2$

(46.1) $CPU\ Time = (Instr\ Cnt)(CPI)(Clk\ Cyc\ Time)$

$$CPU\ Time_{new} = (0.75)(Instr\ Cnt_{Arith})(CPI_{Arith})((Clk\ Cyc\ Time_{old}) +$$
$$(Instr\ Cnt_{L/S})(CPI_{L/S})((Clk\ Cyc\ Time_{old}) +$$
$$(Instr\ Cnt_{Branch})(CPI_{Branch})((Clk\ Cyc\ Time_{old})$$
$$= (0.75)(500 \times 10^6)(1)(1.1)((Clk\ Cyc\ Time_{old}) +$$
$$(300 \times 10^6)(1)(1.1)((Clk\ Cyc\ Time_{old}) +$$
$$(100 \times 10^6)(3)(1.1)((Clk\ Cyc\ Time_{old})$$
$$= (412.5 \times 10^6 + 330 \times 10^6 + 330 \times 10^6)((Clk\ Cyc\ Time_{old})$$
$$= (4042.5 \times 10^6)(Clk\ Cyc\ Time_{old})$$

- Thus, the use of the new instruction leads to a large increase in the clock cycle time, which results in a slower execution time
- Therefore, it is not a good design choice