CSM151B
Computer Systems Architecture

Week 4 Discussion

2/2/2018

Logistics

- HW3 due today

Agenda

- Single-cycle microarchitecture

Instruction Processing Viewed Another Way

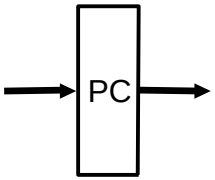
- An instruction processing engine consists of two components
  - **Datapath**: Consists of hardware elements that deal with and transform data signals
    - functional units that operate on data
    - hardware structures (e.g. wires and muxes) that enable the flow of data into the functional units and registers
    - storage units that store data (e.g., registers)
  - **Control logic**: Consists of hardware elements that determine control signals, i.e., signals that specify what the datapath elements should do to the data

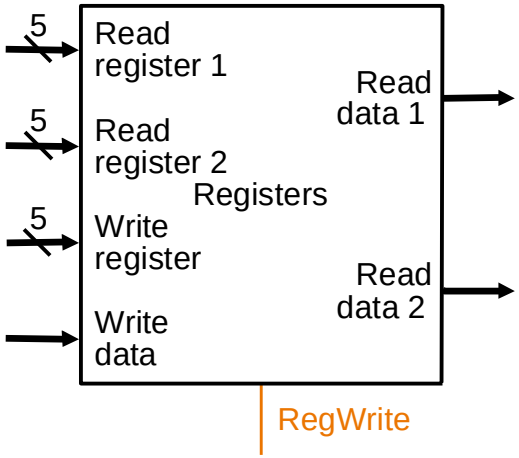
Many Ways of Datapath and Control Design

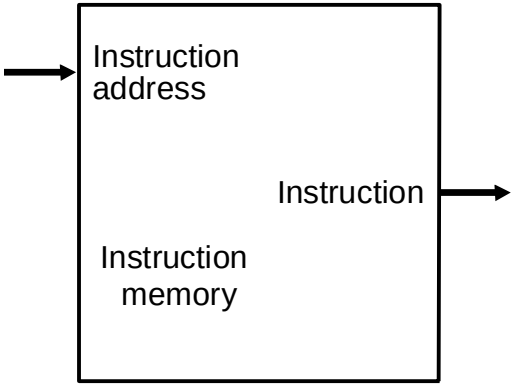
- There are many ways of designing the datapath and control logic
- Single-cycle, multi-cycle, pipelined datapath and control
- Hardwired/combinational vs. microcoded/microprogrammed control
  - Control signals generated by combinational logic versus
  - Control signals stored in a memory structure
- Control signals and structure depend on the datapath design

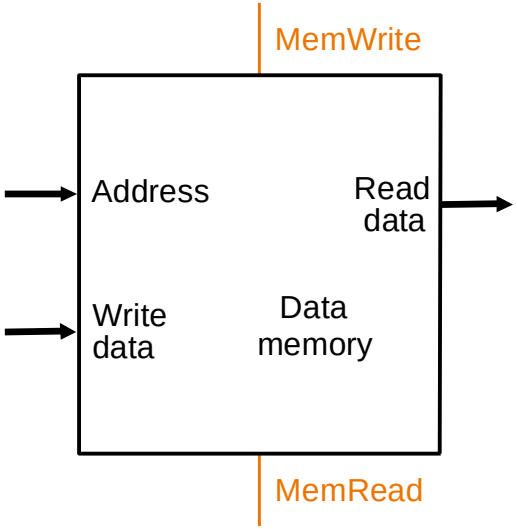
The State Elements

- Data and control inputs

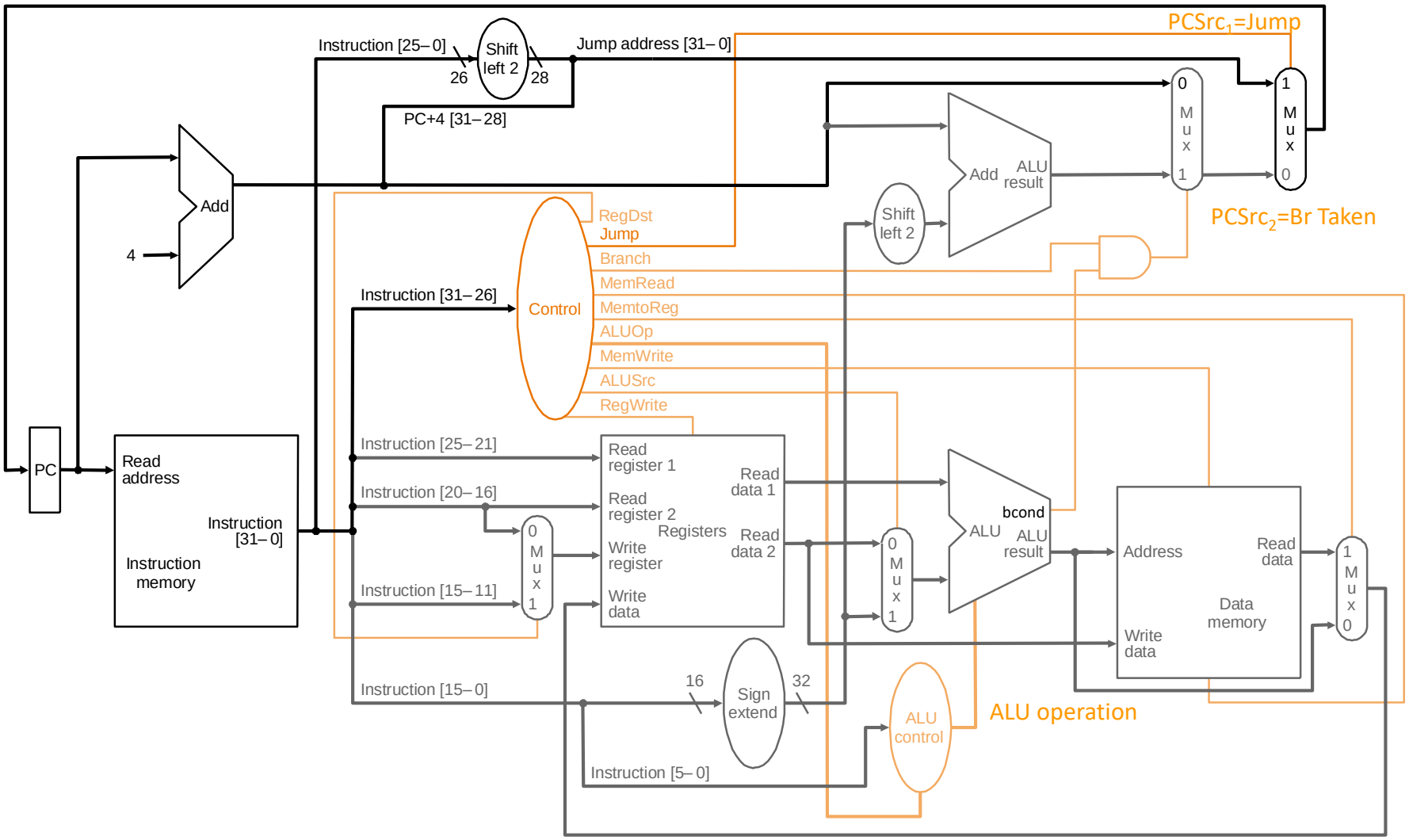




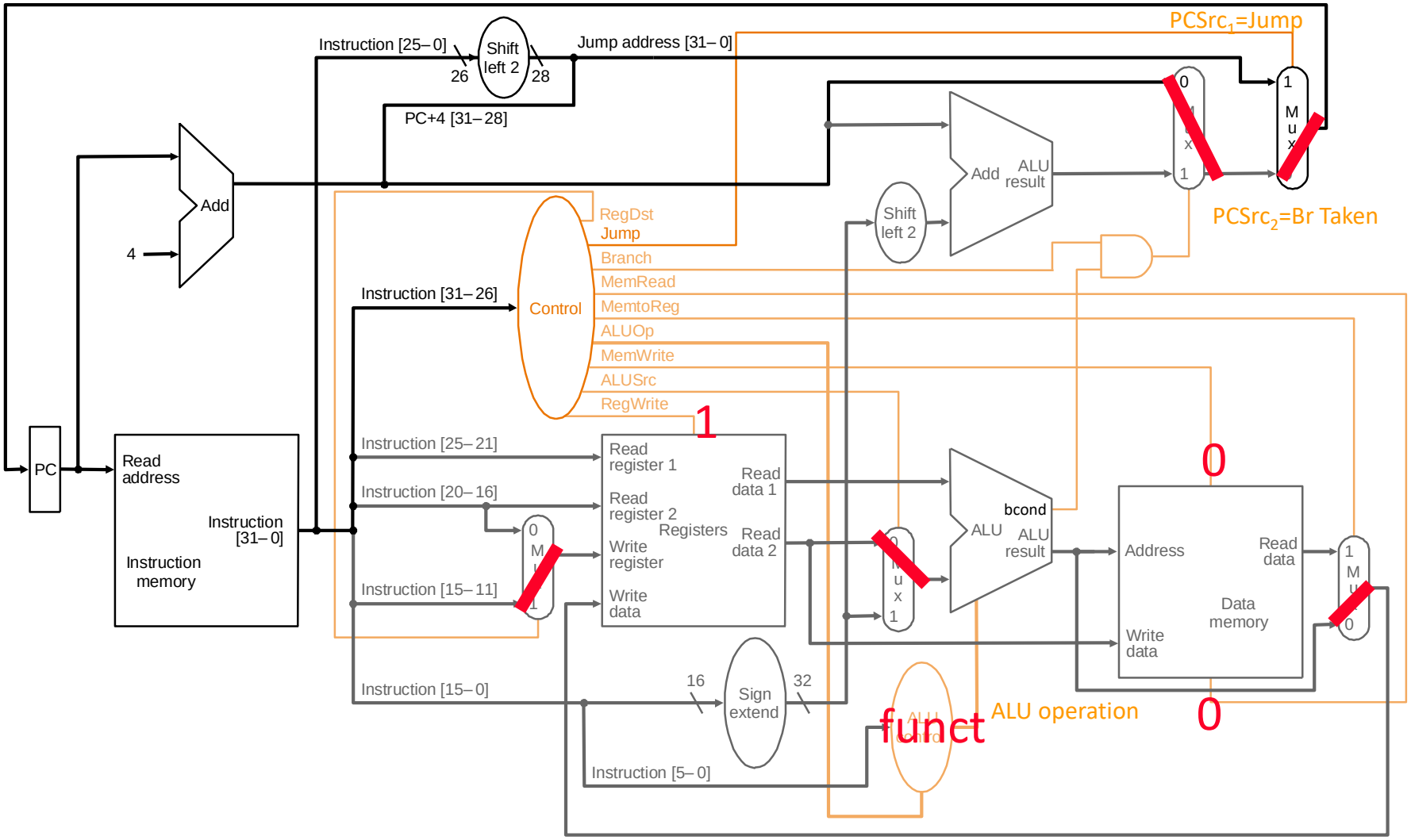




The Full MIPS Datapath



R-Type ALU


PCSrc1=Jump
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Shift left 2
26
28
Jump address [31–0]
PC+4 [31–28]
Add
4
Add
ALU result
Shift left 2
M u x
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Sign extend
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ALU
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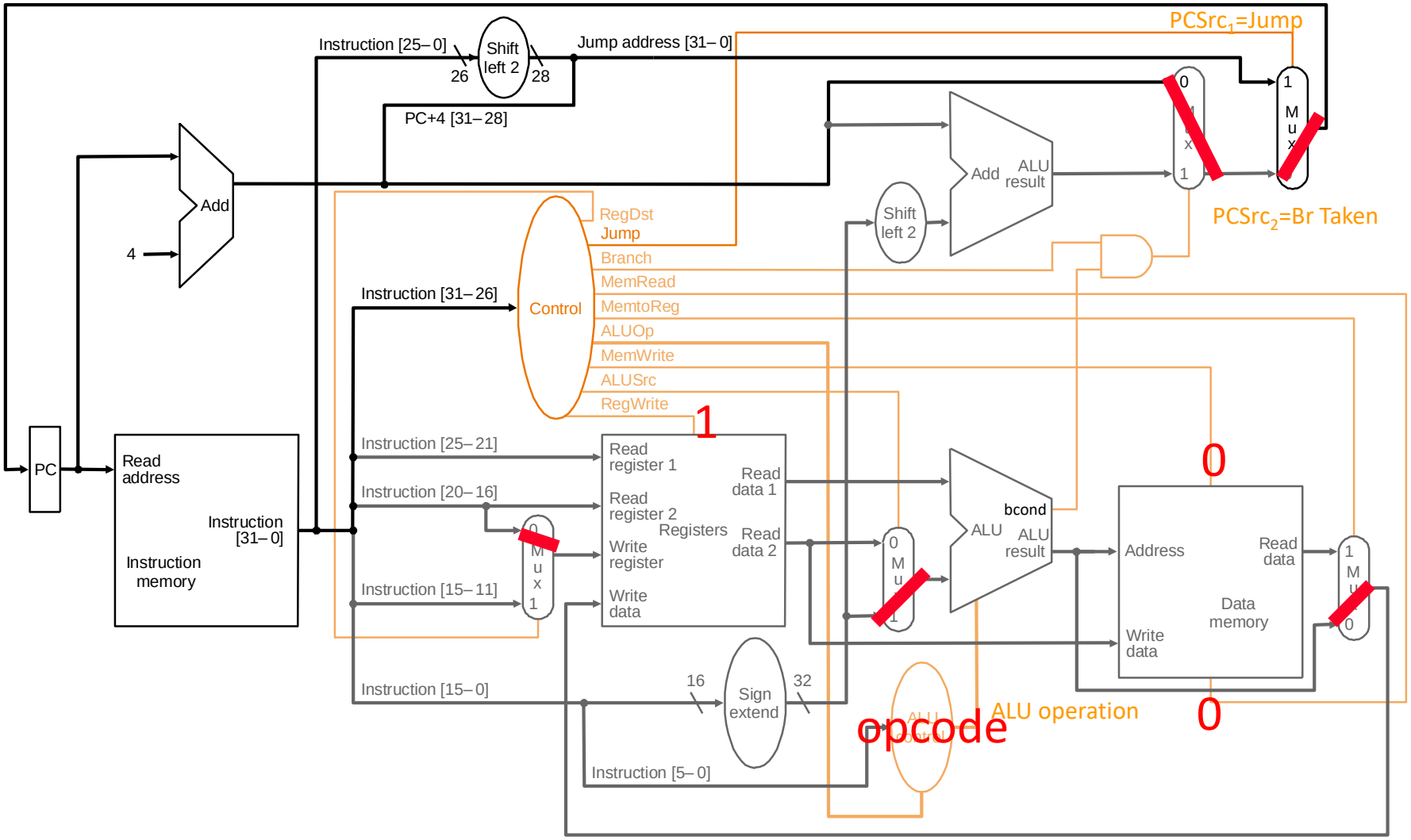
ALU operation

I-Type ALU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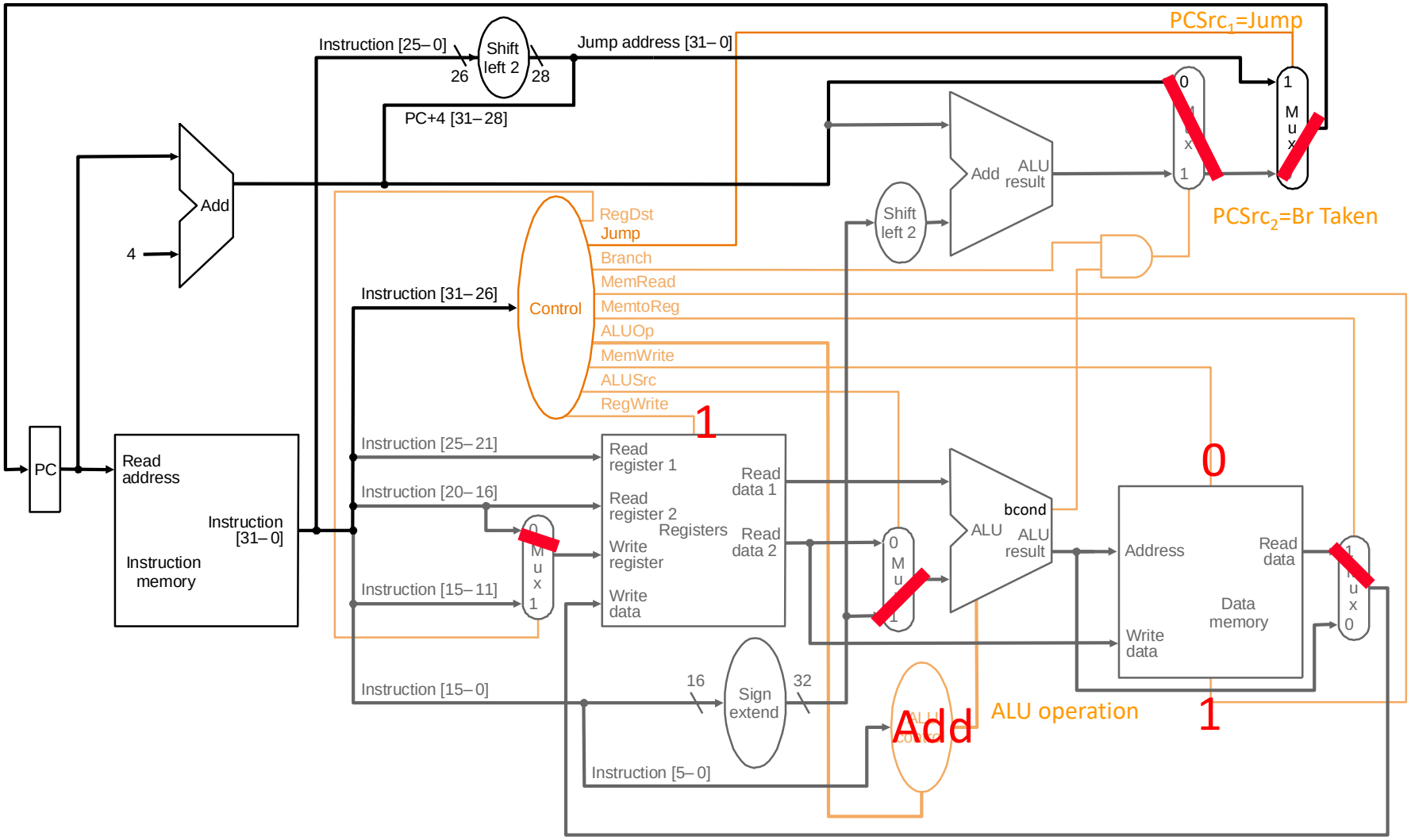
LW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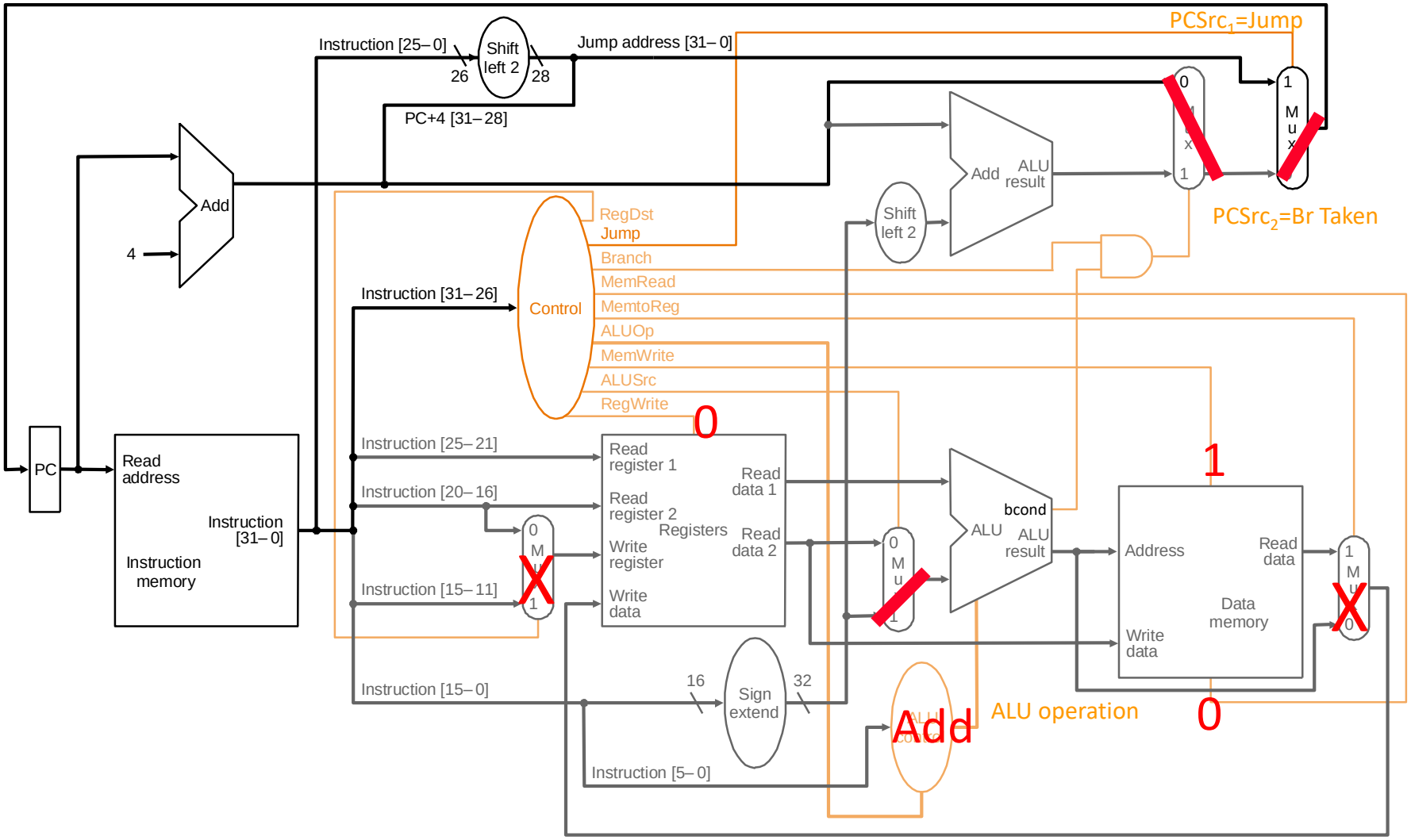
SW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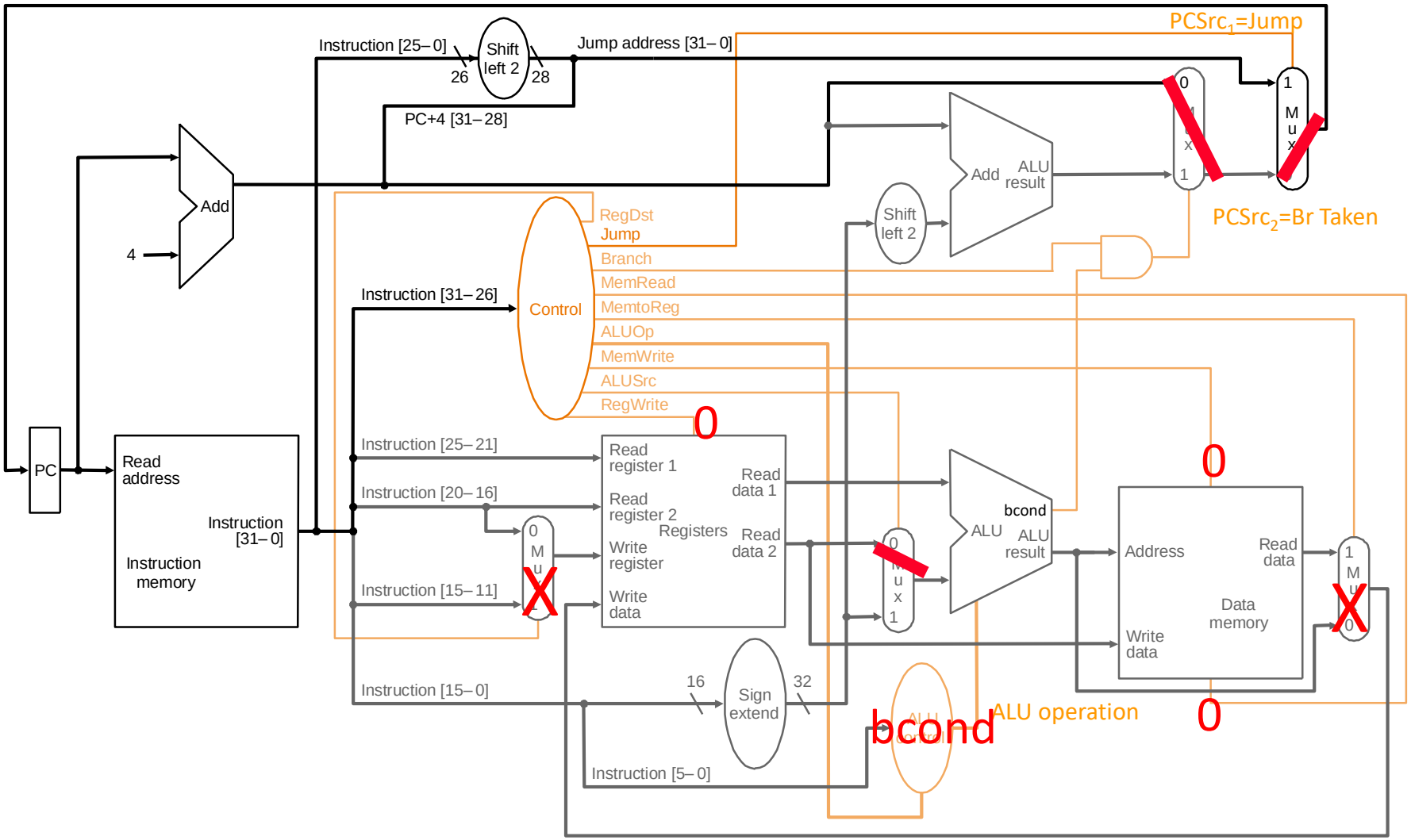
Branch (Not Taken)

Some control signals are dependent on the processing of data



Branch (Taken)

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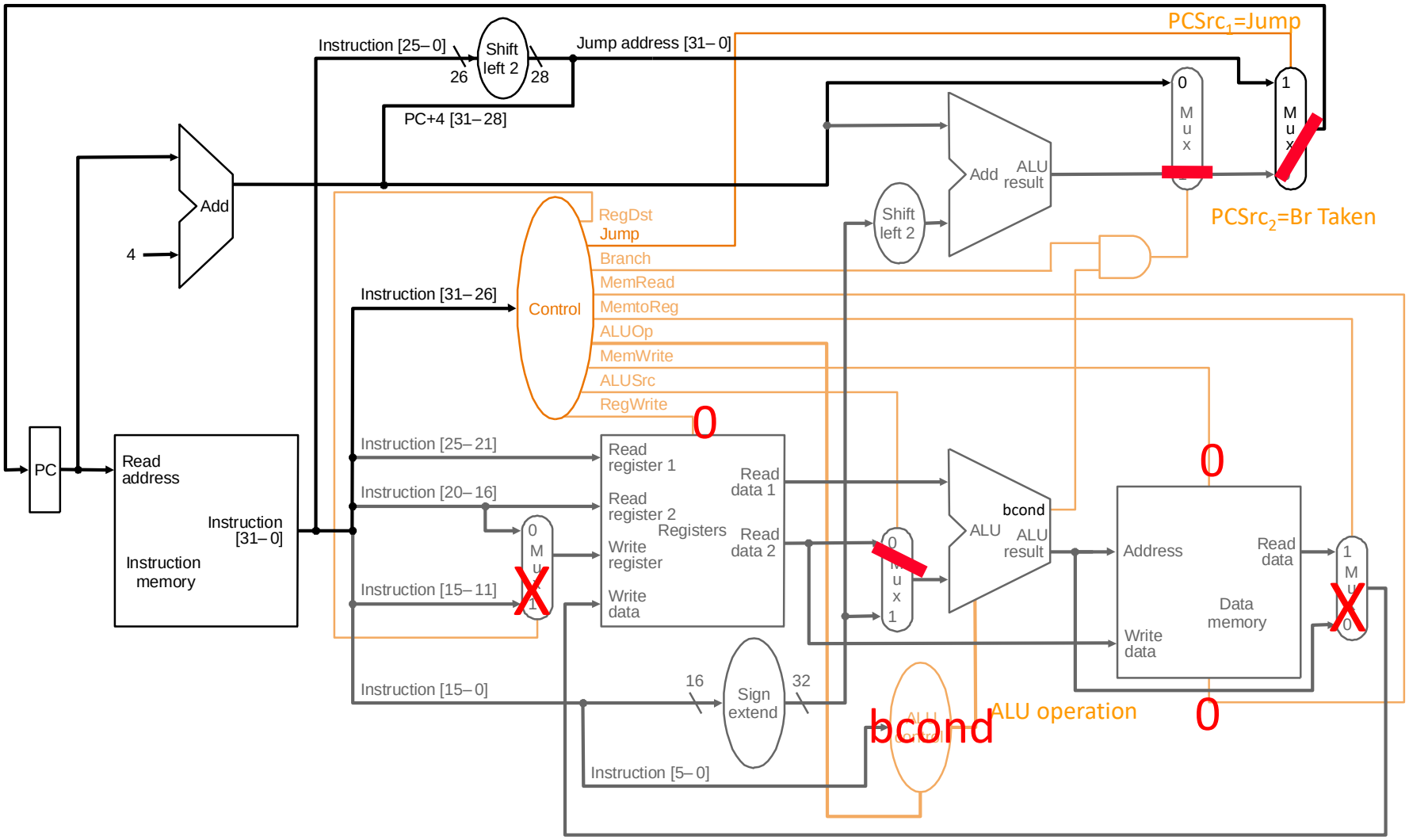
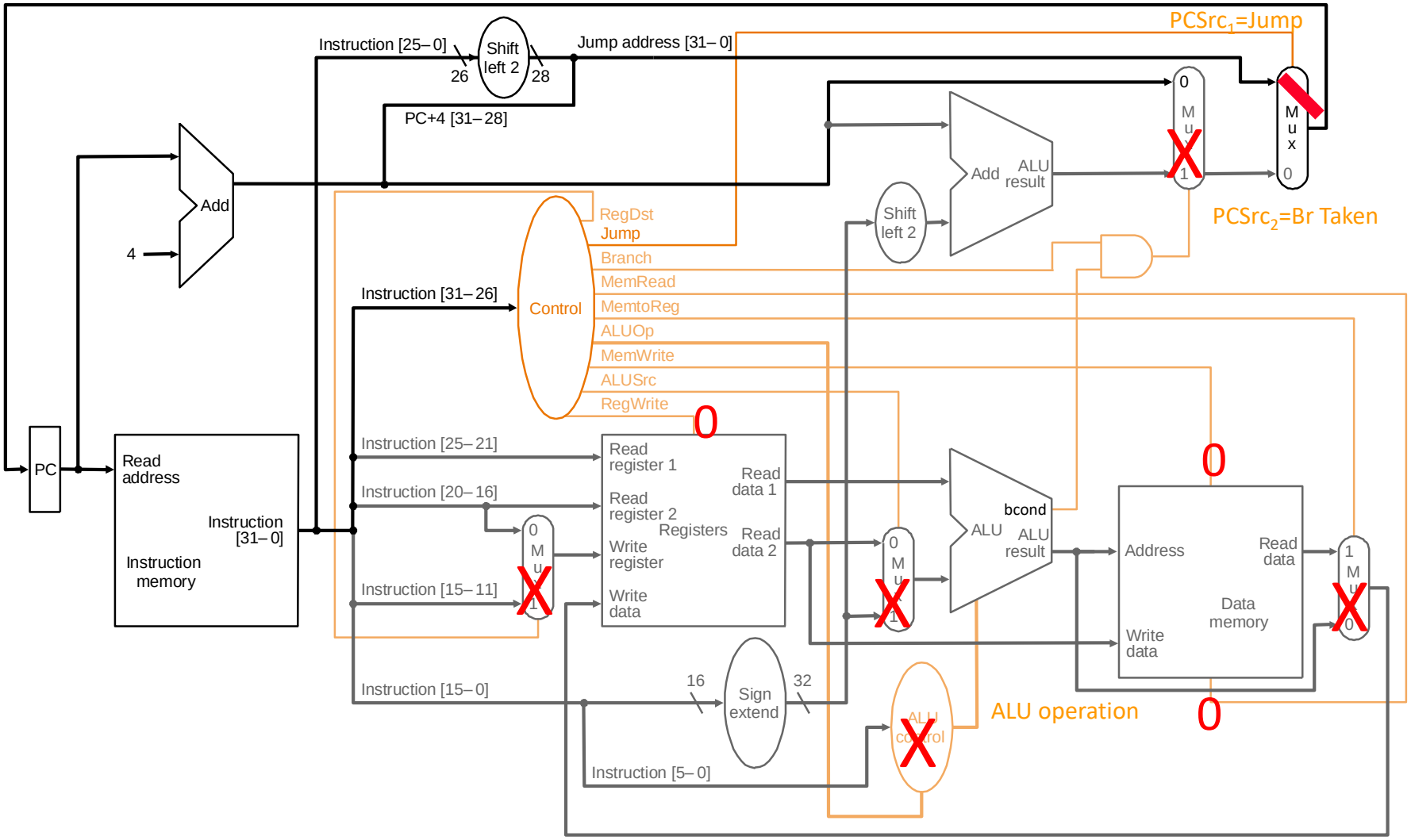


Jump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0
0
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What is in That Control Box?

- Combinational Logic → **Hardwired Control**
  - Idea: Control signals generated combinationally based on instruction
  - Necessary in a single-cycle microarchitecture…
- Sequential Logic → **Sequential/Microprogrammed Control**
  - Idea: A memory structure contains the control signals associated with an instruction
  - Control Store

A Single-Cycle Microarchitecture: Analysis

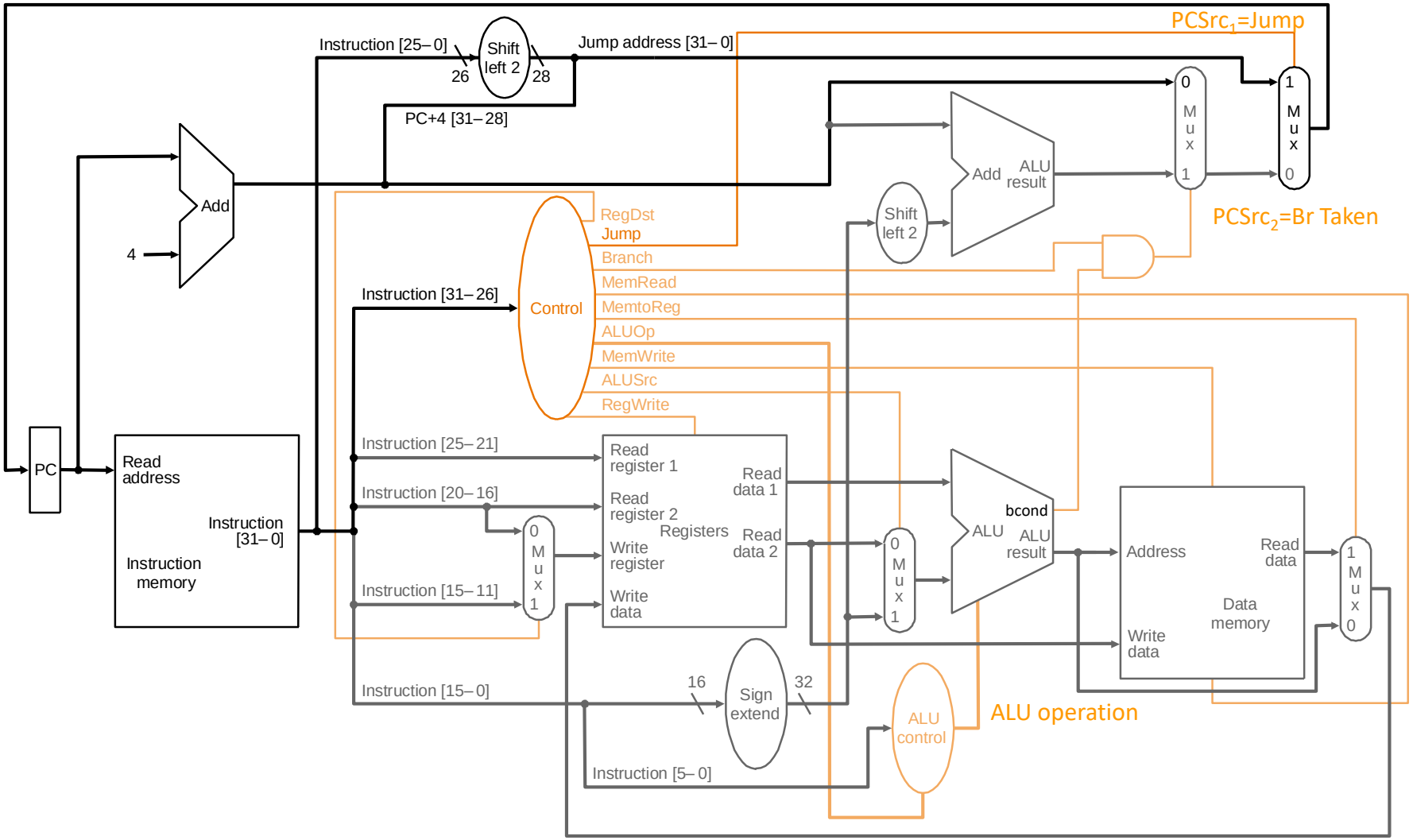
- Every instruction takes 1 cycle to execute
  - CPI (Cycles per instruction) is strictly 1
- How long each instruction takes is determined by how long the slowest instruction takes to execute
  - Even though many instructions do not need that long to execute
- Clock cycle time of the microarchitecture is determined by how long it takes to complete the slowest instruction
  - Critical path of the design is determined by the processing time of the slowest instruction

Single-Cycle Datapath Analysis

- **Assume**
  - **memory units (read or write): 200 ps**
  - **ALU and adders: 100 ps**
  - **register file (read or write): 50 ps**
  - **other combinational logic: 0 ps**

steps	IF	ID	EX	MEM	WB	Delay
resources	mem	RF	ALU	mem	RF	
R-type						
I-type						
LW						
SW						
Branch						
Jump						

Let's Find the Critical Path



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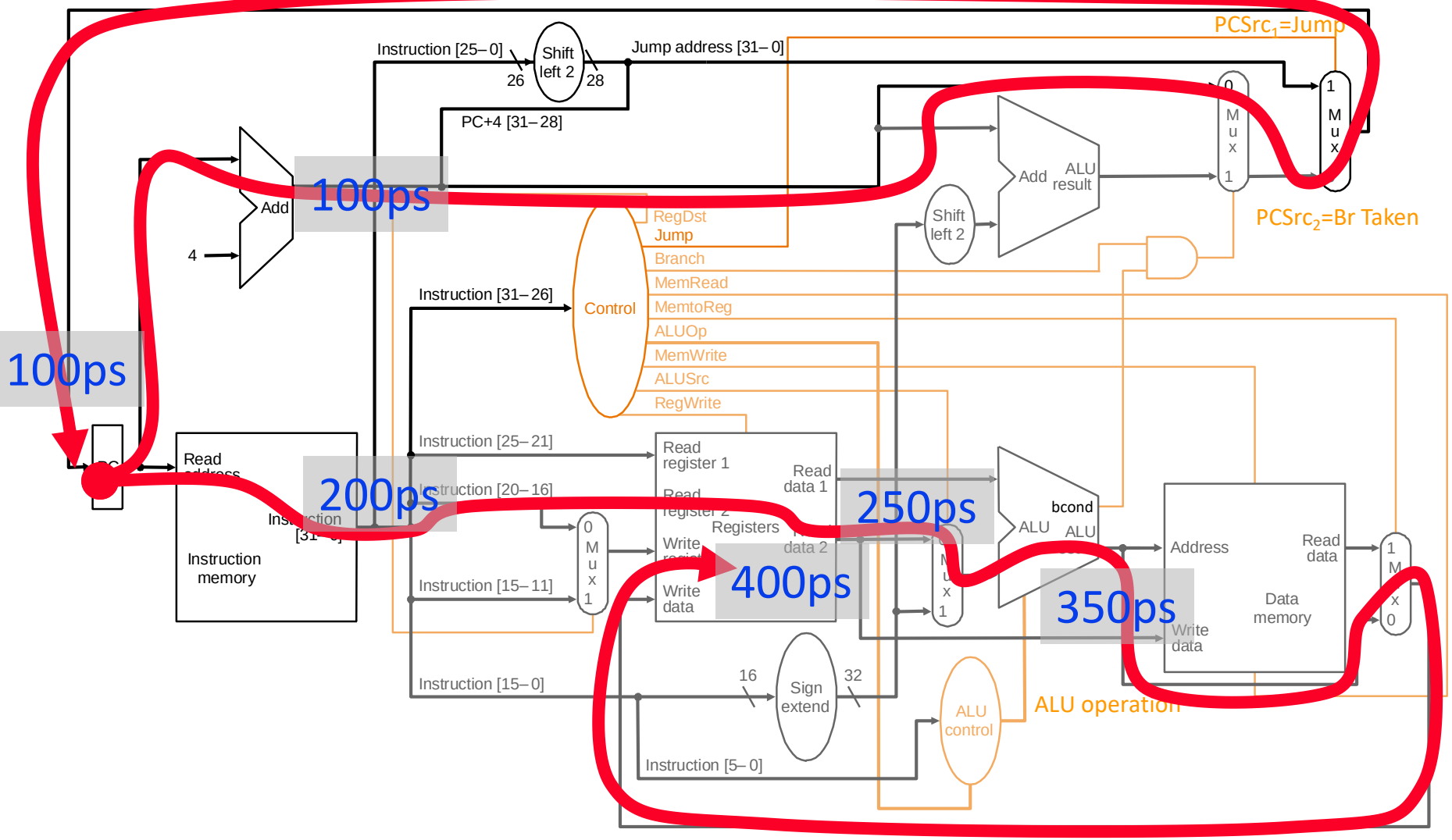
resources	mem	RF	ALU	mem	RF	
R-type	200	50	100		50	400
I-type	200	50	100		50	400
LW	200	50	100	200	50	600
SW	200	50	100	200		550
Branch	200	50	100			350
Jump	200					200

R-Type and I-Type ALU



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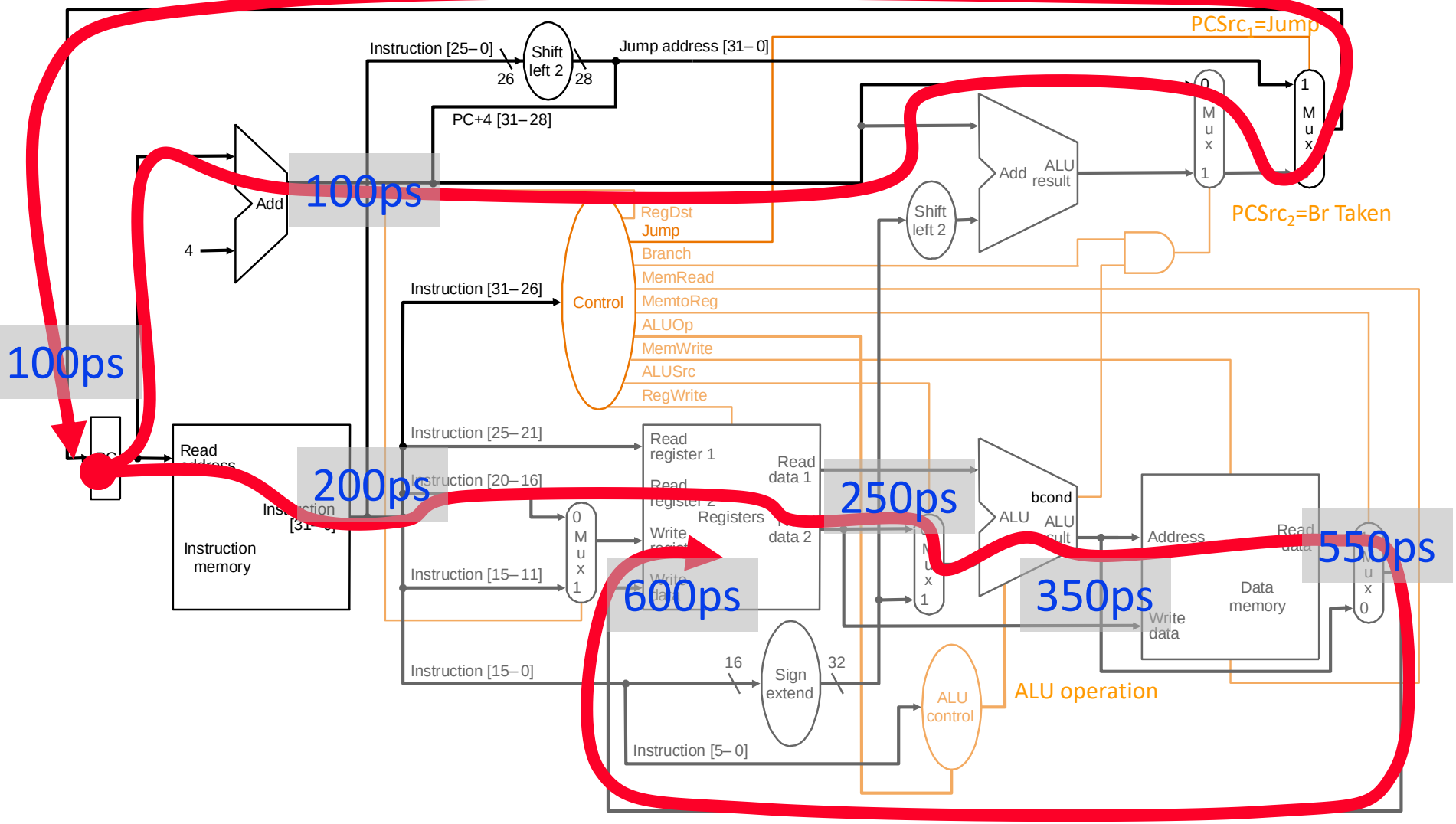
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Read register 1
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Registers
Write register
Write data
Read data 1
Read data 2
0
M u x
1
600ps
250ps
ALU
bcond
ALU result
M u x
1
350ps
Address
Read data
Data memory
Write data
M u x
0
550ps
16
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ALU control
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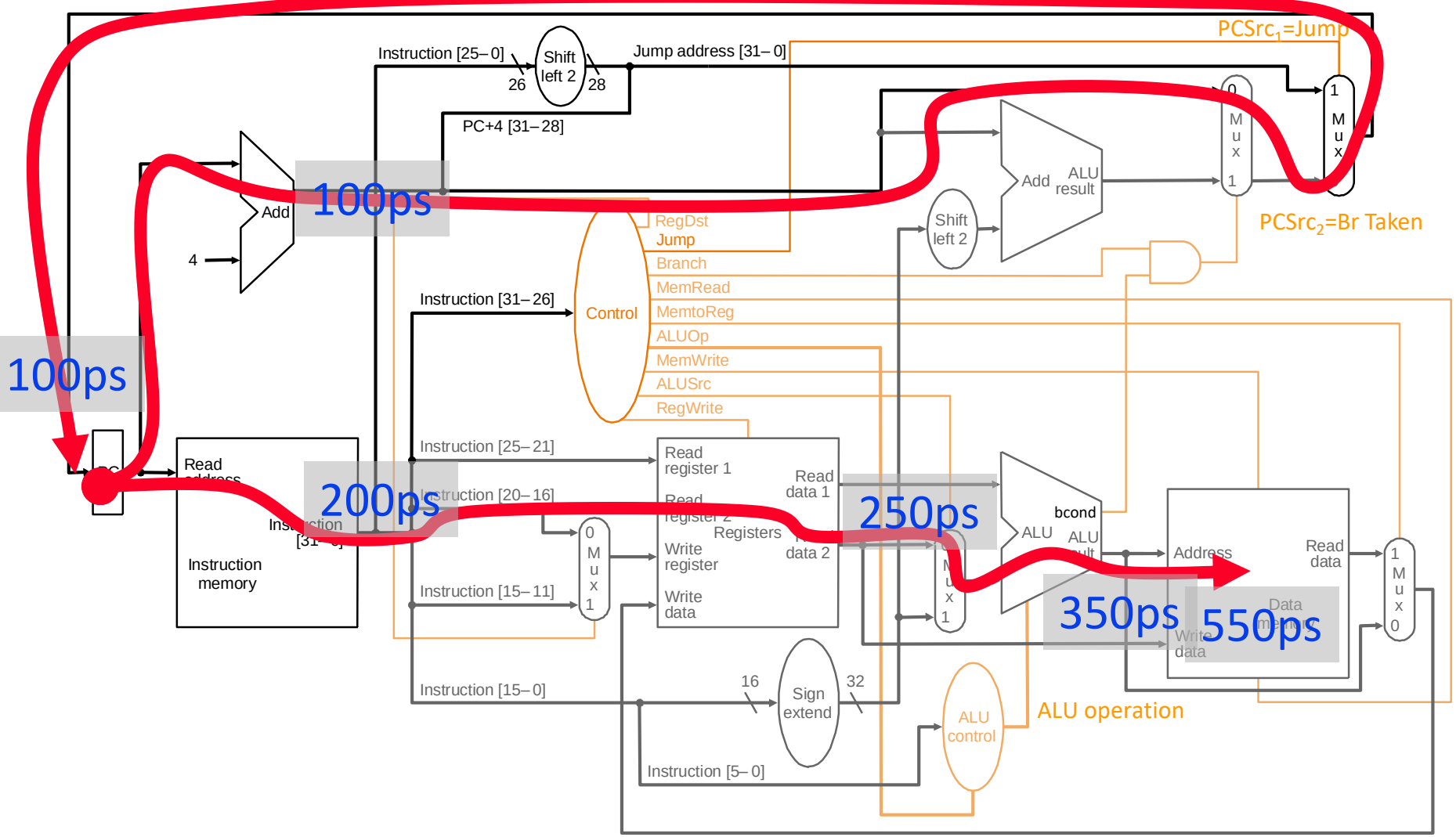
SW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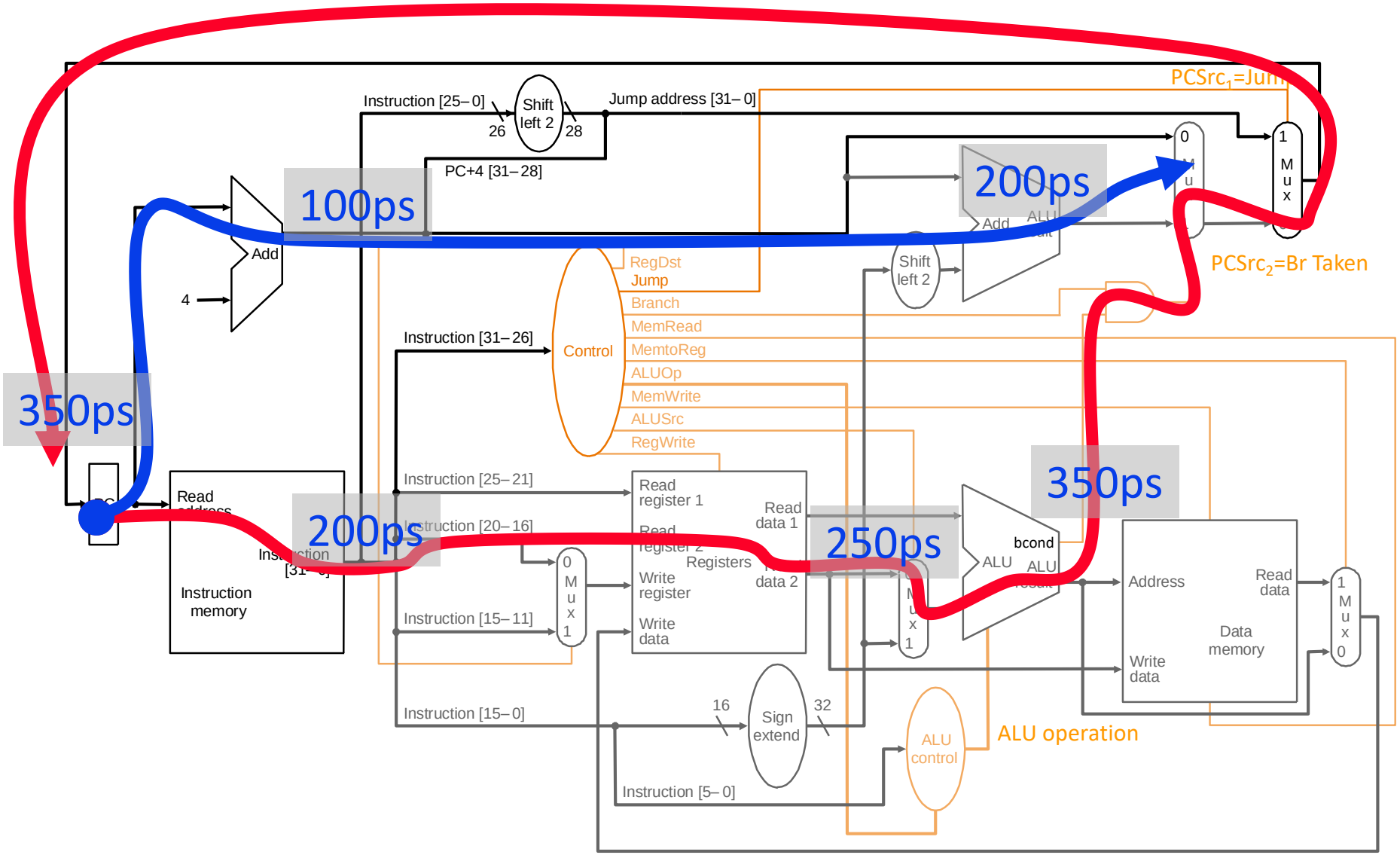
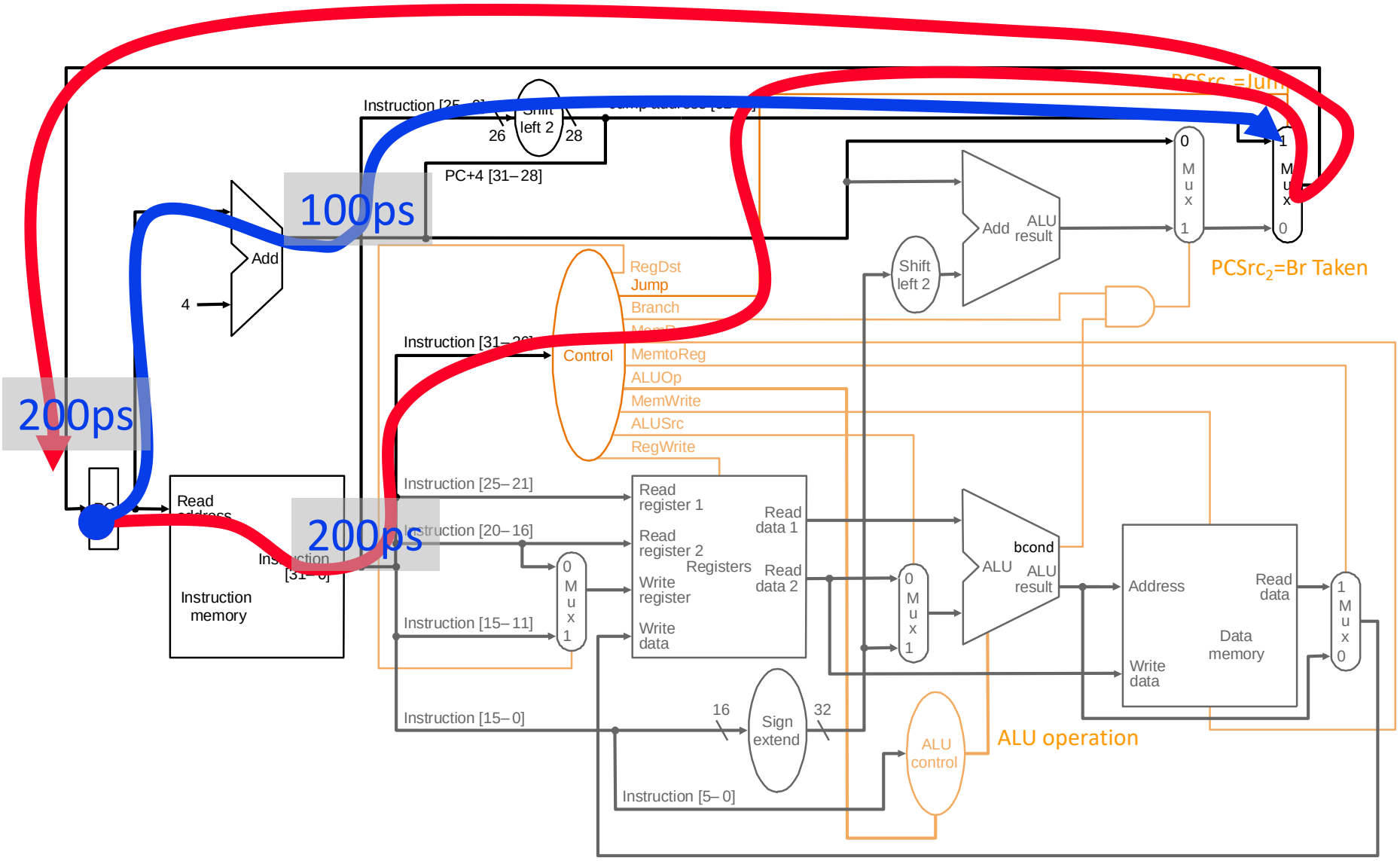
Branch Taken



Jump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Sample Question

- The basic single-cycle MIPS implementation can only implement some instructions. New instructions can be added to an existing ISA, but the decision whether or not to do that depends, among other things, on the cost and complexity such an addition introduces into the processor datapath and control. The new instructions are shown below:

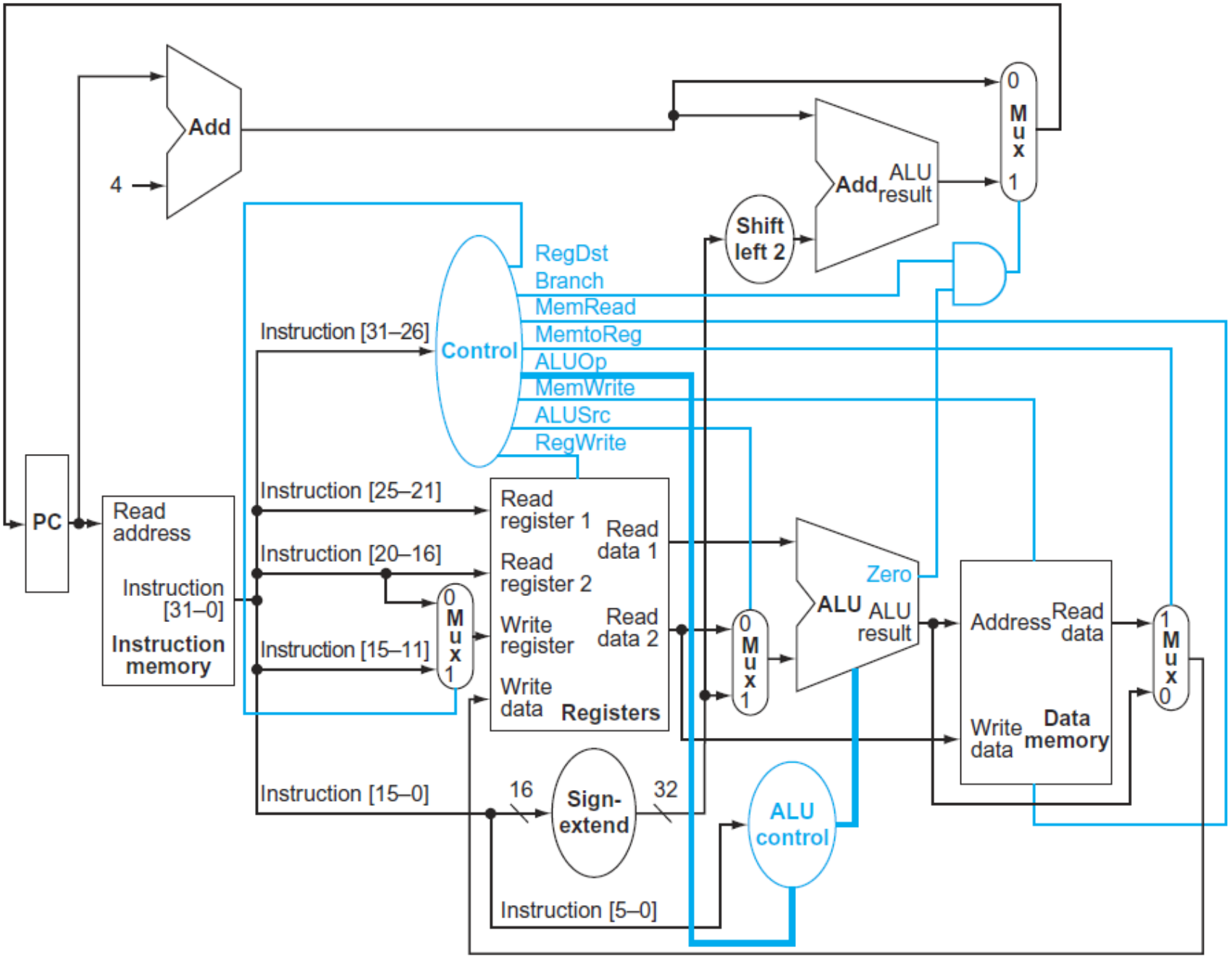
- jri: jump register + immediate
  - jri $s0 IMM
  - PC = R[rs] + sign-extend(IMM)

Sample Question

- PC = R[rs] + sign-extend(IMM)
- What type of instruction should this be?
- We need a register and an immediate. I-type fits the bill.
  - We'd have a unused register if we implement it as an I-type
- We could possibly optimize by defining a new instruction type that has one register and one immediate
  - Trade off?

Sample Question

- PC = R[rs] + sign-extend(IMM)
- What new connections must be made?
- Additional connections
  - Already hooked up in such a way as to do addition of register value and a sign extended immediate
  - From output of ALU to PC
- How do we choose the output of the ALU as the input to the PC
  - Need a MUX somewhere before the PC
  - Also a new control signal to selection input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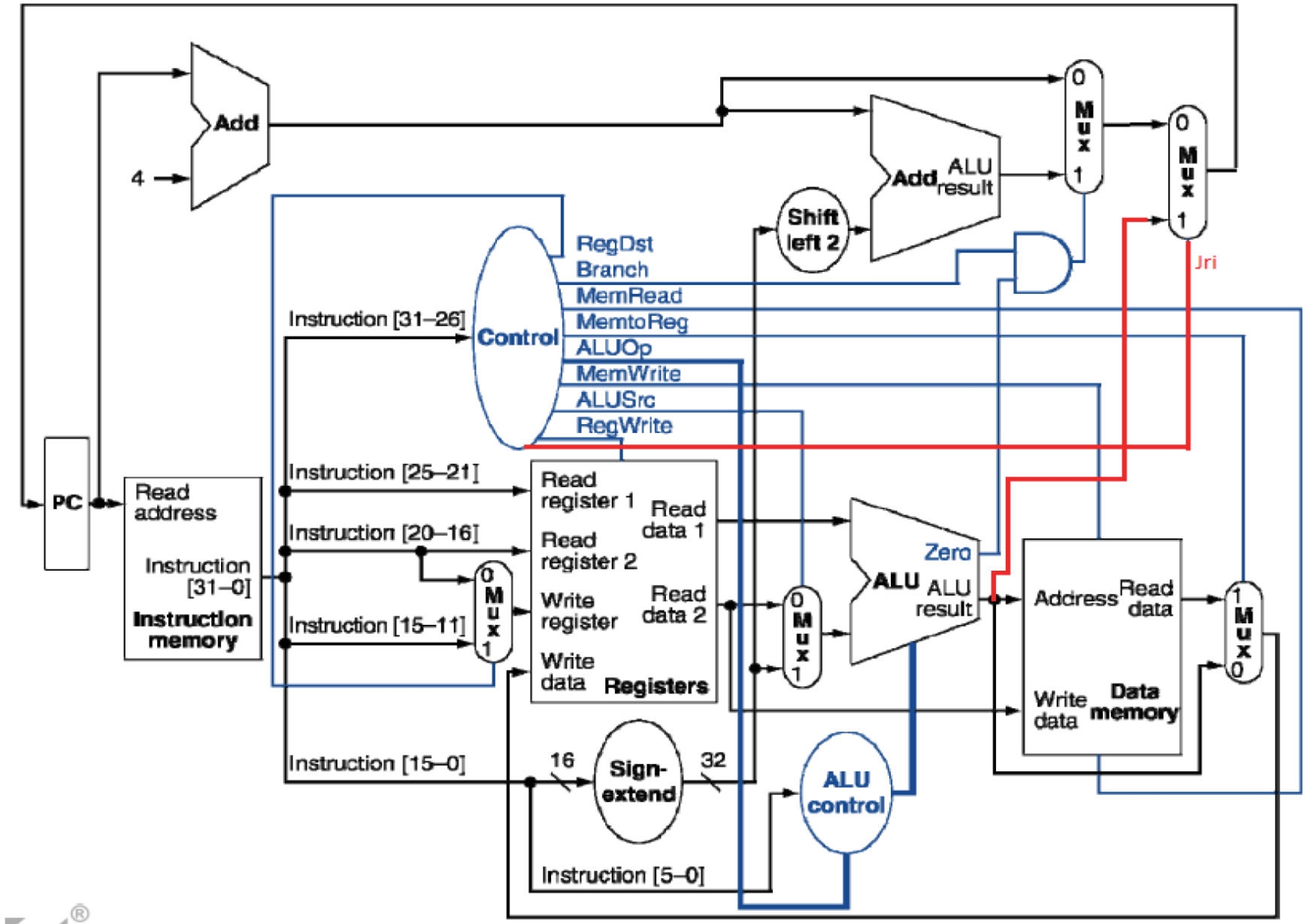
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Slide credits

- Onur Mutlu