Cache Performance

Cache performance depends primarily on hit and miss penalties. A cache hit is quick, but a miss can drastically increase the cycles needed. For example, if the instruction cache (I-cache) miss rate is 2% and the data cache (D-cache) miss rate is 4%, with a base CPI of 2 and a miss penalty of 100 cycles, we can determine the memory miss cycle as follows:

- I-cache miss cycles: $0.02 \times 100 = 2$
- D-cache miss cycles (with 36% of instructions involving loads and stores): $0.36 \times 0.04 \times 100 = 1.44$
- Total memory miss cycles: $2 + 1.44 = 3.44$

This results in a total CPI of 5.44 (base CPI 2 + memory miss cycles 1.44) In an ideal scenario with a perfect cache (no misses), the CPU would run at the base CPI of 2. Comparing the actual CPI to this shows that the CPU would be approximately 2.72 times faster if there were no memory stalls. If we reduce the base CPI by half, the new total CPI becomes 4.44. Memory stalls remain a significant portion of the overall CPI, showing how reducing the CPI alone without addressing memory latency, yields limited results.