1. Create new project -> create new block design

2. add these blocks:

    a. zynq7 processing system

        i. run block automation and do the DDR and FIXED_IO connections

        ii. double click PS -- PS-PL configuration -> GP Master AXI Interface -> M AXI GP0 Interface and make sure its checked

    b. reset for ps

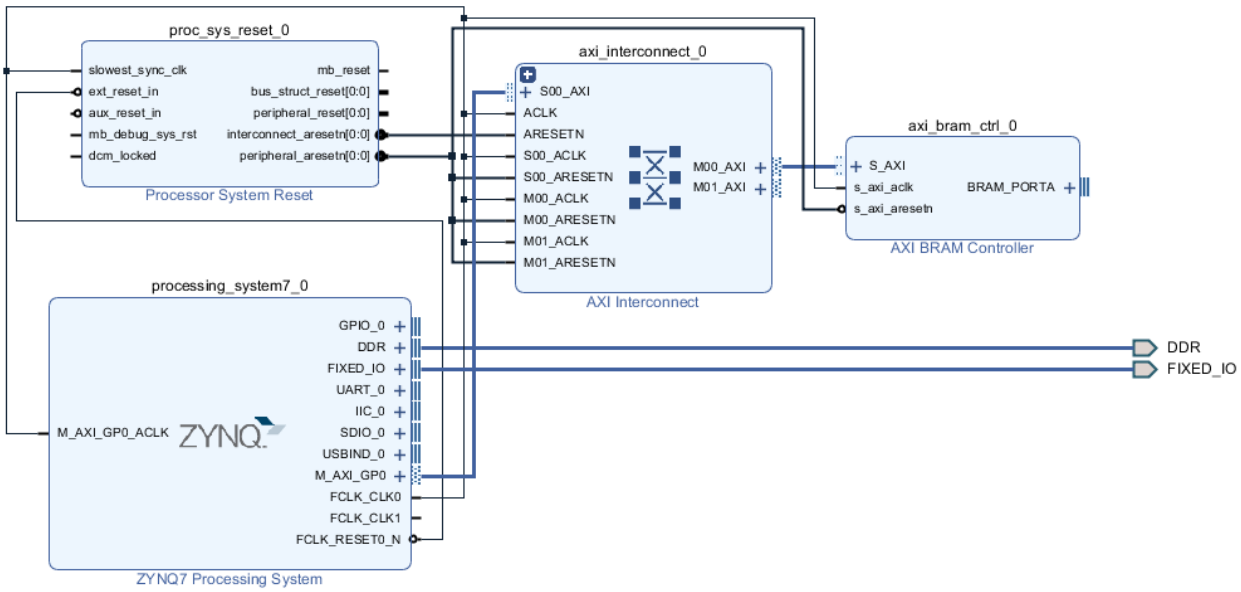
    c. axi interconnect

    d. axi bram ctrl

        i. double click it and changed number of BRAM interfaces to 1 and change to AXI4LITE

3. After all this is added, run connection automation, press regenerate layout to reorder components (*makes it look neater), press validate design and make sure no errors.

4. You should have this after doing everything above, if not, connect all the wires manually and validate design:



5. Tools -> create and package new IP -> new AXI peripheral -> create a name you will remember -> edit IP on the last step and press finish

6. in the package IP vivado -> add all the design sources

7. add this in, the _v1_0.v file, if you are unsure about this step, refer to the github where its uploaded:

    a. At line 7:

parameter WIDTH=32, SIZE=512, //WIDTH is bits per word(shouldn't be changed), SIZE is # of WORDS

parameter NUM_COL = 4,

parameter COL_WIDTH = 8,

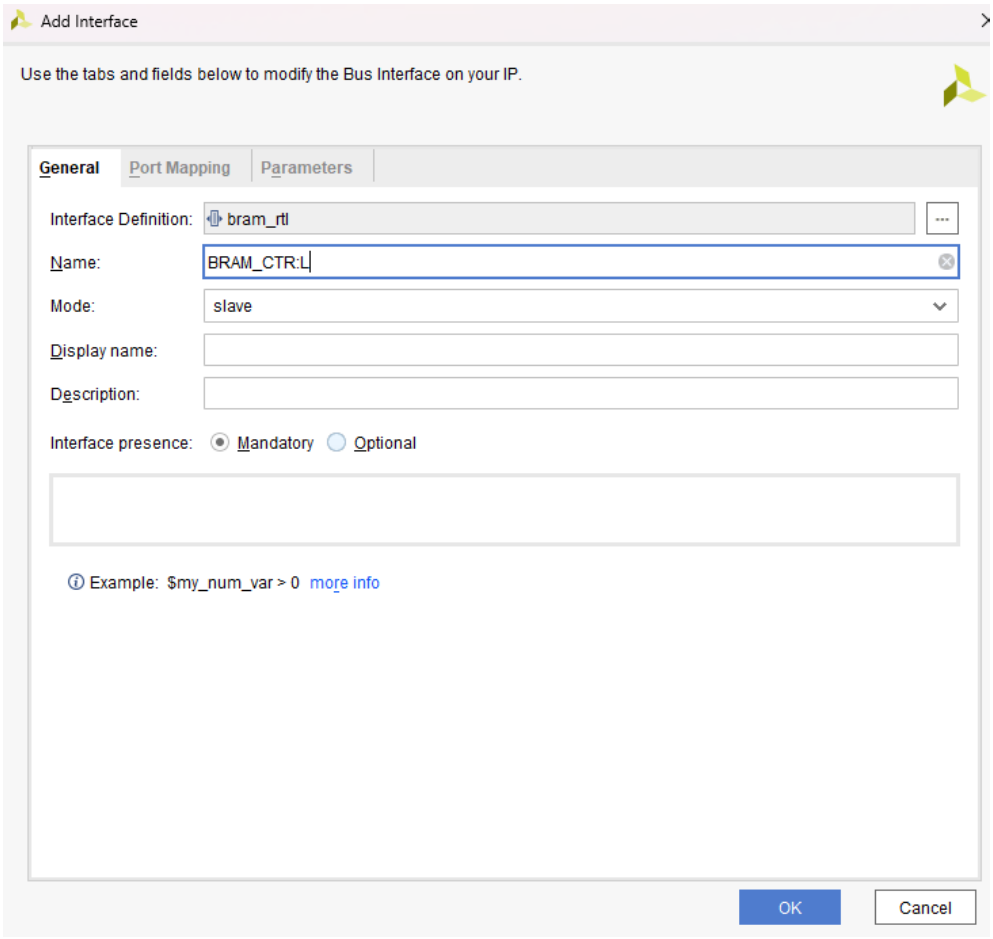
localparam integer LOGSIZE=$clog2(SIZE),

b. at line 49 add: wire ps_reset;

c. add this inside the instantiation .ps_reset(ps_reset)

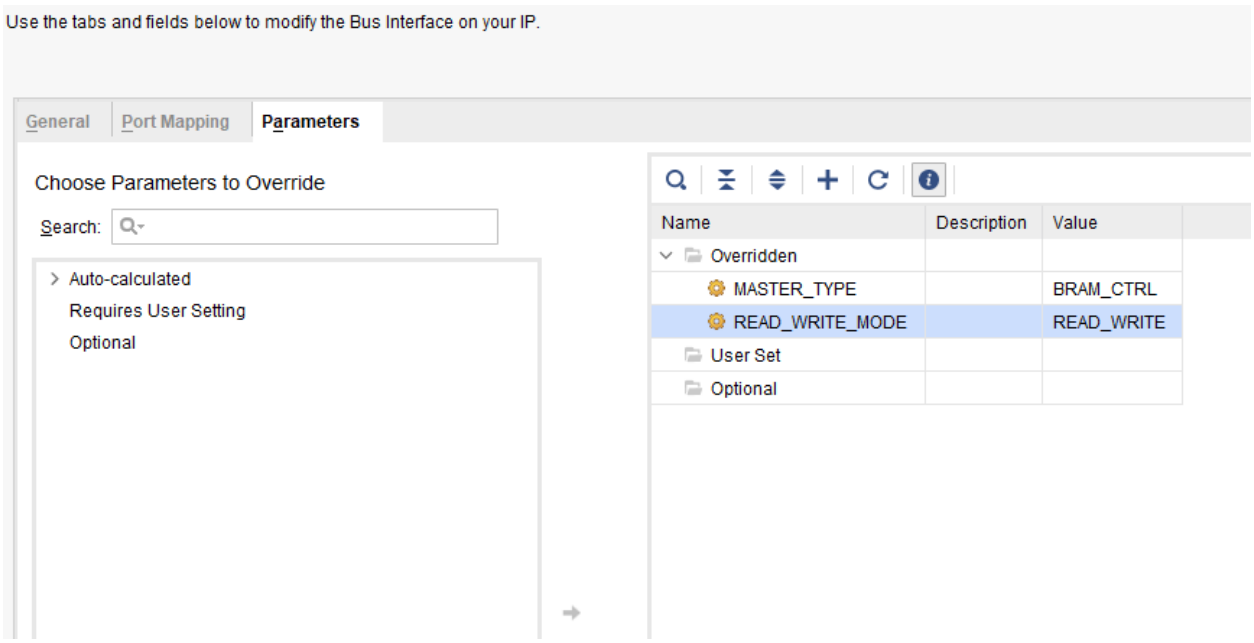
d. output ps_reset, -> add at line 18

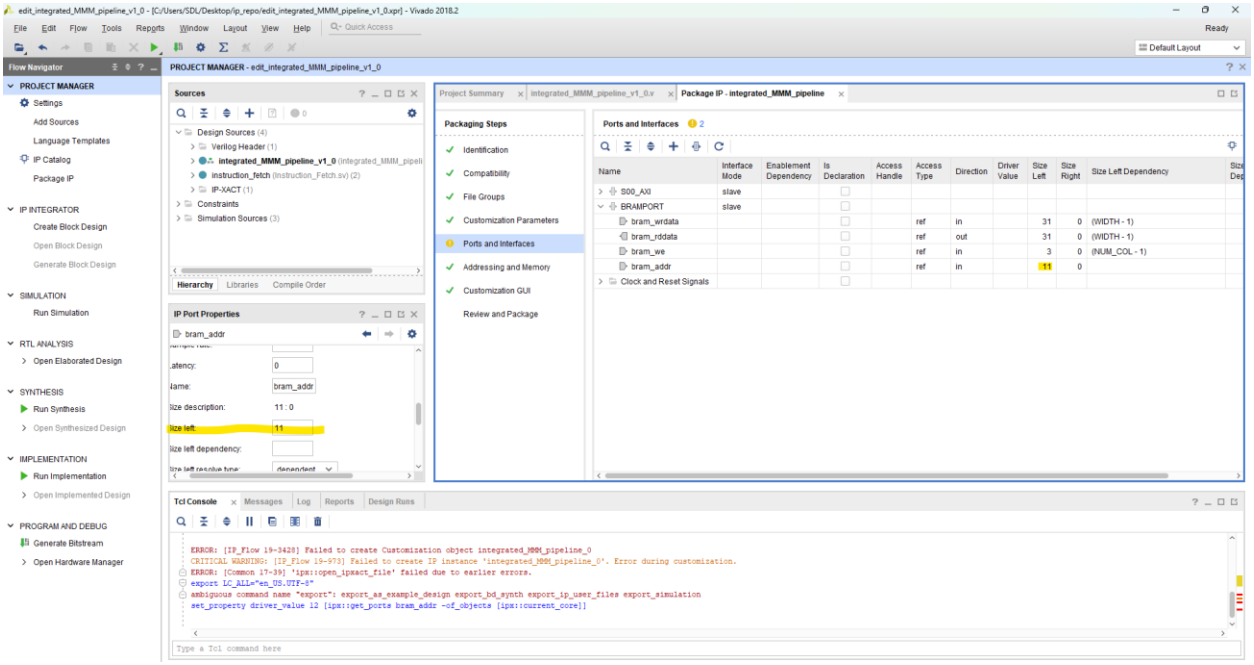
assign ps_reset = slv_reg0; -> add this to line 117



Mapped Ports Summary

Logical Port	Physical Port
ADDR	bram_addr
WE	bram_we
DIN	bram_wrdata
DOUT	bram_rddata

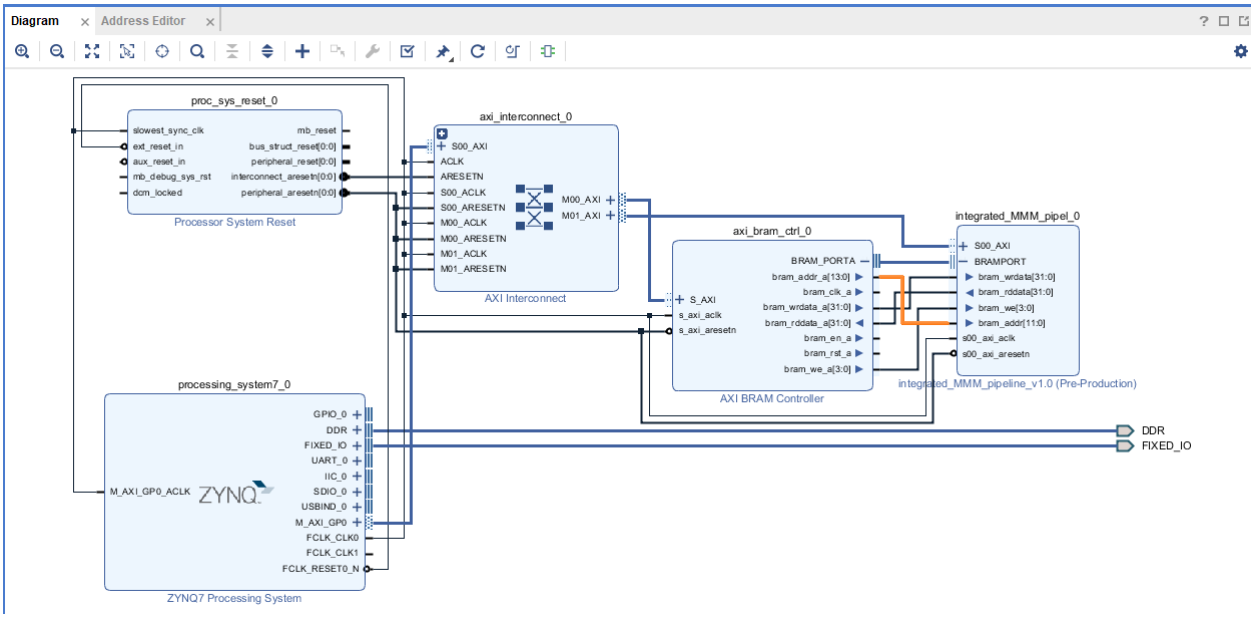




Edit bram_addr in ip port properties for size left and make it 11.

8. merge changes in the packaging steps tabs and package IP.

9. By now, Block diagram should look like this:



Validate design to make sure there is no errors.

Lastly, create HDL warpper