Homework 4

1. **(50%) Virtual and Physical Addresses.** For each configuration (a-c), state how many bits are needed for each of the following:
    - Virtual address
    - Physical address
    - Virtual page number
    - Physical page number
    - Offset

    a. 32-bit operating system, 4-KB pages, 1 GB of RAM

    b. 32-bit operating system, 16-KB pages, 2 GB of RAM

    c. 64-bit operating system, 16-KB pages, 16 GB of RAM

    1. You can fill out a table like this:

Config.	V. Addr.	P. Addr.	V. Page #	P. Page #	Offset
a					
b					
c					

    2. What are some advantages of using a larger page size?

    3. What are some disadvantages of using a larger page size?

2. **(50%) Using the TLB.** As described in your textbook, virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. To speed up this translation, modern processors implement a cache of the most recently used translations, called the *translation-lookaside buffer* (TLB). This exercise shows how the page table and TLB must be updated as addresses are accessed.

    The following list is a stream of virtual addresses as seen on a system. Assume 4-KB pages and a four-entry fully associative TLB with LRU replacement policy. If pages must be brought in from disk, give them the next largest unused page number (i.e., starting at 13).

Address	Result (H, M, PF)
0x0FFF	
0x7A28	
0x3DAD	
0x3A98	
0x1C19	
0x1000	
0x22D0	

Initial TLB: (Note: Values are in base-10)

Valid	Tag	Physical Page #	LRU
1	11	12	2
1	7	4	3
1	3	6	4
0	4	9	1

The LRU column works as follows: The older an entry is, the lower its LRU number will be. Each time an entry is used, its LRU number is set to 4 (since it is now the most-recently used), and the other numbers are adjusted downward accordingly.

Initial Page Table: (Note: Values are in base-10)

Index	Valid	Physical Page or On Disk
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	11
6	0	Disk

7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	12

Given the address stream, initial TLB, and initial page table, show the final state of the system (TLB and page table). Also show for each memory access whether it is a hit in the TLB (H), a hit in the page table (TLB miss, or M), or a page fault (PF).