CSCI-564 Advanced Computer Architecture

Project 1

Due date: 3/15

In this project, you'll be working on a cache simulator. You will be given an incomplete implementation of a cache simulator. Your task is to fill in the missing pieces. Specifically, you need to do the following.

1. Download the simulator from http://inside.mines.edu/~bwu/CSCI_564_17SPRING/Project/CacheSim.tar.gz

2. Understand how the cache module is used by the system module. You can focus on the function MultiCacheSystem::memAccess.

3. Complete the implementation of findTag (20 pts), updateLRU (30 pts), and insertLine (30 pts).

4. Implement a random replacement policy (20 pts). There should be a parameter in your code to control which policy (LRU or random) to use.

5. Compare the hit ratios of the two policies using the provided input file in the tarball.

What you should turn in:

1. Four files: cache.h, cache.cpp, system.cpp, and ratios.txt.
2. Ratios.txt should have two numbers. The first number represents the hit ratio of the LRU cache. The second number represents the hit ratio of the random cache.

Note:

1. The tarball has a trace file pinatrace.out, which is the default input of the simulator.

2. The cache state INV means "invalid", which is the only cache state you need to care about for your implementation.

3. You should heavily document your code so that our TA can easily understand it.