Homework 3

Problem 1 (50%): The size of the branch predictor can affect the amount of aliasing (two branches mapping to the same entry in a branch prediction table) between branches. While this sort of aliasing usually results in negative interference, it can sometimes result in positive interference.

a. Describe a branch T-NT (taken not-taken) pattern for two branches for which aliasing will result in negative interference.
b. Describe a branch T-NT (taken not-taken) pattern for two branches for which aliasing will result in positive interference.
c. Why is it that aliasing usually results in negative interference?

Some key terms here:

Aliasing - The mapping of two or more branches to the same entry in a branch predictor data structure.

Negative interference - The branch prediction rate of either or both aliased branches reduces from what they would've been without aliasing.

Positive interference - The branch prediction rate of either or both aliased branches increases from what they would've been without aliasing.

Problem 2 (50%): Assume a machine with a typical MIPS 5-stage pipeline that uses branch prediction without branch delay slots and has a branch misprediction penalty of 3 cycles. 1 in every 5 instructions is a branch for a certain program, of which 80% are predicted correctly by our branch predictor. Given this:

a. How many cycles would it take to execute 'n' instructions?

b. Imagine we had a Pentium 4 instead which has a 20-stage pipeline because of which the branch misprediction penalty is now a staggering 19 cycles. What should your branch prediction rate be to have the same performance as the MIPS machine we saw in (a).