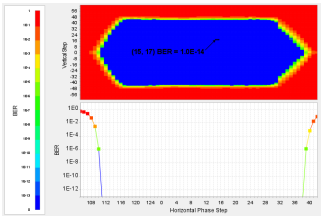
Feb. 3 loopback tests

- Performed internal and external loopback tests
- Clock rate: 156.25 MHz (reference clock used for transceivers)
- Test pattern: PRBS7
- Data rate: 10 Gbps
- Main 16 transceivers implemented in project (3 are functioning)
- Project uses TFM framework

Internal loopback tests

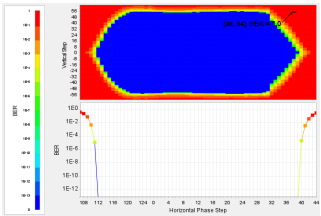
Link 0

56/89



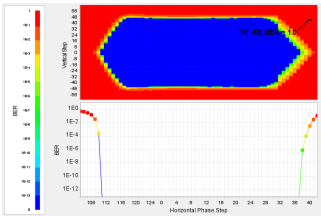
Link 7

56/111



Link 15

55/93

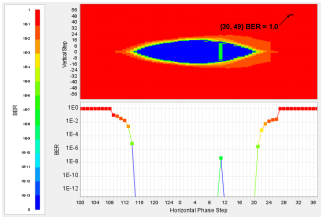


Currently we are not sure which link corresponds to which SMAs (Kade will check)

External loopback tests

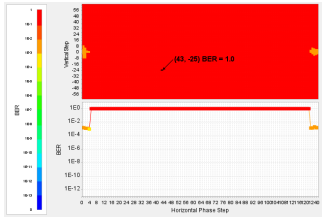
Link 0

34/31



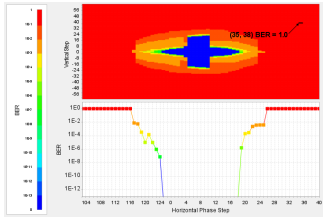
Link 7

no eye



Link 15

22/43

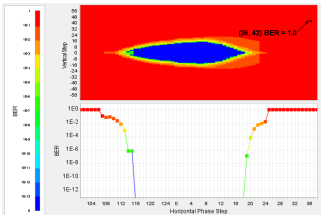


These diagrams looked very strange, so we tried power cycling

External loopback tests (after power cycling)

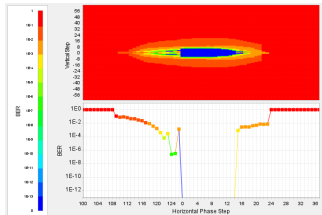
Link 0

33/29



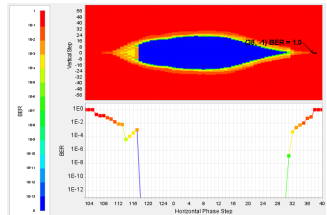
Link 7

22/11



Link 15

41/44



- Look better, but still not great (especially link 7)
- This Friday we will try a project with 64-bit interfacing