XCHG EAX, EAX translates to NOP

When having two MOV pointer goes to lates

Many memory errors (page faults, swaps from memory to disk)

Retiring=committing

Real writing to memory cannot happen out of order, making usage of store forwarding

2 active hyperthreads on one memory buffer (then buffer is evenly partitioned between both)

Mfence guarantees that stores and loads before are finished

Weak consistency

Our instructions appear in order

Mfence ensures ordering

Branch target buffer contains only a part of the address – in case of miss match we just loose performance (data cache claims to be always correct and thus requires whole address to ensure correctness)

Declaration as long or short branch depends on the branch predictor state

Branch history slide!!

Detect branch access with cache access on BTB?

Knock knock

Branch prediction

Whos there

TODO read Jump overASLR: Attaking branch predictors to bypass ASLR